

Schmitt-trigger circuit

The invention relates to a Schmitt-trigger circuit as described in the introductory part of Claim 1.

A Schmitt-trigger circuit comprising two emitter-coupled transistors is known from JP-A 60136413(A). The input voltage is applied to the base of one
5 transistor (first input). The second input, i.e. the base of the second transistor, is connected to a current mirror and to the collector of the second transistor. The first and the second transistor have their emitters connected to a current source.

The known Schmitt-trigger circuit cannot readily be fabricated in integrated circuit technology, because resistors, in particular those having high values,
10 are difficult to integrate.

Therefore, it is an object of the invention to provide a Schmitt-trigger circuit which does not employ any resistors.

In a Schmitt-trigger circuit of the type defined in the opening paragraph this object is achieved by means of the characterizing features in Claim 1.

15 In this Schmitt-trigger circuit a current will flow into the first current source via the input stage of the first current mirror and the differential amplifier if the input signal is small enough. The current reproduced by the first current mirror flows from the output stage of this current mirror into the second current source via the semiconductor junction. No current will flow into the first diode array because the
20 voltage across the current-mirror output and the semiconductor junction is smaller than two diode voltages. If the input signal is large enough there will be no current in the first current mirror and the semiconductor junction. The current which flows into the second current source is supplied by the first diode array.

If the semiconductor junction is a base-emitter junction of a feedback
25 transistor which has its base coupled to the output of the first current mirror and its emitter to the base of the second transistor, the current gain from the output of the first current mirror to the base of the second transistor will be higher, which causes the trigger circuit to change over more rapidly.

The output signal can be derived by means of, for example, a further current mirror at the first diode array. The output signal changes from a low to a high level at a first switching threshold, which depends upon the voltage of the output stage of the first current mirror and the base-emitter voltage of the feedback transistor. The
5 second switching threshold, at which a change from a high to a low level takes place, depends upon the sum of the forward voltages of the diode elements in the first diode array.

The first diode array should comprise at least two series-connected diode elements. The diode elements are poled in the forward direction for the current which
10 flows to the second current source.

The hysteresis width, i.e. the spacing between the two switching thresholds, is dictated by the number of diode elements in the first diode array. The switching thresholds can be reduced, while maintaining their spacing, in that a second diode array is arranged between the first and the second coupling point.

15 Preferably, the output signal is taken from the first diode array by means of a current mirror. The first diode array is then arranged in the input-current path of an input stage of a second current mirror having an output stage connected to the output terminal.

In the currentless state temperature variations or crystal defects may give
20 rise to a leakage current in the output stage of the first current mirror. In order to drain (absorb) this leakage current, the collector of the first transistor is connected to an input of a third current mirror which has an output coupled to an input of a fourth current mirror having an output connected to the base of the feedback transistor. The leakage current is then drained by the output stage of the fourth current mirror. Moreover, the
25 loop gain is increased, which improves the edge steepness of the output signal at the upper switching threshold.

In order to prevent the first transistor of the differential amplifier from being driven into saturation for high input voltages, the input terminal is coupled to the base of the first transistor via an input diode array.

30 In a further embodiment of the invention the input of the first current mirror is preceded by an input stage of a fifth current mirror, which has an output stage coupled to an input stage of a sixth current mirror having an output stage connected to the output terminal. This embodiment may be used to drain the leakage current of the

output stage of the second current mirror in the currentless state. The output stages of the second and the sixth current mirror are then interconnected.

Said further embodiment may also serve to apply the output signal to a circuit in I²L-technology. The second current mirror can then be dispensed with and the first and the second current source each form a current-source array which comprises transistors whose bases are connected to a common injector.

Embodiments of the invention will now be described in more detail with reference to the drawings. In the drawings:

Fig. 1 is a simplified circuit diagram of a Schmitt-trigger circuit,
Fig. 2 shows the transfer characteristic of the Schmitt-trigger circuit, and
Figs. 3 and 4 show more detailed embodiments of the Schmitt-trigger circuit.

The Schmitt-trigger circuit shown in a simplified form in Fig. 1 comprises a differential amplifier 1 comprising two NPN transistors 2 and 3, whose emitters are connected to a current source 4. The other terminal of the current source 4 is connected to the negative power supply terminal of a voltage source. The collector of the transistor 2 is connected to the positive power supply terminal 50 of the voltage source, and an input voltage U_e on the input terminal 52 is applied to the base of the transistor 2. The collector of the transistor 3 is connected to an input stage of a first current mirror 5. The input stage comprises a PNP transistor 6, which has its emitter connected to the positive power supply terminal 50 and which has its base and its collector connected to the collector of the transistor 3. The output stage of the current mirror 5 is formed by a PNP transistor 7 whose base is connected to the base of the transistor 6 and whose emitter is also connected to the positive power supply terminal 50. The collector of the transistor 6 is connected to the base of an NPN-type feedback transistor 8 whose collector is connected to the positive power supply terminal 50 and whose emitter is connected to a second current source 9, to the base of the transistor 3 and to the emitter of an NPN transistor 10 connected as a diode element. The other terminal of the current source 9 is connected to the negative power supply terminal 51. The base and the collector of the transistor 10 are connected to the collector and the base of a PNP transistor 11, which constitutes the input stage of a second current mirror 12. The emitter of the transistor 11 as well as the emitter of a PNP transistor 13 are connected to the positive power supply terminal 50. The base of the transistor 13 is

connected to the base of the transistor 11. The collector of the transistor 13 constitutes the output 53 of the Schmitt-trigger circuit.

The operation of the Schmitt-trigger circuit will now be explained by means of the transfer characteristic shown in Fig. 2. When the input signal U_e is negative, the transistor 2 is turned off and the transistor is turned on. A current flows into the current source 4 via the transistor 6 of the current mirror 5 and the collector-emitter junction of the transistor 3. The conductive feedback transistor 8 feeds a substantially equal current to the current source 9. The transistor 7 in the output stage of the current mirror 5 is saturated. Since the transistor 8 is turned on, the diode junctions of the two transistors 10 and 11, which are connected as diode elements, are short-circuited. As a result of this the current mirror 12 is in a currentless state and the output voltage U_{amin} supplied to the output is approximately zero, relative to the negative power supply terminal 51.

The output voltage U_a changes from a low level U_{amin} to a high level U_{amax} when the input voltage U_e is equal to U_{s1} . The transistor 3 is then turned off and the transistor 2 is turned on. No current flows via the current mirror 5 and the transistor 8 is turned off. The current source 9 draws its current from the current mirror 12 and the transistor 10. Now the output voltage is equal to the product of the current from the current source 9 and a load resistance, which is not shown here. The output voltage U_a changes from a high level U_{amax} to a low level U_{amin} at a switching threshold U_{s2} . The switching threshold U_{s1} is higher than the switching threshold U_{s2} . The switching threshold U_{s1} is determined by the saturation voltage of the transistor 7 and the base-emitter voltage of the transistor 8. The switching threshold U_{s1} complies with the following equation:

$$U_{s1} = U_p - U_{sat7} - U_{be8},$$

where U_p is the voltage on the supply-voltage terminal 50, U_{sat7} is the saturation voltage of the transistor 7 and U_{be8} is the base-emitter voltage of the transistor 8.

The switching threshold U_{s2} is dictated by the base-emitter voltages of the transistors 10 and 11. The switching threshold U_{s2} complies with the following equation:

$$U_{s2} = U_p - U_{be10} - U_{be11},$$

where U_{be10} is the base-emitter voltage of the transistor 10 and U_{be11} is the base-emitter voltage of the transistor 11.

The spacing between the two switching thresholds Us_1 and Us_2 can be increased by means of further transistors arranged as diode elements. These transistors arranged as diode elements must be connected in series with the transistor 10. The position of the switching hysteresis can also be changed by means of further transistors
5 connected as diode elements. The spacing between the two switching thresholds remains the same in this case. The transistors connected as diode elements should be arranged between the junction point between the emitters of the transistors 8 and 10 and the junction point between the base of the transistor 3 and the current source 9.

In the off-state of the transistor 3, when the current mirror 5 should be
10 currentless, crystal defects or temperature changes may give rise to leakage currents from the transistor 7. The output stage of the second current mirror 12 may also produce a leakage current. In comparison with the embodiment shown in Fig. 1, the embodiment shown in Fig. 3 comprises some additional current mirrors, which ensure that the leakage currents are absorbed. The collector of the transistor 2 is connected to
15 an input stage of a third current mirror 14, whose output stage is coupled to a fourth current mirror 15. The input stage of the current mirror 14 comprises a PNP transistor 16 having its emitter connected to the positive power supply terminal and having its base and its collector connected to the collector of the transistor 2. The PNP transistor 17, which constitutes the output stage of the current mirror 14, also has its emitter
20 connected to the positive power supply terminal and its base to the base of the transistor 16. The collector of the transistor 17 constitutes the output of the current mirror 14. This output is connected to the base and the collector of an NPN transistor 18, which constitutes the input stage of the current mirror 15. The emitter of the transistor 18 is connected to the negative power supply terminal. The output stage of the current mirror
25 15 is constituted by an NPN transistor 19 having its collector coupled to the base of the feedback transistor 8 and to the collector of the transistor 7. The emitter is connected to the negative power supply terminal and the base of the transistor 19 is connected to the base of the transistor 18. A leakage current supplied by the collector of the transistor 7 is drained by the transistor 19. In addition, the third and the fourth current mirror
30 provide a higher loop gain and hence steeper edges of the output signal obtained at the switching threshold Us_1 .

A fifth current mirror 21 is arranged between the collector of the transistor 3 and the input stage of the first current mirror 5 and comprises the PNP

transistors 22 and 23. The base of the transistor 22 and the base of the transistor 23 are connected to the collector of the transistor 3 and the collector of the transistor 22. The emitters of the two transistors are connected to the base of the transistor 6. The collector of the transistor 23 is connected to the input stage of a sixth current mirror 24.

- 5 The input stage comprises an NPN transistor 25 which has its emitter connected to the negative power supply terminal and its base and collector to the collector of the transistor 23. The output stage of the sixth current mirror 24 is constituted by an NPN transistor 26 whose collector together with the collector of the transistor 13 constitutes the output. The emitter is also connected to the negative power supply terminal and its
10 base is connected to the base of the transistor 25. The transistor 26 drains the leakage current produced by the collector of the transistor 13 when this transistor should be in a currentless state.

- The current sources 4 and 9 are formed by the output stages of a current-source array 28. The two output stages each comprise an NPN transistor 29 and 30
15 respectively, whose emitters are connected to the negative power supply terminal and whose bases are connected to the base of an NPN transistor 31. The collector of the transistor 29 is connected to the emitters of the transistors 2 and 3 and the collector of the transistor 30 is connected to the base of the transistor 3. The emitter of the transistor 31 is also connected to the negative power supply terminal and the collector
20 of the transistor 31 is connected to the base and to a further current source 32. The other terminal of the current source is connected to the negative power supply terminal.

- In order to prevent the transistor 2 of the differential amplifier 1 from being saturated for high input voltages, a transistor 33 arranged as a diode element is connected to the base of the transistor 2. The input signal U_e is applied to the base and
25 to the collector of the transistor 33, whose emitter is connected to the base of the transistor 2. Consequently, the two switching thresholds $U_{,1}$ and $U_{,2}$ are each shifted by a base-emitter voltage.

- The Schmitt-trigger circuit can also be used in an I^2L circuit. Fig. 4 shows an embodiment suitable for this purpose. This embodiment differs from that
30 shown in Fig. 3 in that the transistor 13 is dispensed with and an injector supplies a base current to the current-source array, which current is generated by a PNP transistor 40 operating in common-base arrangement. The transistor 40 has its collector connected to the base of the transistor 31 and its emitter to the current source 32. The base of the

transistor 40 is connected to earth. The output of the circuit arrangement is constituted by the collector of the transistor 26.

The switching thresholds $Us1$ and $Us2$ in the present embodiment have also changed because further diode-element transistors are arranged between the emitter connection of the transistor 8 and the base connection of the transistor 3 and between the emitter connection of the transistor 8 and the emitter connection of the transistor 10. An NPN transistor 41 has its collector and its base connected to the emitter of the transistor 10 and has its emitter connected to the base and the collector of a further NPN transistor 42. The emitter of the transistor 42 is connected to the emitter of the transistor 8 and to the base and the collector of a further NPN transistor 43. The emitter of the transistor 43 is connected to the base and the collector of an NPN transistor 44, which has its emitter connected to the base of the transistor 3 and to the collector of the transistor 30. The switching threshold $Us1$ satisfies the following equation:

$$Us1 = U_p - U_{sat7} - U_{be8} - U_{be43} - U_{be44} + U_{be33},$$

and the switching threshold $Us2$ complies with the equation:

$$Us2 = U_p - U_{be11} - U_{be10} - U_{be41} - U_{be42} - U_{be43} - U_{be44} + U_{be33}, \text{ where}$$

U_{be33} , U_{be41} , U_{be42} , U_{be43} and U_{be44} are the base-emitter voltages of the transistors 33, 41, 42, 43 and 44.

CLAIMS:

1. A Schmitt-trigger circuit for converting an input signal (Ue) at an input terminal (52) into an output signal (Ua) at an output terminal (53), which circuit comprises a differential amplifier (1) comprising a first transistor (2) and a second transistor (3) each having a base, an emitter and a collector, the emitters of the first and the second transistor (2, 3) being coupled to a first current source (4), the base of the first transistor (2) being coupled to the input terminal and the collector of the second transistor (3) being coupled to an input of a first current mirror (5), and the base of the second transistor (3) being coupled to an output of the first current mirror (5), characterized in that the base of the second transistor (3) is coupled to a second current source (9) and to the output of the first current mirror (5) via a semiconductor junction and to a first diode array which comprises at least two series-arranged diode elements (10, 11) arranged in the forward direction for the current flowing to the second current source and arranged in parallel with the first current mirror (5) and the semiconductor junction.
- 15 2. A circuit as claimed in Claim 1, characterized in that the semiconductor junction is a base-emitter junction of a feedback transistor (8) which has its base coupled to the output of the first current mirror (5) and its emitter to the base of the second transistor.
3. A circuit as claimed in Claim 1 or 2, characterized in that a second diode array (43, 44) is arranged between a first coupling point of the base of the second transistor (3) and the second current source (9), and a second coupling point of the semiconductor junction and the first diode array (10, 11).
- 20 4. A circuit as claimed in Claim 1, 2 or 3, characterized in that the first diode array is arranged in the input current-path of an input stage of a second current mirror (12) having an output stage (13) connected to the output terminal (53).
- 25 5. A circuit as claimed in Claim 2, 3 or 4, characterized in that the collector of the first transistor (2) is connected to an input of a third current mirror (14) which has an output coupled to an input of a fourth current mirror (15) having an output



connected to the base of the feedback transistor (8).

6. A circuit as claimed in Claim 5, characterized in that the input terminal (52) is coupled to the base of the first transistor (2) via an input diode array (33).

7. A circuit as claimed in Claim 1, 2, 3, 5 or 6, characterized in that the
5 input of the first current mirror (5) is preceded by an input stage (22) of a fifth current mirror (21), which has an output stage (23) coupled to an input stage (25) of a sixth current mirror (24) having an output stage (26) connected to the output terminal (53).

8. A circuit as claimed in Claim 7, where appendant to Claim 4,
characterized in that the output stages (13, 26) of the second and the sixth current
10 mirror (12, 24) are interconnected.

9. A circuit as claimed in Claim 8, characterized in that the first and the second current source (4, 9) each form an output stage (29, 30) of a current-source array which is constructed in integrated injection logic technology and which comprises transistors whose bases are connected to a common injector (40, 32).