niobate. Generally, lithium niobate is not compatible with standard CMOS fabrication. Accordingly, in one embodiment, the second part can be a lithium-niobate-on-insulator (LNOI) wafer. The materials other than the lithium niobate that are not compatible with standard CMOS fabrication include but not limited to, III-V materials such as Indium Phosphide or Gallium Arsenide and Nonlinear Crystal Materials such as lithium tantalate or Potassium Dideuterium.

[0061] In one embodiment, there is provided a hybrid silicon photonics modulator comprising a silicon on insulator (SOI) and a lithium-niobate-on-insulator (LNOI), wherein the SOI is bonded to the LNOI to ensure compatibility with lithium-niobate devices or silicon devices via a single transition layer.

[0062] The silicon on insulator (SOI) can represent the first part of the modulator. The silicon on insulator (SOI) can include one or more silicon dioxide (SiO_2) layers, a substrate layer and a waveguide. A silicon (Si) layer can be optionally included. The lithium-niobate-on-insulator (LNOI) can represent the second part of the modulator. The lithium-niobate-on-insulator (LNOI) can include a lithium niobate layer and a silicon dioxide (SiO_2) layer. A silicon (Si) layer can be optionally included.

[0063] In one embodiment, the waveguide can be a silicon (Si) waveguide or silicon nitride (SiN) waveguide.

[0064] Upon integration and bonding of the first and second parts (i.e. SOI and LNOI) the second substrate layer of the second part can be positioned to be in contact with the waveguide, or spaced with a thin layer between the second substrate layer and the waveguide. In one embodiment, the second substrate layer can be positioned adjacent to and above the waveguide.

[0065] To integrate the first and second parts, the top layer of the first part can include one or more etched regions to accommodate the second part such that the second part is enclosed within the first part with only the top surface of the second part being exposed.

[0066] In one embodiment, the one or more etched regions can comprise an etched

CLAIMS

What is claimed is:

1. A hybrid silicon photonics modulator comprising:

a first part comprising a first substrate layer, a first oxide layer, and a waveguide, wherein the first oxide layer comprises one or more etched regions;

a second part comprising a second substrate layer, a second oxide layer and a non-CMOS material layer, wherein the non-CMOS material layer comprises one of a lithium niobate layer, a III-V material, and a nonlinear crystal material; and

at least two electrodes,

wherein one etched region of the one or more etched regions is sized and shaped to accommodate the second part such that the second part is enclosed within the first part with only a top surface of the second substrate layer being exposed, and

wherein the first part is bonded to the second part via the at least two electrodes, the second oxide layer being formed above the non-CMOS material layer, and the at least two electrodes being positioned beneath the non-CMOS material layer relative to an orientation of the second part when placed in the first part,

or the non-CMOS material layer is directly bonded or fused bonded to the first part such that the second oxide layer is formed between the non-CMOS material layer and the at least two electrodes.

2. The modulator of claim 1, wherein the first part is a silicon on insulator (SOI), and the first oxide layer is a silicon dioxide (SiO_2) layer.

3. The modulator of claim 1, wherein the second part is a lithium-niobate-on-insulator (LNOI) and is the second oxide layer is a silicon dioxide (SiO_2) layer.

4. The modulator of claim 1, wherein the waveguide is a silicon (Si) waveguide or silicon nitride (SiN) waveguide.

5. The modulator of claim 1, wherein the non-CMOS material layer is the lithium niobate layer, and the lithium niobate layer is in contact with the waveguide.

6. The modulator of claim 5, wherein the lithium niobate layer is above the waveguide.

7. The modulator of claim 1, wherein the first part is bonded to the second part via the at least two electrodes, the second oxide layer being formed above the non-CMOS material layer, and the at least two electrodes being positioned beneath the non-CMOS material layer relative to the orientation of the second part when placed in the first part.

8. The modulator of claim 1, wherein the non-CMOS material layer is directly bonded or fused bonded to the first part such that the second oxide layer is formed between the non-CMOS material layer and the at least two electrodes.

9. The modulator of claim 2, wherein the one or more etched regions comprise two gaps etched into the silicon dioxide (SiO_2) layer of the SOI, wherein the electrodes form metallic pillars that are lithographically positioned in the two gaps.

10. The modulator of claim 9, wherein the two gaps are separated by the waveguide positioned in between.

11. The modulator of claim 2, wherein the non-CMOS material layer is enclosed within the SOI.

12. The modulator of claim 1, wherein the modulator is operatively connected to a silicon device to form a Multi-Project Wafer (MPW) semiconductor.

13. The modulator of claim 1, wherein the first part comprises one or more etched

regions for bonding with the second part.

14. A lithium-niobate or silicon device integrated with the modulator of claim 1 via a single transition layer.

15. A method for manufacturing a hybrid silicon photonics modulator comprising the steps of:

forming a first part comprising a first substrate layer, a first oxide layer, and a waveguide, wherein the first oxide layer comprises one or more etched regions;

forming a second part comprising a second substrate layer, a second oxide layer and a non-CMOS material layer, wherein the non-CMOS material layer comprises one of a lithium niobate layer, a III-V material, and a nonlinear crystal material; and

forming at least two electrodes,

wherein one etched region of the one or more etched regions is sized and shaped to accommodate the second part such that the second part is enclosed within the first part with only a top surface of the second substrate layer being exposed, and

wherein the first part is bonded to the second part via the at least two electrodes, the second oxide layer being formed above the non-CMOS material layer, and the at least two electrodes being positioned beneath the non-CMOS material layer relative to an orientation of the second part when placed in the first part,

or the non-CMOS material layer is directly bonded or fused bonded to the first part such that the second oxide layer is formed between the non-CMOS material layer and the at least two electrodes.

16. The method of claim 15, wherein the first part is bonded to the second part via the at least two electrodes, the second oxide layer being formed above the non-CMOS material layer, and the at least two electrodes being positioned beneath the non-CMOS material layer relative to the orientation of the second part when placed in the first part.

17. The method of claim 15, wherein the non-CMOS material layer is directly bonded or fused bonded to the first part such that the second oxide layer is formed between the non-CMOS material layer and the at least two electrodes.

18. The method of claim 15, wherein the first part is a Silicon-On-Insulator (SOI) and the second part is a lithium-niobate-on-insulator (LNOI), wherein the non-CMOS material layer is a lithium niobate layer.

19. A computer readable storage medium having stored thereon computer executable instructions that, when executed on a processor in a chip fabrication system, causes the chip fabrication system to perform the steps of the method of claim 15.