Claims

1. A substrate coated with a multi-layer coating, comprising in order:
   i. a substrate,
   ii. a conductive metal seed layer,
   iii. a ta-C containing layer adjacent the seed layer, and
   iv. a DLC containing layer having a thickness of from 1.5µm to 3.5µm,

wherein the coating has a surface electrical resistance of from 10^5 Ω/sq to 10^9 Ω/sq; the ta-C containing layer comprises greater than 90% ta-C by weight; and the DLC containing layer comprises greater than 90% DLC by weight having a hydrogen content of 20% or greater and an sp^2 content of 50% of greater.

2. A coated substrate according to claim 1, wherein the ta-C containing layer has a thickness of from 0.1 µm to 1.0 µm.

3. A coated substrate according to any preceding claim, wherein the ta-C containing layer consists of ta-C.

4. A coated substrate according to any preceding claim, wherein the DLC containing layer consists of DLC.

5. A coated substrate according to any preceding claim, wherein the coating has a surface electrical resistance of from 10^6 Ω/sq to 10^7 Ω/sq.

6. A coated substrate according to any preceding claim, wherein the ta-C containing layer and the DLC containing layer are adjacent.

7. A coated substrate according to any preceding claim, wherein the conductive metal seed layer is a titanium or chromium seed layer.

8. A coated substrate according to any preceding claim, wherein the DLC of the DLC containing layer has a hydrogen content of 30% or greater.

9. A coated substrate according to any preceding claim, wherein the ta-C has a hydrogen content of 5% or less and an sp^2 content of 20% or less.

10. A coated substrate according to any preceding claim, wherein the substrate is made of metal , silicon or glass.

11. A coated substrate according to any preceding claim, wherein the DLC containing layer is deposited by a CVD method.

12. A coated substrate according to any preceding claim, wherein the ta-C containing layer is deposited by a PVD method.

13. A coated substrate according to any preceding claim, wherein the ta-C containing layer is deposited by filtered cathodic vacuum arc.

14. A coated substrate according to any preceding claim, wherein the DLC containing layer is deposited by a PACVD process with the following deposition parameters:

i. a coating temperature of from 100°C to 200°C,
ii. a gas flow of from 50sccm to 200sccm, wherein the gas is selected from CH_4, C_2H_6 or C_2H_2,
iii. a bias voltage of from -50V to -1200V, and
iv. a duty cycle of from 3.2% to 75%.

15. A coated substrate according to any preceding claim, wherein the DLC containing layer is deposited by a PACVD process with the following deposition parameters:

i. a coating temperature of from 110°C to 120°C,
ii. a gas flow of from 80sccm to 120sccm, wherein the gas is C_2H_2,
iii. a bias voltage of from -800V to -1200V, and
iv. a duty cycle of from 3.2% to 20%.

16. A substrate coated with a multi-layer coating according to any one of claims 1 to 4 and 6 to 15, consisting of in order:

i. a substrate,

ii. a seed layer,

iii. a ta-C containing layer, and

iv. a DLC containing layer,

wherein the coating has a surface electrical resistance of from 10^5 Ω/sq to 10^9 Ω/sq.

17. A coated substrate according to any preceding claim, comprising in order:

i. a metal substrate,

ii. a conductive metal seed layer,

iii. a ta-C containing layer having a thickness of from 0.1 µm to 1.0 µm, and

iv. a DLC containing layer having a thickness of from 1.5 µm to 3.5 µm.

18. A method of making a coated substrate according to any preceding claim, comprising coating onto the substrate, in order:

i. a seed layer,

ii. a ta-C containing layer using filtered cathodic vacuum arc deposition adjacent the seed layer, and

iii. a DLC containing layer having a thickness of from 1.5µm to 3.5µm

wherein the coating has a surface electrical resistance of from 10^5 Ω/sq to 10^9 Ω/sq; the ta-C containing layer comprises greater than 90% ta-C; and the DLC containing layer comprises greater than 90% DLC having a hydrogen content of 20% or greater and an sp^2 content of 50% of greater.

19. A method according to claim 18, comprising coating onto the substrate, in order:

i. a seed layer,

ii. a ta-C containing layer deposited by filtered cathodic vacuum arc deposition, and

iii. a DLC containing layer deposited by a PACVD process with the following deposition parameters:

a. a coating temperature of from 100°C to 200°C,

b. a gas flow of from 50sccm to 200sccm, wherein the gas is selected from CH_4, C_2H_6 or C_2H_2,

c. a bias voltage of from -50V to -1200V, and

d. a duty cycle of from 3.2% to 75%,

wherein the coating has a surface electrical resistance of from 10^5 Ω/sq to 10^9 Ω/sq

5