CLAIMS

1. A method to control aging of a system on chip (SOC) comprising one or more devices (D1, D2, D3,…) including semiconductor circuit components and at least one aging controller (AGC) monitoring electrical signals circulating inside the system on chip (SOC), each device having at least one operating mode, the method comprising:

- stressing, by the aging controller (AGC), at least one device (D1, D2, D3,…) of the system on chip (SOC) by varying hardware parameters related to the at least one operating mode of said at least one device (D1, D2, D3,…),

- comparing, by the aging controller (AGC), at least one parameter associated with an electrical signal produced by the at least one device (D1, D2, D3,…) with a reference parameter to determine a difference corresponding to an operating age value of the at least one device (D1, D2, D3,…),

- if the operating age value equals or exceeds a predetermined threshold age value (TA), determining a stress state value (ST),

the method is characterized in that it comprises steps of:

- encoding the stress state value (ST) as a binary value associated with each device (D1, D2, D3,…),

and restricting or disabling one or more functions in the at least one operating mode of the system on chip (SOC) according to an array of values formed by one or more binary values, the array of values forming a binary string representing stress state values (ST) associated with each device (D1, D2, D3,…), the binary string being stored in a secure memory (M) monitored by the aging controller (AGC).

2. The method according to claim 1, characterized in that the aging controller (AGC) comprises an oscillator circuit (ROF1, ROF2, ROF3,…) associated with at least one device (D1, D2, D3,…), generating a signal having a frequency (F_{osc}) that decreases with the device operating time and applied stress, said frequency (F_{osc}) being compared with a reference frequency (F_{ref}) for determining a difference (ΔF) corresponding to an operating age value of the at least one device.

3. The method according to claim 2, characterized in that the oscillator circuit (ROF1, ROF2, ROF3,…) comprises a ring oscillator made up of a chain including an odd number of CMOS inverters (IN_1,…,IN_N) connected in series where the output of the last inverter (IN_N) is fed back as input of the first inverter (IN_1).

4. The method according to claim 2 or 3, characterized in that the oscillator circuit (ROF1, ROF2, ROF3,…) is stressed, during a predetermined time or within time periods, with commands (SI1, SI2, SI3,…) managing hardware parameters variations comprising a DC over-voltage, an AC voltage bias, a current increase in a resistor inducing a higher temperature than a normal operating temperature or a combination thereof.

5. The method according to anyone of claim 2 to 4, characterized in that a value of the reference frequency (F_{ref}) is either initially stored in a non-volatile set up memory of the system on chip (SOC) or provided by a clock signal generated by a reference generator, said generator being placed inside or outside the system on chip (SOC).

6. The method according to anyone of claim 1 to 5, characterized in that the binary string being stored in the secure memory (M) is used to form a unique key to perform cryptographic computations.

7. The method according to claim 1, characterized in that the aging controller (AGC) controls signal timing parameters comprising transition time or propagation time of signals produced by at least one device (D1, D2, D3,…) of the system on chip (SOC), said signal timing parameters increasing with the device operating time and applied stress, said signal timing parameters of a stressed device (D1, D2, D3,…) being compared with a reference signal for determining a difference corresponding to an operating age value of the at least one device (D1, D2, D3,…).

8. A system on chip (SOC) configured to control aging of one or more devices (D1, D2, D3,…) comprising semiconductor circuit components, and at least one aging controller (AGC) configured to monitor electrical signals circulating inside the system on chip (SOC), each device (D1, D2, D3,…) having at least one operating mode, the aging controller (SOC) being further configured to:

stress at least one device (D1, D2, D3,…) of the system on chip (SOC), by varying hardware parameters related to the at least one operating mode of said at least one device (D1, D2, D3,…), compare at least one parameter associated with an electrical signal produced by the at least one device (D1, D2, D3,…) with a reference parameter to determine a difference corresponding to an operating age value of the at least one device (D1, D2, D3,…),

determine a stress state value (ST) if the operating age value equals or exceeds a predetermined threshold age value (TA),

the system on chip (SOC) is characterized in that the aging controller (AGC) is further configured to:

encode the stress state value (ST) as a binary value associated with each device (D1, D2, D3,…), and restrict or disable one or more functions in the at least one operating mode of the system on chip (SOC) according to an array of values formed by one or more binary values, the array of values forming a binary string representing stress state values (ST) associated with each device (D1, D2, D3,…), the binary string being stored in a secure memory (M) monitored by the aging controller (AGC).

9. The system on chip (SOC) according to claim 8, characterized in that the aging controller (AGC) comprises an oscillator circuit (ROF1, ROF2, ROF3,…) associated with at least one device (D1, D2, D3,…) configured to generate a signal having a frequency (F_{osc}) decreasimg with the device operating time and applied stress, the aging controller (AGC) being further configured to compare said frequency (F_{osc}) with a reference frequency (F_{ref}) and to determine a difference (ΔF) corresponding to an operating age value of the at least one device associated with at least one device (D1, D2, D3,…).

10. The system on chip (SOC) according to claim 9, characterized in that the oscillator circuit (ROF1, ROF2, ROF3,…) comprises a ring oscillator made up of a chain including an odd number of CMOS inverters (IN_1,…,IN_N) connected in series where the output of the last inverter (IN_N) is fed back as input of the first inverter (IN_1).

11. The system on chip (SOC) according to claim 9 or 10, characterized in that the stress of the oscillator circuit (ROF1, ROF2, ROF3,…) includes commands (SI1, SI2, SI3,…) acting, during a predetermined time or within time periods, on hardware parameters variations comprising a DC over-voltage, an AC voltage bias, a current increase in a resistor inducing a higher temperature than a normal operating temperature or a combination thereof.

12. The system on chip (SOC) according to anyone of claim 9 to 11, characterized in that a value of the reference frequency (F_{ref}) is initially stored in a non-volatile set up memory of the system on chip (SOC) or provided by a clock signal generated by a reference generator placed inside or outside the system on chip (SOC).

13. The system on chip (SOC) according to anyone of claim 8 to 12, characterized in that the binary string, stored in the secure memory (M) is configured to be used as a unique key to perform cryptographic computations.

14. The system on chip according to claim 8, characterized in that the aging controller (AGC) is configured to control signal timing parameters comprising transition time or propagation time of signals produced by at least one device (D1, D2, D3,…) of the system on chip (SOC), said signal timing parameters increasing with the device operating time and stress applied during a predetermined time or within time periods, the aging controller (AGC) being further configured to compare signal timing parameters of a stressed device (D1, D2, D3,…) with the signal timing parameters of a reference signal and determine a difference corresponding to an operating age value of the at least one device (D1, D2, D3,…).

15. The system on chip according to claim 10, characterized in that the aging controller (AGC) further comprises:

- an input interface configured to receive stressing commands (SI1, SI2, SI3,…) acting on hardware parameters related at least one operating mode of the ring oscillator circuit (ROF1, ROF2, ROF3,…),

- a first comparator (CP1) configured to compare the signal frequency (F_{osc}) with a reference frequency (F_{ref}) and to determine a difference (ΔF) showing a decrease of

the signal frequency (F_{osc}) corresponding to an operating age value of the ring oscillator (ROF1, ROF2, ROF3,…),

- a second comparator (CP2) configured to compare the operating age value with a threshold age value (TA) and to output a stress state value (ST).

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