

CLAIMS

1. A method of fabricating an electronic device comprising:
 - forming, on a substrate, a first access line layer and a first self-selecting memory stack on the first access line layer;
 - etching, in a first etching operation, the first access line layer and the first self-selecting memory stack to form a first set of rows extending in a first direction on the substrate, each row of the first set of rows comprising remaining portions of the first access line layer and the first self-selecting memory stack, wherein the first self-selecting memory stack comprises a first layer of chalcogenide glass for both selection and storage;
 - forming a second access line layer and a second self-selecting memory stack on the first set of rows;
 - etching, in a second etching operation, the second access line layer and the second self-selecting memory stack to form a first set of columns extending in a second direction on the first set of rows, each column of the first set of columns comprising remaining portions of the second access line layer and the second self-selecting memory stack, wherein the second self-selecting memory stack comprises a second layer of chalcogenide glass for both selection and storage; and
 - etching, in the second etching operation, portions of the self-selecting memory stack included in the first set of rows that is located between adjacent columns of the first set of columns to form a first set of memory cells, wherein the remaining portions of the first access line layer are not etched during the second etching operation.
2. The method of claim 1, further comprising:
 - forming a third access line layer on the first set of columns;
 - etching, in a third etching operation, the third access line layer to form a second set of rows extending in the first direction on the first set of columns, each row of the second set of rows comprising the third access line layer; and
 - etching, in the third etching operation, portions of the first set of columns located between adjacent rows of the second set of rows to form a second set of memory cells.
3. The method of claim 1, further comprising:
 - forming a third access line layer and a third self-selecting memory stack on the first set of columns;

etching, in a third etching operation, the third access line layer and the third self-selecting memory stack to form a second set of rows extending in the first direction on the first set of columns, each row of the second set of rows comprising the third electrode layer and the third self-selecting memory stack; and

etching, in the third etching operation, portions of the second set of rows located above adjacent columns of the first set of columns to form a second set of memory cells.

4. The method of claim 3, further comprising:

forming a fourth access line layer on the second set of rows;

etching, in a fourth etching operation, the fourth access line layer to form a second set of columns extending in the second direction on the second set of rows, each column of the second set of columns comprising the fourth electrode layer; and

etching, in the fourth etching operation, portions of the second set of rows located above adjacent columns of the second set of columns to form a third set of memory cells.

5. The method of claim 1, wherein each self-selecting memory stack comprises a first layer of barrier material below and in contact with a layer of chalcogenide glass and a second layer of barrier material above and in contact with the layer of chalcogenide glass.

6. The method of claim 5, wherein the second etching operation comprises:

etching through the second self-selecting memory stack and through a portion of the first self-selecting memory stack below and between adjacent columns of the first set of columns;

detecting the first layer of barrier material in contact with a first layer of chalcogenide glass has been reached in the second etching operation, the first self-selecting memory stack comprising the first layer of chalcogenide glass; and

stopping the second etching operation.

7. The method of claim 5, wherein the second etching operation comprises:

etching through the second self-selecting memory stack and through a portion of the first self-selecting memory stack below and between adjacent columns of the first set of columns;

detecting the second layer of barrier material in contact with a first layer of chalcogenide glass has been reached in the second etching operation, the first self-selecting memory stack comprising the first layer of chalcogenide glass; and
stopping the second etching operation.

8. The method of claim 1, wherein a width of each column of the first set of columns is a same width as a width of each respective memory element located under each column of the first set of columns.

9. The method of claim 8, wherein the width of each column is a same width as the width of each row.

10. The method of claim 8, wherein the width of each column is a different width as the width of each row.

11. The method of claim 1, wherein the second access line layer forms an upper access line for a column of memory cells of the first set of memory cells that are located under each column of the first set of columns, and forms a lower access line for a second column of a second set of memory cells formed using the second self-selecting memory stack.

12. The method of claim 11, wherein a second access line is formed in a single deposition process and is etched in a single etching process as part of the second etching operation.

13. The method of claim 1, wherein the first etching operation exposes a sidewall of the first self-selecting memory stack and the second etching operation exposes a sidewall of the second self-selecting memory stack, the method further comprising:

forming a first sealing layer in contact with the sidewall of the first self-selecting memory stack, the first sealing layer configured to maintain a chemical composition of the first layer of chalcogenide glass; and

forming a second sealing layer in contact with the sidewall of the second self-selecting memory stack, the second sealing layer configured to maintain a chemical composition of the second layer of chalcogenide glass.

14. The method of claim 13, further comprising:
 depositing, after forming the first sealing layer, a dielectric material between rows of the first set of rows; and
 depositing, after forming the second sealing layer, the dielectric material between columns of the first set of columns.

15. The method of claim 14, further comprising:
 forming the first sealing layer and the second sealing layer at a first temperature; and
 depositing the dielectric material at a second temperature that is greater than the first temperature.

16. A memory device, comprising:
 a first array of memory cells that each comprise a first self-selecting memory element, the first array of memory cells having a first plurality of columns extending in a first direction and a first plurality of rows extending in a second direction, wherein a first memory cell of the first array of memory cells is coupled with a first access line and a second access line and comprises a first layer of chalcogenide glass for both selection and storage; and
 a second array of memory cells that each comprise a second self-selecting memory element, the second array of memory cells having a second plurality of columns extending in the first direction and a second plurality of rows extending in the second direction, wherein the second array overlies the first array, and wherein a second memory cell of the second array of memory cells is coupled with the second access line and a third access line, and wherein the first access line is formed during a first etching operation and the second access line and the first array of memory cells are formed during a second etching operation, and wherein the second array of memory cells comprises a second layer of chalcogenide glass for both selection and storage.

17. The memory device of claim 16~~17~~, further comprising:
 a first plurality of access lines comprising the first access line coupled with a lower portion of each memory cell of each row of the first plurality of rows;

a second plurality of access lines comprising the second access line coupled with an upper portion of each memory cell of each column of the first plurality of columns and coupled with a lower portion of each memory cell of each column of the second plurality of columns; and

a third plurality of access lines comprising the third access line coupled with an upper portion of each memory cell of each row of the second plurality of rows.

18. The memory device of claim 17, wherein the first plurality of columns, the second plurality of access lines, and the second plurality of columns are self-aligned.

19. The memory device of claim 17, wherein the first plurality of columns, the second plurality of access lines, and the second plurality of columns have a same patterning registration and a same width.

20. The memory device of claim 17, wherein the second plurality of access lines comprise a metal material with an absence of an intra-layer boundary.

21. The memory device of claim 16, wherein the first self-selecting memory element comprises a first layer of chalcogenide glass for both selection and storage and the second self-selecting memory element comprises a second layer of chalcogenide glass for both selection and storage.

22. The memory device of claim 21, further comprising:
a first sealing layer in contact with a sidewall of the first self-selecting memory element, the first sealing layer configured to maintain a chemical composition of the first layer of chalcogenide glass; and

a second sealing layer in contact with a sidewall of the second self-selecting memory element, the second sealing layer configured to maintain a chemical composition of the first layer of chalcogenide glass.

23. The memory device of claim 22, further comprising:
a dielectric material deposited adjacent to the first sealing layers; and
the dielectric material deposited adjacent to the second sealing layers.

24. A memory device, comprising:

a plurality of pillars arranged in a three-dimensional cross-point architecture with a first access line extending in a first direction, a second access line extending in a second direction, and a third access line extending in the first direction, each pillar comprising:

a first memory storage element coupled to the first access line and the second access line, wherein the first access line is formed during a first etching operation, and wherein the first access line comprises remaining portions of the first access line and a first self-selecting memory stack; and

a second memory storage element coupled to the second access line and the third access line, wherein the second access line and the first memory storage element are formed during a second etching operation, and wherein the remaining portions of the first access line layer are not etched during the second etching operation.

25. The memory device of claim 24, wherein the second memory storage element has a second width in a second direction substantially orthogonal to the first direction, the second width different from the width of the respective pillar in the first direction.

26. The memory device of claim 24, wherein each of the first memory storage element and the second memory storage element comprise a self-selecting memory storage element.

27. The memory device of claim 24, wherein the first memory storage element and the second memory storage element each comprise a chalcogenide glass.

28. The memory device of claim 24, wherein the first memory storage element comprises a first deck of a three-dimensional cross point memory architecture and the second memory storage element comprises a second deck of the three-dimensional cross point memory architecture.

29. The memory device of claim 24, wherein the second access line comprises a metal material with an absence of an intra-layer boundary.