DUAL STRESS MEMORY TECHNIQUE METHOD

AND RELATED STRUCTURE


ABSTRACT OF THE DISCLOSURE

A method for providing a dual stress memory technique in a semiconductor device including an nFET and a PFET and a related structure are disclosed. One embodiment of the method includes forming a tensile stress layer over the nFET and a compressive stress layer over the pFET, annealing to memorize stress in the semiconductor device and removing the stress layers. The compressive stress layer may include a high stress silicon nitride deposited using a high density plasma (HDP) deposition method. The annealing step may include using a temperature of approximately 400-1200 °C. The high stress compressive silicon nitride and/or the anneal temperatures ensure that the compressive stress memorization is retained in the pFET.


**Figure 6**