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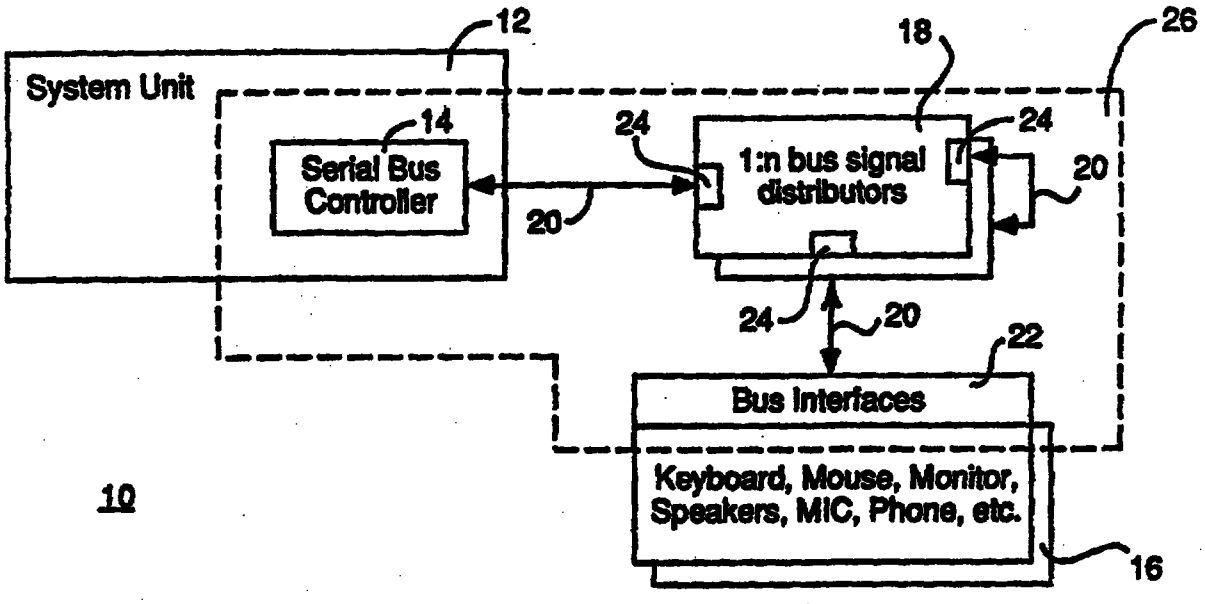
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(57) Abstract

A bus controller (14), a number of 1:n bus signal distributors (18), and a number of bus interfaces (22) are provided to form a hierarchical serial bus assembly (26) for serially interfacing a number of isochronous and asynchronous peripherals (16) to the system unit of a computer system. The bus controller (14), bus signal distributors (18), and bus interfaces (22) are provided with circuitry and complementary logic (16c) for implementing a master/slave model of low control for serially interfacing the bus agents to each other to conduct data communication transactions. In certain embodiments, these circuitry and complementary logic (16c) further conduct connection management transactions employing also the master/slave model of flow control, implement a frame based polling schedule for polling the slave "devices", employ at least two address spaces to conduct the various transactions, support communication packet based transactions, and/or electrically represent data and/or control states.