# PASSIVATING POINT DEFECTS IN HIGH-K GATE DIELECTRIC LAYERS DURING GATE STACK FORMATION

## ABSTRACT OF THE DISCLOSURE

Generally, the present disclosure is directed to techniques for improving the reliability of semiconductor devices with high-k gate dielectric layers by passivating point defects during the gate stack formation. One illustrative method disclosed herein includes performing a plurality of material deposition cycles to form a high-k dielectric layer above a semiconductor material layer, and introducing a passivating material into a gaseous precursor that is used for forming the high-k dielectric layer during at least one of the plurality of material deposition cycles.

Figure 2d