WHAT IS CLAIMED:

1. A method, comprising:

forming a first stress-inducing layer (230) above a first transistor (220B) formed above a substrate (201), said first stress-inducing layer (230) generating a first type of stress;

forming a second stress-inducing layer (240) above a second transistor (220A), said second stress-inducing layer (240) generating a second type of stress other than said first type of stress;

forming a third dielectric layer (260) above said first and second transistors (220B, 220A), said third dielectric layer (260) having an internal stress level above said second transistor (220A) that is less than that of said first and second stress-inducing layers (240, 230);

forming an interlayer dielectric material (250) above said first and second transistors (220B, 220A); and

forming contact openings (251) connecting to said first and second transistors (220B, 220A) by using said first and second stress-inducing layers (230, 240) and said third dielectric (260) layer as an etch stop material.

2. A method, comprising:

forming a first dielectric layer (230) above a first transistor (220B), said first dielectric layer (230) inducing a compressive strain in a channel region (224) of said first transistor (220B), wherein said first transistor comprises a P-channel transistor;

forming a second dielectric layer (240) above a second transistor (220A), said second dielectric layer (240) inducing a tensile strain in a channel region (224) of said second transistor (220A), wherein said second transistor comprises an N-channel transistor;

forming a third dielectric layer (260) above said first transistor (220B) and said second transistor (220A), said third dielectric layer (260) having an internal stress level that is less than an internal stress level of said first and second dielectric layers (230, 240); and

depositing an interlayer dielectric (250) material above said third dielectric layer (260).

3. The method of claim 1 or 2, wherein a thickness of said third dielectric layer (260) is approximately 100 nm and less.

4. The method of claim 1 or 2, wherein an internal stress level of the third dielectric layer (260) above said second transistor (220A) is substantially equal to said internal stress level above said first transistor (220B).

5. The method of claim 1 or 2, wherein forming said third dielectric layer (260) comprises depositing material of said third dielectric layer (260) above said first and second transistors (220B, 220A) and treating at least a portion of the deposited material to adjust said internal stress level.

6. The method of claim 5, wherein treating the portion of the deposited material comprises selectively adjusting said internal stress level above said second transistor (220A) without substantially adjusting said internal stress level above said first transistor (220B).

7. The method of claim 5, wherein treating the portion of the deposited material comprises performing an ion implantation process.

8. The method of claim 5, wherein treating the portion of the deposited material comprises performing at least one of a thermal process and a plasma process.

9. The method of claim 1 or 2, wherein said internal stress level of said third dielectric layer (260) is substantially neutral.

10. A semiconductor device (200), comprising:

a first dielectric layer (230) formed above a first transistor (220B), said first dielectric layer (230) inducing a first type of stress;

a second dielectric layer (240) formed above a second transistor (220A), said second dielectric layer (240) inducing a second type of stress other than said first type;

a third dielectric layer (260) formed on said first and second dielectric layers (230, 240), said third dielectric layer (260) having an internal stress level that is less than an internal stress level of said first and second dielectric layers (230, 240); and

an interlayer dielectric material (250) formed above said third dielectric layer (260), said interlayer dielectric material (250) having a thickness that is greater than a combined thickness of said first and third dielectric layers (230, 260).

CLAIMS

1. A method, comprising:

forming a first stress-inducing layer above a first transistor formed above a substrate, said first stress-inducing layer generating a first type of stress;

forming a second stress-inducing layer above a second transistor, said second stress-inducing layer generating a second type of stress other than said first type of stress;

forming a third dielectric layer above said first and second transistors and in direct contact with said first and second stress-inducing layers, said third dielectric layer having an internal stress level above said first transistor that is less than that of said first and second stress-inducing layers;

forming an interlayer dielectric material above said first and second transistors; and

forming contact openings in said interlayer dielectric material by using said third dielectric layer as an etch stop material for the etching of said interlayer dielectric material.

2. The method of claim 1, wherein said internal stress level of said third dielectric layer is substantially neutral.

3. The method of claim 1, wherein said third dielectric layer is comprised of silicon nitride.

4. The method of claim 1, wherein said third dielectric layer comprises silicon and carbon.

5. The method of claim 1, wherein an internal stress level of the third dielectric layer above said second transistor is substantially equal to said internal stress level above said first transistor.

6. The method of claim 1, wherein forming said third dielectric layer comprises depositing material of said third dielectric layer above said first and second transistors and treating the deposited material to adjust said internal stress level.

7. The method of claim 6, wherein said treatment is performed to selectively adjust said internal stress level above said first transistor.

8. The method of claim 6, wherein said treatment is performed commonly for said first and second transistors.

9. The method of claim 6, wherein said treatment comprises performing an ion implantation process.

10. The method of claim 6, wherein said treatment comprises performing at least one of a thermal process and a plasma process.

11. The method of claim 1, wherein said first and second stress-inducing layers comprise silicon and nitrogen.

12. The method of claim 1, wherein at least one of said first and second stress-inducing layers comprises silicon and carbon.

13. The method of claim 1, wherein said first transistor represents an N channel transistor.

14. The method of claim 1, wherein a thickness of said third dielectric layer is approximately 100 nm and less.

15. A method, comprising:

forming a first dielectric layer above a P-channel transistor, said first dielectric layer inducing a compressive strain in a channel region of said P-channel transistor;

forming a second dielectric layer above an N-channel transistor, said second dielectric layer inducing a tensile strain in a channel region of said N-channel transistor;

forming a third dielectric layer above said P-channel transistor and said N-channel transistor and in direct contact with said first and second dielectric layers,

said third dielectric layer having an internal stress level that is less than an internal stress level of said first and second dielectric layers;

depositing an interlayer dielectric material above said third dielectric layer; and

forming contact openings in said interlayer dielectric material by using said third dielectric layer as an etch stop material for the etching of said interlayer dielectric material.

16. The method of claim 15, wherein said third dielectric layer comprises silicon and nitrogen.

17. The method of claim 15, wherein forming said third dielectric layer comprises conformally depositing material of said third dielectric layer and adjusting said internal stress level by treating said material by performing at least one of an ion implantation process, a thermal treatment and a plasma treatment.

18. The method of claim 15, wherein said internal stress level of said third dielectric layer is substantially neutral.

19. A semiconductor device, comprising:

a first dielectric layer formed above a first transistor, said first dielectric layer inducing a first type of stress;

a second dielectric layer formed above a second transistor, said second dielectric layer inducing a second type of stress other than said first type;

a third dielectric layer formed in direct contact with said first and second dielectric layers, said third dielectric layer having an internal stress level that is less than an internal stress level of said first and second dielectric layers; and

an interlayer dielectric material formed above said third dielectric layer, said interlayer dielectric material having a thickness that is greater than a combined thickness of said first and third dielectric layers.

20. The semiconductor device of claim 19, wherein said third dielectric layer is comprised of silicon nitride.

21. The semiconductor device of claim 19, wherein said first and second transistors have a gate length of approximately 50 nm or less.

22. The semiconductor device of claim 19, wherein said first and second dielectric layers contain silicon and nitrogen.

23. The semiconductor device of claim 19, wherein a combined thickness of said first and third dielectric layers is approximately 200 nm or less.

24. A semiconductor device of any of the claims 19-23, formed by a method in accordance with any of the claims 1-18.

25. A semiconductor device formed by a method in accordance with any of the claims 1-18.