CLAIMS

1. A method for testing a semiconductor wafer, including individual semiconductor devices located on the semiconductor wafer, using temporary counterpart sacrificial bond pads, the method comprising:

arranging the individual semiconductor devices on the semiconductor wafer in a configuration having horizontal rows of the individual semiconductor devices with a functional horizontal scribe lane between each set of two horizontal rows of the individual semiconductor devices, and having vertical columns of the individual semiconductor devices with a functional vertical scribe lane between each set of two vertical columns of the individual semiconductor devices, wherein the individual semiconductor devices include normal individual bond pads along a perimeter of each individual semiconductor device;

determining which of the normal individual bond pads on the individual semiconductor devices are critical to a semiconductor wafer testing probe process based on a determination that critical bond pads are more frequently damaged by the semiconductor wafer testing probe process;

providing temporary counterpart sacrificial bond pads only for the normal individual bond pads on the individual semiconductor devices determined to be critical bond pads;

electrically testing a portion of the individual semiconductor devices using a semiconductor wafer tester executing the semiconductor wafer testing probe process, the semiconductor wafer tester using a semiconductor wafer probe that makes physical contact with the temporary counterpart sacrificial bond pads; and

destroying the temporary counterpart sacrificial bond pads upon completion of the electrical testing when the individual semiconductor devices are cut from the semiconductor wafer.

2. The method for testing a semiconductor wafer according to claim 1,

wherein normal individual bond pads designed for individual semiconductor device testing are designated as critical to the semiconductor wafer testing probe process.

3. The method for testing a semiconductor wafer according to claim 1,

wherein normal individual bond pads designed for supplying electrical power and providing electrical grounding are designated as critical to the semiconductor wafer testing probe process.

4 A method for testing a semiconductor wafer, including individual semiconductor devices located on the semiconductor wafer, using temporary counterpart sacrificial bond pads, the method comprising:

arranging the individual semiconductor devices on the semiconductor wafer in a configuration having horizontal rows of the individual semiconductor devices with a functional horizontal scribe lane between each set of two horizontal rows of the individual semiconductor devices, and having vertical columns of the individual semiconductor devices with a functional vertical scribe lane between each set of two vertical columns of the individual semiconductor devices, wherein the individual semiconductor devices include normal individual bond pads along a perimeter of each individual semiconductor device;

creating temporary counterpart sacrificial bond pads, including a temporary counterpart sacrificial bond pad located in the functional horizontal scribe lane and a temporary counterpart sacrificial bond pad located in the functional horizontal scribe lane, each temporary counterpart sacrificial bond pad being electrically connected to a corresponding one of the normal individual bond pads on the individual semiconductor devices;

electrically testing a portion of the individual semiconductor devices using a semiconductor wafer tester executing a semiconductor wafer testing probe process, the semiconductor wafer tester making physical contact with the temporary counterpart sacrificial bond pad; and

destroying the temporary counterpart sacrificial bond pads upon completion of the electrical testing when the individual semiconductor devices are cut from the semiconductor wafer;

wherein the temporary counterpart sacrificial bond pads include at least one temporary counterpart sacrificial bond pad that is larger in size than the other temporary counterpart sacrificial bond pads to accommodate multiple semiconductor probe card contacts for providing higher electrical power delivery to a single normal bond pad of one of the individual semiconductor devices.

5. The method for testing a semiconductor wafer according to claim 4,

wherein the temporary counterpart sacrificial bond pads are smaller in size than the normal individual bond pad located on the individual semiconductor devices.

6. The method for testing a semiconductor wafer according to claim 4,

wherein the temporary counterpart sacrificial bond pads are have a size that is approximately 50% of that of the normal individual bond pad located on the individual semiconductor devices.

7. The method for testing a semiconductor wafer according to claim 4,

wherein the temporary counterpart sacrificial bond pads have a size that is approximately 25% of that of the normal individual bond pads located on the individual semiconductor devices.

8. The method for testing a semiconductor wafer according to claim 4,

wherein the temporary counterpart sacrificial bond pads for adjacent ones of the individual semiconductor devices are offset from one another, so that the temporary counterpart sacrificial bond pads for adjacent ones of the individual bond pads are not located back-to-back.

9. The method for testing a semiconductor wafer according to claim 4,

wherein the temporary counterpart sacrificial bond pads for adjacent ones of the individual semiconductor devices are located back-to-back.

10. The method for testing a semiconductor wafer according to claim 4, further comprising:

providing the temporary counterpart sacrificial bond pads for all of the normal individual bond pads on the individual semiconductor devices.

11. The method for testing a semiconductor wafer according to claim 4,

wherein designated functional horizontal scribe lanes and designated functional vertical scribe lanes are configured to have a sufficient width to accommodate the temporary counterpart sacrificial bond pads that are located back-to-back with a non-conductive separation therebetween.

12. The method for testing a semiconductor wafer according to claim 4,

wherein each temporary counterpart sacrificial bond pad is electrically connected to the corresponding normal individual bond pad located on one of the individual semiconductor devices through the use of a re-distribution layer, which is a conductive layer provided over a semiconductor wafer surface and is otherwise electrically isolated from the individual semiconductor device.

13. The method for testing a semiconductor wafer according to claim 4, further comprising:

staggering a location on the temporary counterpart sacrificial bond pad of a plurality of physical contacts between the semiconductor wafer tester and the temporary counterpart sacrificial bond pad such that each physical contact is at a different location on the temporary counterpart sacrificial bond pad.

14. The method for testing a semiconductor wafer according to claim 4,

wherein the temporary counterpart sacrificial bond pads are smaller in size than the normal individual bond pads on the individual semiconductor devices, and the temporary counterpart sacrificial bond pads, located in a vertical and/or horizontal scribe lane between adjacent ones of the individual semiconductor devices, are arranged in a side-by-side configuration.

15. A semiconductor wafer configured with temporary counterpart sacrificial bond pads for testing individual semiconductor devices on the semiconductor wafer, the semiconductor wafer comprising:

individual semiconductor devices arranged on the semiconductor wafer in a configuration having horizontal rows of the individual semiconductor devices with a functional horizontal scribe lane between each set of two horizontal rows of the individual semiconductor devices, and having vertical columns of individual semiconductor devices with a functional vertical scribe lane between each set of two vertical columns of the individual semiconductor devices, wherein the individual semiconductor devices include normal individual bond pads along a perimeter of each individual semiconductor device; and

temporary counterpart sacrificial bond pads, located in one or more of the functional horizontal scribe lanes and/or one or more of the functional vertical scribe lanes, that are each electrically connected to a corresponding one of the normal individual bond pad located on an individual semiconductor device, each temporary counterpart sacrificial bond pad being used for testing the corresponding individual semiconductor device located on the corresponding semiconductor wafer only before the individual semiconductor device is physically separated from the semiconductor wafer,

wherein the temporary counterpart sacrificial bond pads are smaller in size than the normal individual bond pads located on the individual semiconductor devices,

wherein the temporary counterpart sacrificial bond pads for adjacent ones of the individual semiconductor devices are offset from one another, so that the temporary counterpart sacrificial bond pads for adjacent ones of the individual bond pads are located

side-by-side, and not located back-to-back in the vertical scribe lane or the horizontal scribe lane, and

wherein the temporary counterpart sacrificial bond pads include at least one temporary counterpart sacrificial bond pad that is larger in size than the other temporary counterpart sacrificial bond pads to accommodate multiple semiconductor probe card contacts for providing higher electrical power delivery to a single normal bond pad of one of the individual semiconductor devices.

16. The semiconductor wafer according to claim 15,

wherein each temporary counterpart sacrificial bond pad is electrically connected to the corresponding normal individual bond pad located on one of the individual semiconductor devices through the use of a re-distribution layer, which is a conductive layer provided over a semiconductor wafer surface and is otherwise electrically isolated from the individual semiconductor device.

17. The method for testing a semiconductor wafer according to claim 15,

wherein the temporary counterpart sacrificial bond pads have a size that is approximately 25% of that of the normal individual bond pads located on the individual semiconductor device.