

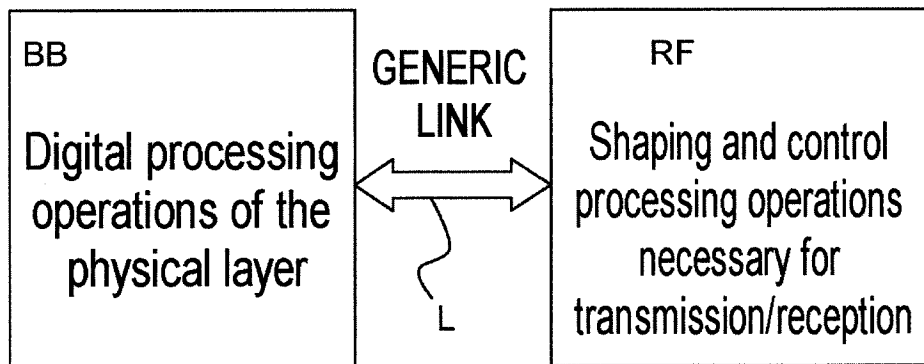


FIG.1

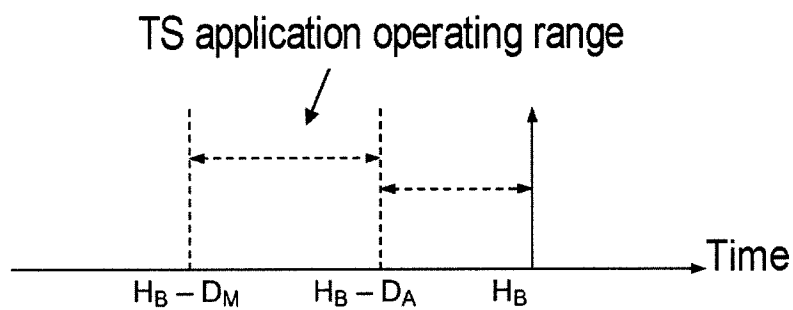


FIG.4

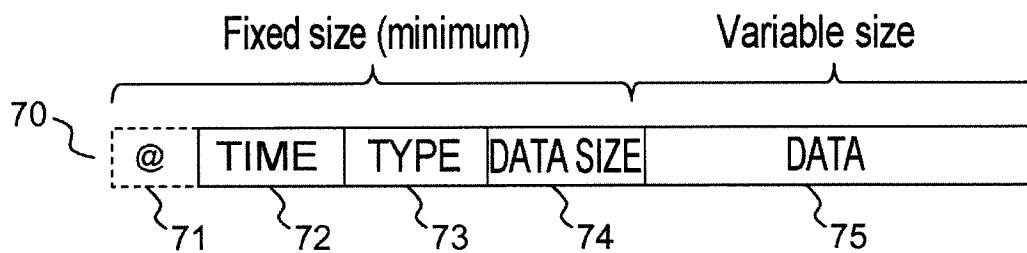


FIG.7

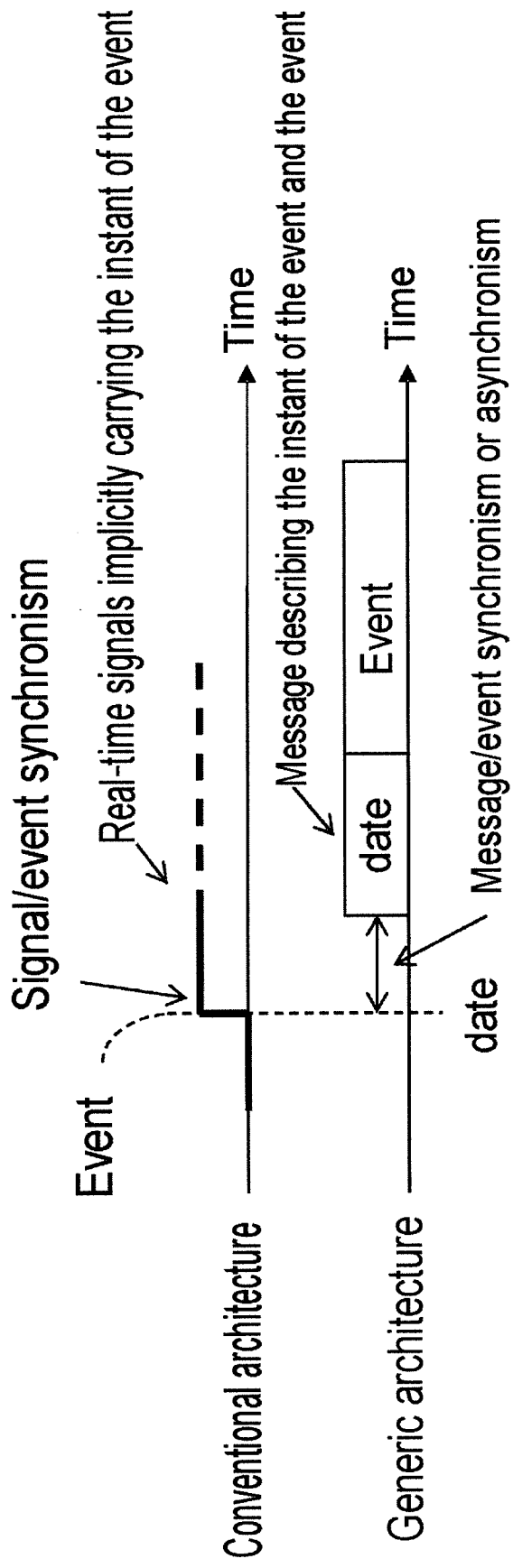


FIG.2

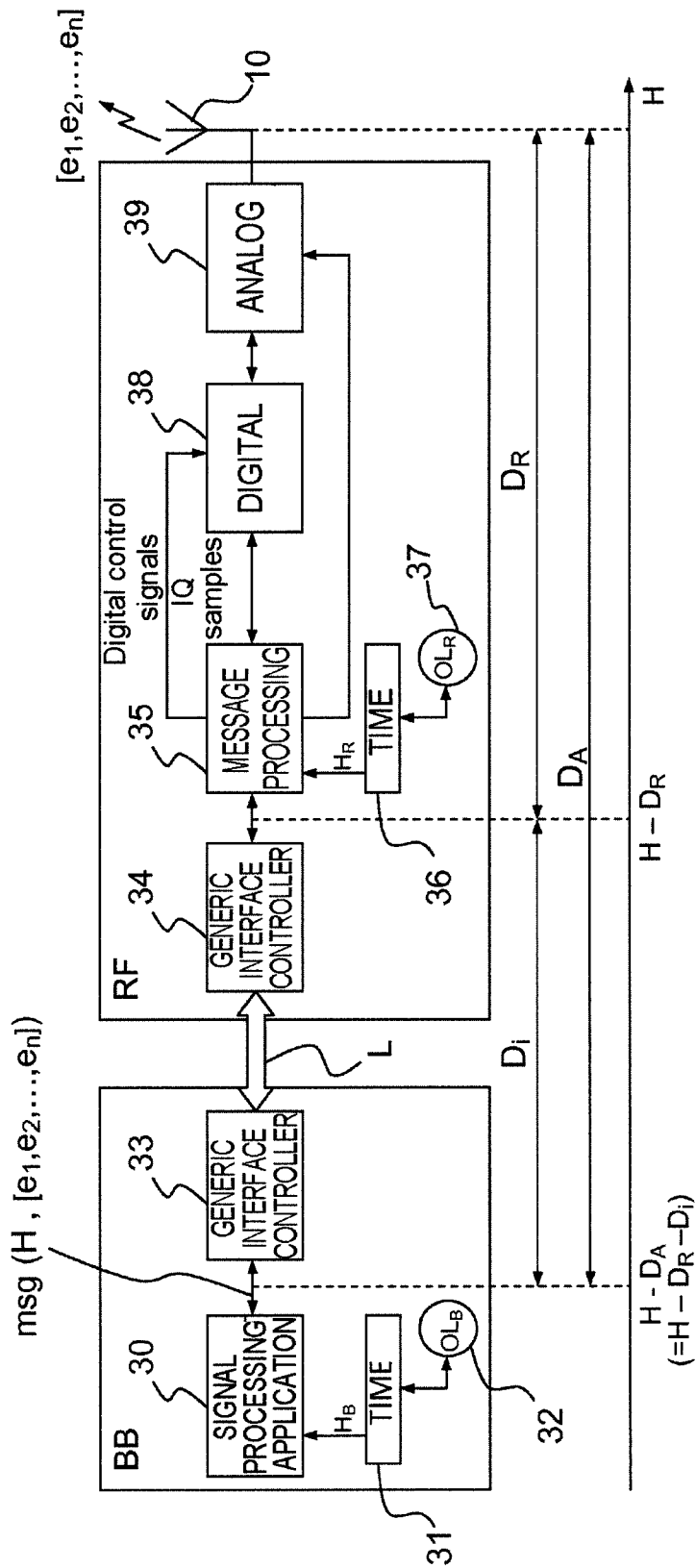


FIG.3

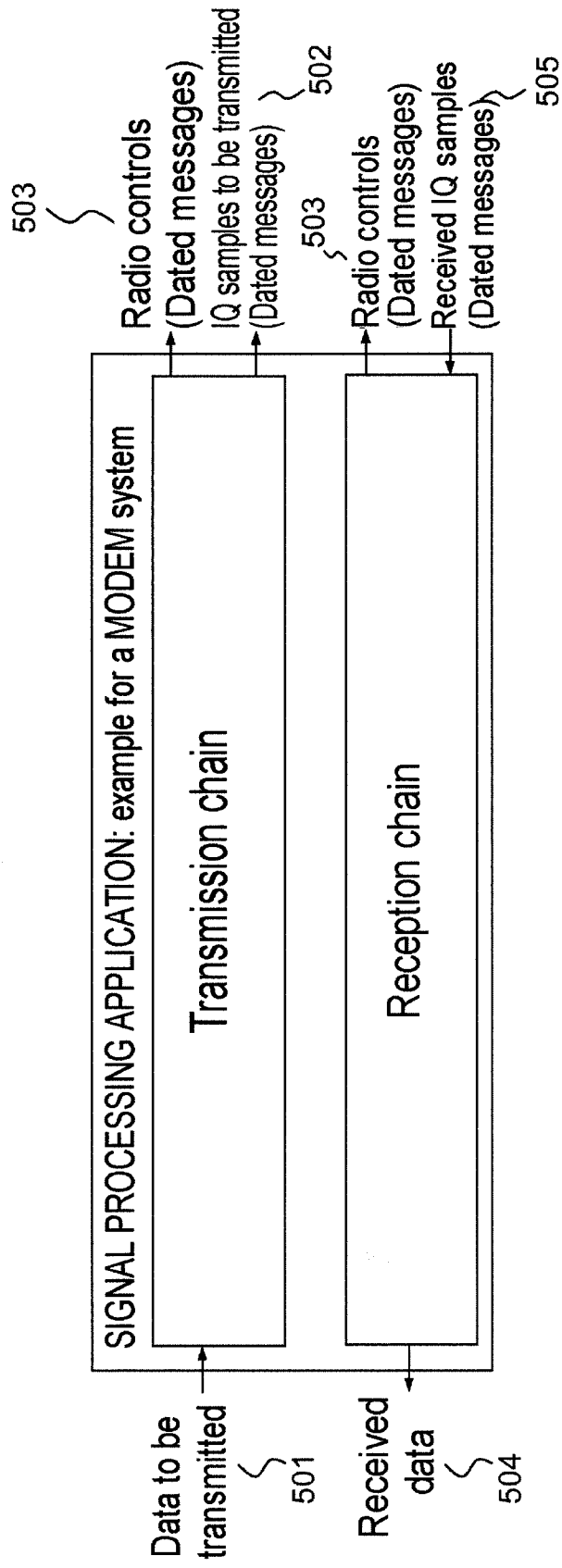


FIG.5

Tx/Rx passage time identical for each controller

The diagram shows a timeline with two main sections: BB (Baseband) and RF (Radio Frequency). Two Generic Interface Controllers, labeled 33 and 34, are connected by a bidirectional arrow. The timeline starts at t_0 with a 'MSG (request $[\pi]$)' signal. This signal is received by controller 33 and then by controller 34. The signal then returns from controller 34 to controller 33, and finally back to the RF section. The timeline ends at $t_0 + t_1$. A second timeline segment is shown below, starting at $t_2 = t_0 + 2 \cdot t_1 + \tau$ and ending at $t_0 + t_1 + \tau$, with a 'MSG (π)' signal. The total duration is labeled $D_i = [(t_0 - t_2) / 2] - \tau$.

The diagram illustrates a system architecture divided into two main functional blocks: BB (Baseband) and RF (Radio Frequency).
 - In the BB block, a 'GENERIC INTERFACE CONTROLLER' is connected to a 'TIME' block. The 'TIME' block outputs a signal H_B to the controller. The controller outputs a signal H_B to the RF block. A feedback loop labeled OL_B returns from the output of the BB block to the 'TIME' block.
 - In the RF block, another 'GENERIC INTERFACE CONTROLLER' is connected to a 'TIME' block. The BB controller outputs a signal $H_B + D_i$ to this controller. The controller outputs a signal H_R to the 'TIME' block. A feedback loop labeled OL_R returns from the output of the RF block to the 'TIME' block.
 - A central message path, labeled 'MSG (time[$H_B + D_i$])', connects the two controllers.
 - At the bottom, two dashed vertical lines mark the boundaries of the BB and RF sections, with labels H_B and $H_B + D_i$ respectively.

FIG.9

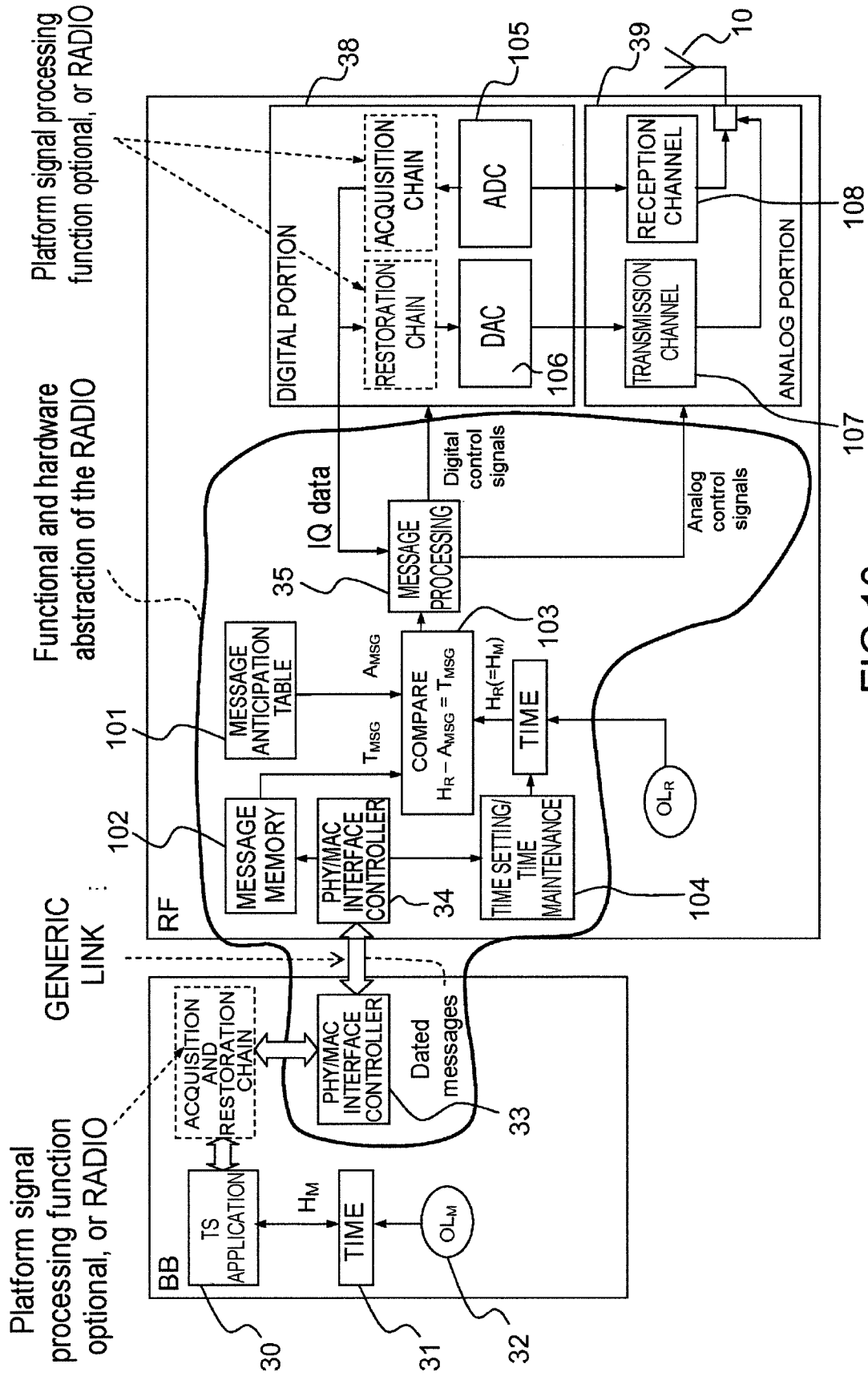


FIG.10

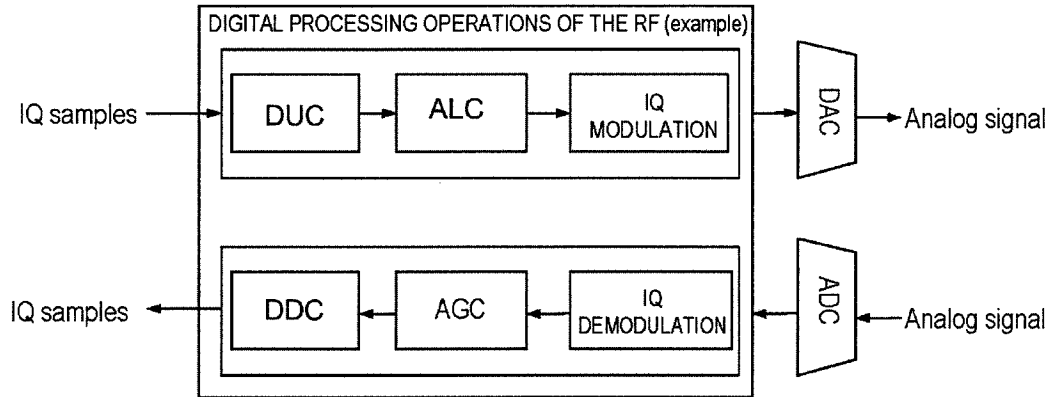


FIG.11

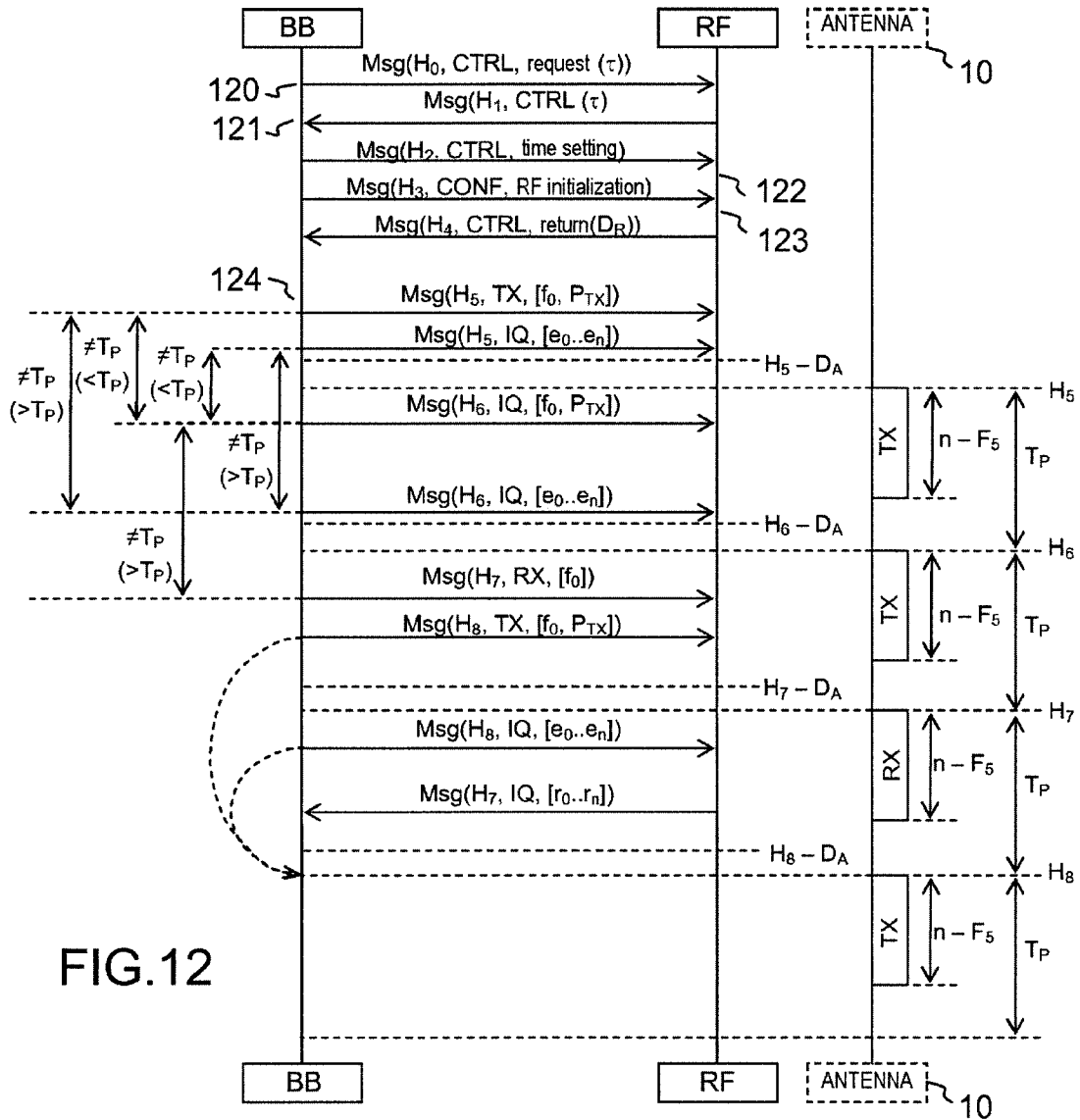


FIG.12

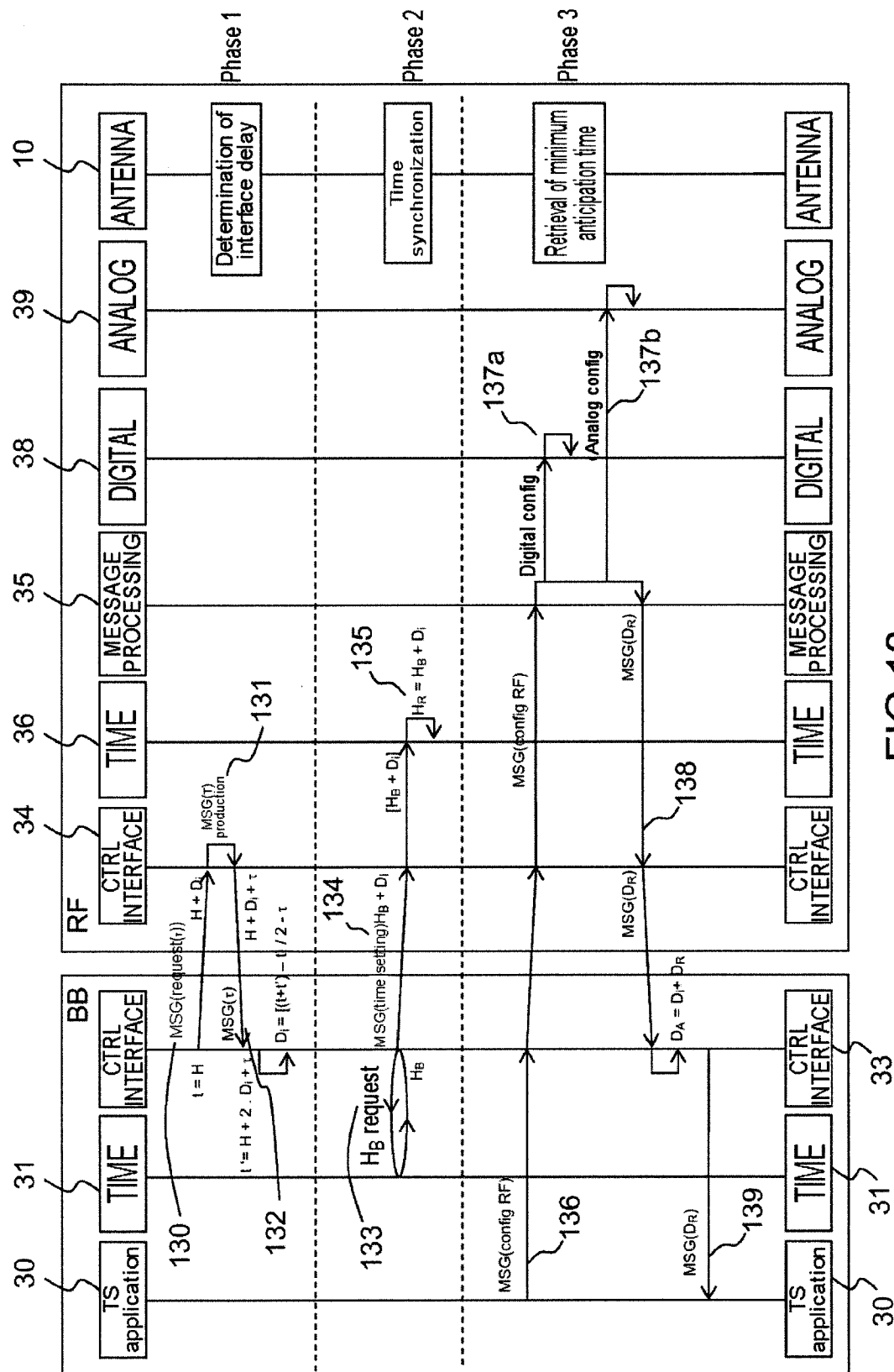


FIG.13

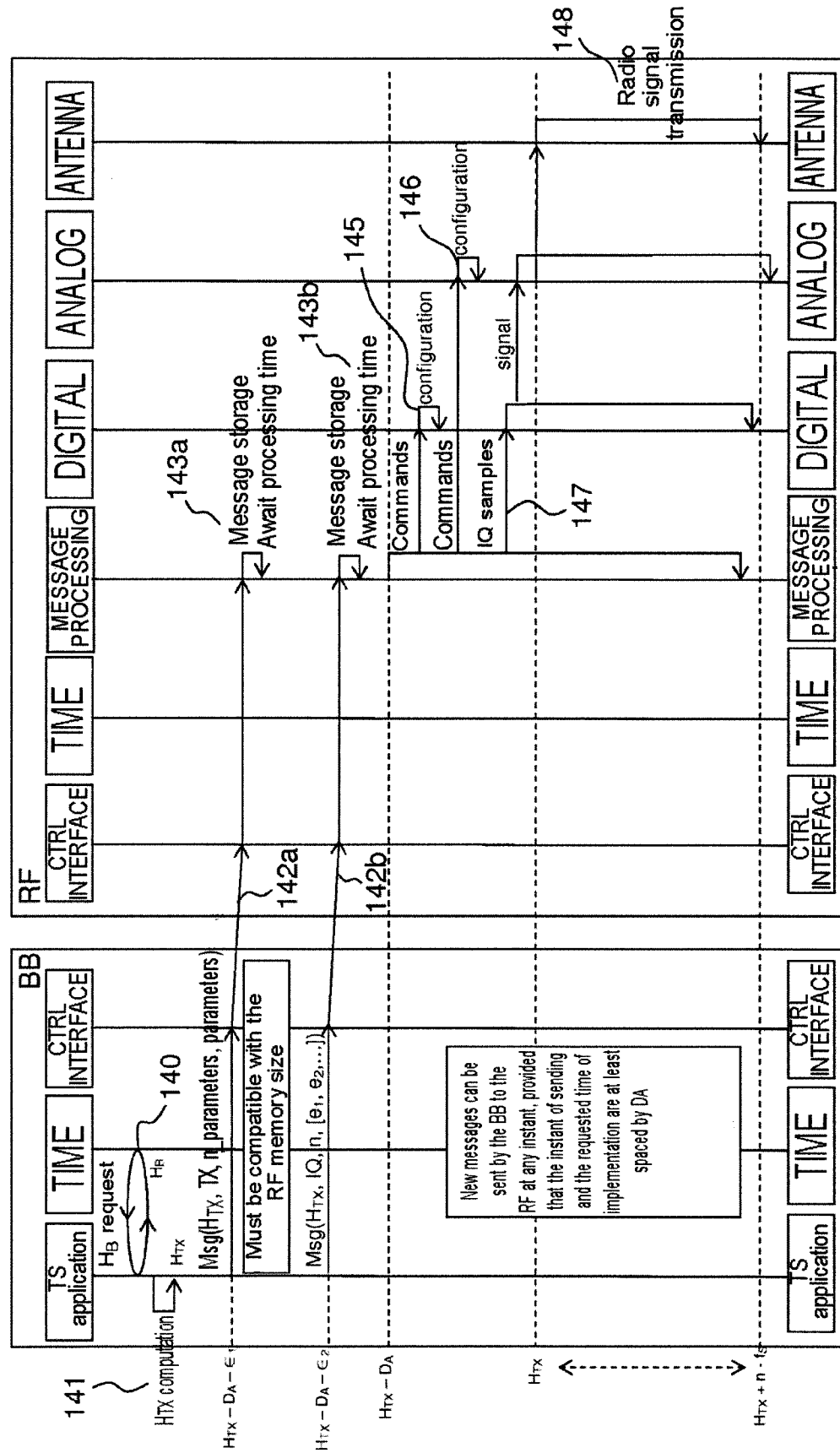


FIG.14

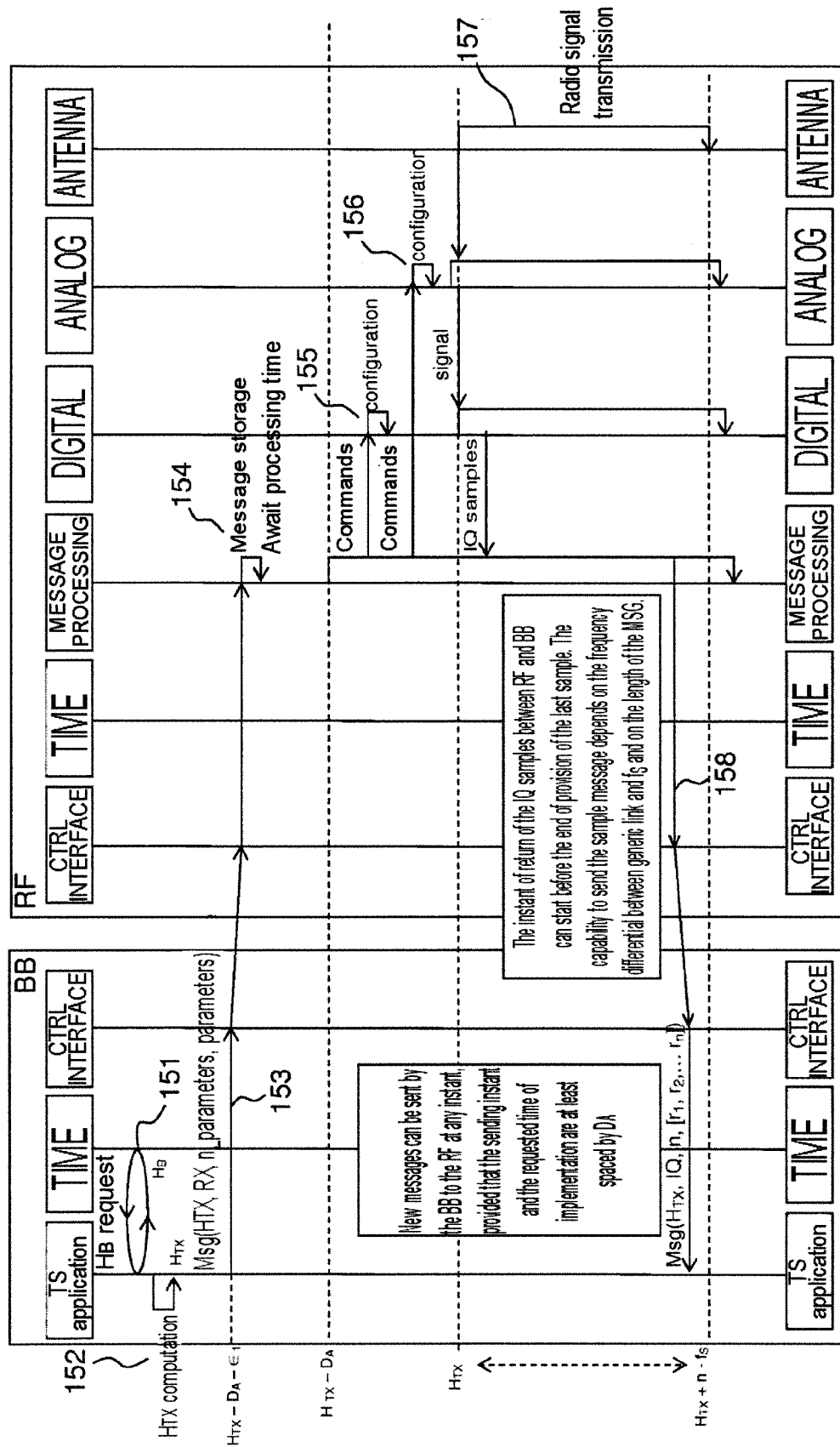


FIG.15

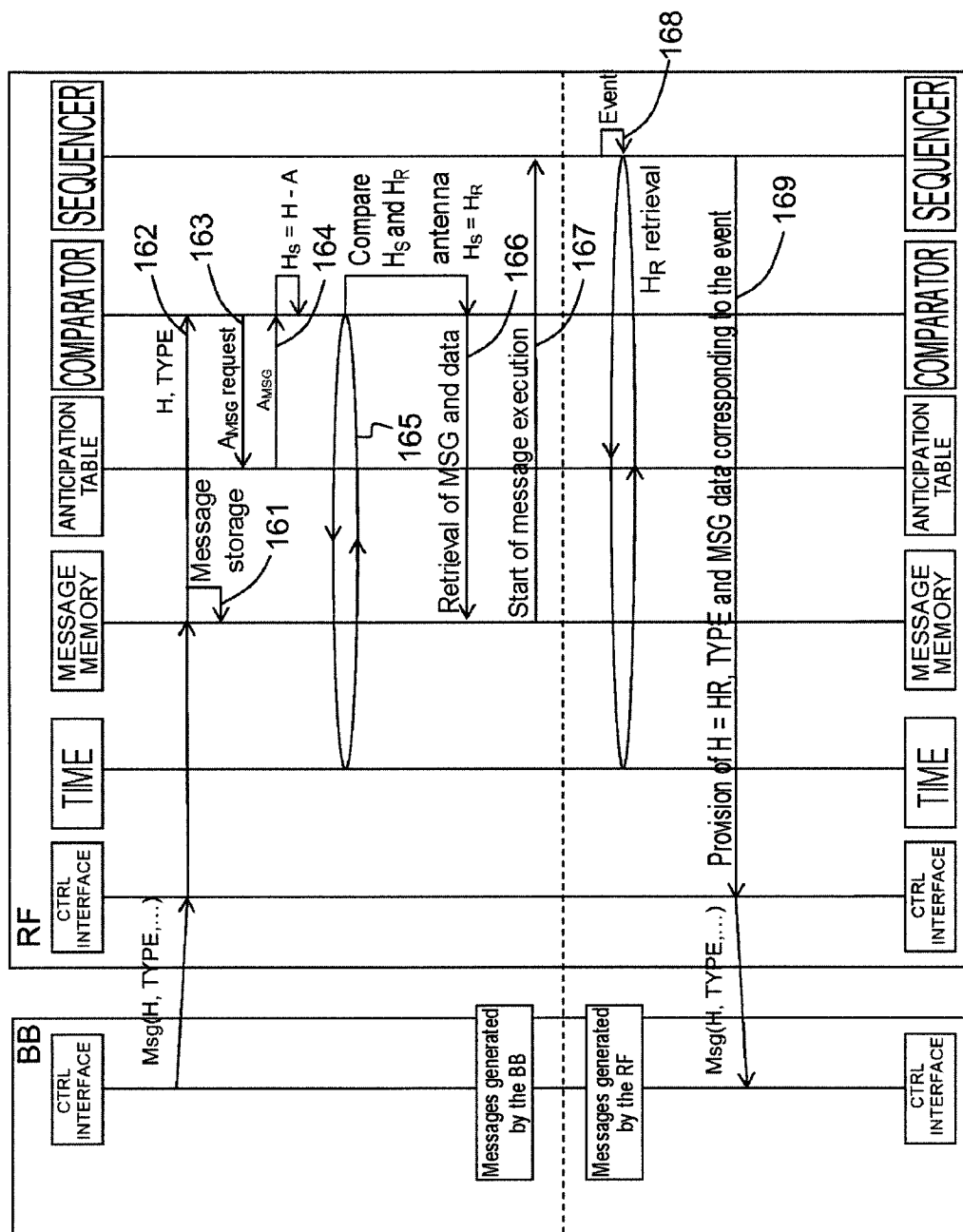


FIG.16