

APPARATUS FOR REPEATEDLY APPLYING SHORT-
CIRCUIT PULSES TO A CURRENT TYPE INVERTER
FOR OUTPUT CURRENT CONTROL

1 This invention relates to the control of current type inverters, and more particularly to the control of a current type inverter utilizing self-extinguish elements for pulse width modulation control.

5 Inverters converting DC power into AC power having a desired frequency are broadly classified into a voltage type and a current type. In the case of the voltage type inverter, its output current waveform is generally sinusoidal, while its output voltage waveform
10 includes pulses distributed in a sinusoidal pattern. On the other hand, in the case of the current type inverter, its output voltage waveform is sinusoidal, while its output voltage waveform is a square waveform.

 In regard to the latter type or current type
15 inverter including thyristors, a proposal has been made in which the inverter is controlled according to a pulse width modulation method similar to that used for the control of the voltage type, so as to improve its output current waveform. However, there has been a limitation in
20 the modulation frequency range in view of the operating characteristics of the thyristors used to constitute the prior art current type inverter, and the desired improvement of the output current waveform by the pulse width modulation technique has been limited to a specific
25 frequency range only. With a view to obviate the drawback

- 1 of the prior art current type inverter, the inventors
have proposed a current type inverter which utilizes
self-extinguish elements operable even in a high frequency
range, which is simple in construction and in which pulse
5 width modulation control can be effected up to the high
frequency range. (Japanese Patent Application No. 56-
186815 corresponding to US Patent Application Serial No.
443,398 and EPC Patent Application Serial No.
82110784.4)
- 10 Such a current type inverter using self-extin-
guish elements as proposed by the inventors can provide
an output current waveform closer to the sinusoidal
waveform than the prior art one when high-frequency pulse
width modulation is effected. However, an attempt to
15 control not only the output current waveform but also the
value of the output currents of the proposed current
type inverter has been quite difficult as far as the known
manner of pulse pattern control is resorted to. This is
because, in the case of the current type inverter which is
20 supplied with direct current from a DC power source and
which is not allowed to be left in an open-circuit
condition unlike the voltage type inverter, the pulse
pattern for effecting the control according to the pulse
width modulation technique must be determined within the
25 above limitation.

More precisely, in the case of the current type
inverter, one of the phases at the positive arms and one
of the phases at the negative arms must be in the on-state.

1 Therefore, when the width of pulses applied to one of the
phases is narrowed so as to decrease the output current
of that phase, the width of pulses applied to another
phase must be widened. This results not only in an
5 unbalance of the output currents of the three phases but
also in a non-sinusoidal output current waveform. There-
fore, the desired output current waveform cannot be
obtained when the balance among the three phases and the
current waveforms of the three phases are considered.

10 A technique for generating a sinusoidal output
current waveform from a current type inverter is discussed
in a paper entitled "A Novel PWM Technique for Three
Phase Inverter/Converter" reported by T. Ohnishi et al in
IEEJ, Conference Record IPEC-Tokyo, pp. 384-395 (March,
15 1983).

This paper discloses an inverter control apparatus
capable of providing a sinusoidal output current waveform
and capable of also controlling the value of the output
currents. However, the proposed control apparatus requires
20 a high switching frequency resulting in an increased loss
of the elements. Accordingly, the proposed control
apparatus has shortcomings from the viewpoints of efficien-
cy improvement and capacity increase.

It is therefore a primary object of the present
25 invention to provide an apparatus for controlling a
current type inverter, which can provide output voltages
and output currents of sinusoidal waveform containing
higher harmonics in a very small proportion and which can

achieve variable control of the output currents over a wide range.

According to the present invention there is provided an apparatus for controlling a current type inverter including a plurality of self extinguishing elements connected in a bridge circuit; the self-extinguish
5 elements being arranged to be triggered by pulse width modulation signals, said apparatus comprising:

clock generator means for generating a clock signal in accordance with a frequency command;

pulse width modulation pattern generation circuit means for
10 generating, in synchronism with said clock signal, pulse width modulation pattern signals for respective ones of said self-extinguish elements;

short-circuit pulse generating circuit means for generating, in synchronism with said clock signal, short-circuit pulses having a predetermined pulse width for turning on ones of said self-extinguish
15 elements connected in series with others of said self-extinguish elements to form pairs in said bridge circuit, the others of said self-extinguish elements being arranged to be turned on by the corresponding pulse width modulation pattern signals, thereby enabling short-circuiting of a DC circuit of said inverter;

20 composite circuit means for generating trigger pattern signals for triggering said self-extinguish elements of said bridge circuit in accordance with said pulse width modulation pattern signals and said short-circuit pulse signals; and

driver circuit means for delivering trigger signals to said self-
25 extinguish elements of said bridge circuit in accordance with said trigger pattern signals.

The present invention will be apparent from the following detailed description taken in conjunction with the accompanying drawings, in which:

30 FIG. 1 is a circuit diagram of a current type inverter using self-extinguish elements;

FIG. 2 is a block diagram showing the structure of one form of a prior art inverter control apparatus;

FIG. 3 shows the relation between the output pulses of the prior
35 art inverter control apparatus shown in FIG. 2 and the three-phase output currents of the inverter;

FIG. 4 is a block diagram showing the structure

1 of an embodiment of the inverter control apparatus
according to the present invention;

FIG. 5 shows the relation between the output
pulses of the inverter control apparatus shown in FIG. 4
5 and the three-phase output currents of the inverter;

FIG. 6 is an enlarged waveform diagram of part
of FIG. 5;

FIG. 7 is a block diagram showing the structure
of another embodiment of the present invention;

10 FIG. 8 illustrates the operation of the short-
circuit pulse generating circuit in the embodiment
shown in FIG. 7;

FIG. 9 is a signal and current waveform diagram
for illustrating the operation of the embodiment shown
15 in FIG. 7;

FIGS. 10(a) and 10(b) illustrate the relation
between the short-circuit pulse width and the output
current waveform in the embodiment shown in FIG. 7;

FIG. 11 is a block diagram showing the structure
20 of still another embodiment of the present invention;

FIG. 12 is a signal and current waveform diagram
for illustrating the operation of the embodiment shown
in FIG. 11;

FIG. 13 is an enlarged waveform diagram of part
25 of FIG. 12;

FIG. 14 illustrates the inverter operation under
the signal condition shown in FIG. 13;

FIG. 15 is a block diagram showing the structure

1 of yet another embodiment of the present invention;

FIG. 16 is a signal and current waveform diagram for illustrating the operation of the embodiment shown in FIG. 15;

5 FIG. 17 is an enlarged waveform diagram of part of FIG. 16;

FIG. 18 illustrates the inverter operation under the signal condition shown in FIG. 17;

FIG. 19 is a signal and current waveform diagram for illustrating the operation of a further embodiment of the present invention; and

FIG. 20 is an enlarged waveform diagram of part of FIG. 19.

Referring now to the drawings, FIG. 1 shows a
15 current type inverter which has been proposed by the inventors and which utilizes self-extinguish elements such as gate turn-off (GTO) thyristors. Referring to FIG. 1, pairs of self-extinguish elements S_U , S_X ; S_V , S_Y ; and S_W , S_Z connected in series are connected in
20 parallel with one another to constitute a bridge circuit of the current type inverter 3 connected across a DC power source 1 through a DC reactor 2 and controlled by a control apparatus 6. Outputs derived from the connection points between the self-extinguish elements
25 S_U and S_X , between the self-extinguish elements S_V and S_Y , and between the self-extinguish elements S_W and S_Z respectively are supplied to a load 4 which may be a three-phase motor. Three output-terminal capacitors 5

1 of Y or Δ connection are connected across the output terminals of the inverter 3.

FIG. 2 shows the structure of a prior art control apparatus 6 used for the pulse width modulation (PWM) control of such a current type inverter including such self-extinguish elements. Referring to FIG. 2, the control apparatus 6 includes a clock generating circuit 61, a PWM pattern generating circuit 62 and a drive circuit 63. In response to the application of a frequency command signal f , signals P_U , P_Z , P_V , P_X , P_W and P_Y having the desired PWM patterns are applied to the gates of the associated self-extinguish elements S_U , S_Z , S_V , S_X , S_W and S_Y respectively.

FIG. 3 is a signal and current waveform diagram showing the waveforms of inverter output currents I_U , I_V and I_W compared with those of the gate signals P_U , P_Z , P_V , P_X , P_W and P_Y applied to the gates of the respective self-extinguish elements S_U , S_Z , S_V , S_X , S_W and S_Y in the inverter 3.

20 The current type inverter proposed by the inventors and utilizing the self-extinguish elements is advantageous in that, in spite of its simple construction, high-frequency pulse width modulation can be achieved to provide output currents including higher harmonics in a very small proportion. However, as far as triggering of the proposed current type inverter is controlled by the PWM pattern signals provided under consideration of not leaving the inverter in its open-circuit condition, as

1 shown in FIG. 3, it is unable to control the output current
value in the inverter itself as in the case of prior art
current type inverters.

FIG. 4 is a block diagram showing the structure
5 of an embodiment of the inverter control apparatus accord-
ing to the present invention which has such a function
that, while one of the self-extinguish elements forming
one of the pairs with the other is turned on, an on pulse
is applied to the other at the same time.

10 Referring to FIG. 4, a clock generating circuit
61 generates a clock signal having a frequency propor-
tional to an inverter frequency command signal f applied
thereto. A pulse width modulation (PWM) pattern generat-
ing circuit 62 generates, in synchronism with the clock
15 signal, PWM pulse pattern signals having pulse widths
corresponding to the triggering (on-off) durations of the
individual self-extinguish elements S_U, S_Z, S_V, S_X, S_W
and S_Y . The patterns are such that the pulse width
distribution provides inverter output current of sinu-
20 soidal waveform. On the basis of the PWM pattern signals
applied thereto, a drive circuit 63 generates gate
signals P_U, P_Z, P_V, P_X, P_W and P_Y which are applied to the
gates of the associated self-extinguish elements $S_U, S_Z,$
 S_V, S_X, S_W and S_Y respectively.

25 The output signal from the clock generating
circuit 61 is applied not only to the PWM pattern generat-
ing circuit 62 but also to an on-pulse generating circuit
64 (which will be referred to hereinafter as a short-

1 circuit pulse generating circuit). This short-circuit
pulse generating circuit 64 generates short-circuit pulses
applied to the self-extinguish elements which form the
pairs with those turned on according to the PWM patterns.
5 The PWM pattern generating circuit 62 is similar to that
shown in FIG. 2, and its output signals are similar to
the signals $P_U, \dots, P_Y$ shown in FIG. 3. The output
signals from the PWM pattern generating circuit 62
are applied together with the output signal from the
10 short-circuit pulse generating circuit 64 to a composite
signal generating circuit 65 which provides composite
output signals. The output signals from this composite
signal generating circuit 65 are applied to the drive
circuit 63 to appear therefrom as the signals $P_U, P_Z, P_V,$
15 P_X, P_W and P_Y with the timing shown in FIG. 5. The
signals P_U, P_Z, P_V, P_X, P_W and P_Y shown in FIG. 5 have
waveforms different from those shown in FIG. 3 in that
the short-circuit pulses generated from the short-circuit
pulse generating circuit 64 are added to the corresponding
20 waveforms shown in FIG. 3.

FIG. 6 is an enlarged waveform diagram of part
of FIG. 5 for illustrating the generating timing of the
short-circuit pulses. Referring to FIG. 6, a signal U_1
is generated as the gate signal P_U from the PWM pattern
25 generating circuit 62, and this signal U_1 is followed by
a train of short-circuit pulses S_1, S_2 and S_3 generated
from the short-circuit pulse generating circuit 64 in
synchronism with the leading edge of pulses X_1, X_2 and

(37)

1 X_3 respectively of the gate signal P_X . The pulse width of
the short-circuit pulses S_1 , S_2 and S_3 is smaller than
that of any one of the pulses generated from the PWM
pattern generating circuit 62. In the embodiment of the
5 present invention being described, such short-circuit
pulses are applied to the self-extinguish element S_U
forming the pair with the self-extinguish element S_X .
However, such short-circuit pulses may be applied to the
self-extinguish element S_Y forming the pair with the
10 self-extinguish element S_V .

It will be seen from the waveforms of the output
currents I_U , I_V and I_W shown in FIGs. 5 and 6, the value
of these output currents varies depending on the pulse
width d of the applied short-circuit pulses. Since, thus,
15 the value of the output currents is small and large when
the pulse width d of the short-circuit pulses is large
and small respectively, the value of the output currents
can be controlled by controlling the pulse width d of the
short-circuit pulses.

20 FIG. 7 is a block diagram showing the structure
of another embodiment of the control apparatus according
to the present invention. Referring to FIG. 7, a clock
generating circuit 61, a PWM pattern generating circuit 62
and a drive circuit 63 have functions similar to those
25 shown in FIG. 2.

A frequency divider circuit 66 divides the
frequency of the clock signal generated from the clock
generating circuit 61 and acts also to generate a pulse

1 train signal Q_1 which has a predetermined pulse width d_s
corresponding to the desired output current value and
which is synchronous with the frequency-divided clock
signal. This pulse train signal Q_1 is applied to a short-
5 circuit pulse generating circuit 64.

FIG. 8 illustrates the operation of the short-
circuit pulse generating circuit 64. Referring to FIG. 8,
the short-circuit pulse generating circuit 64 receives
PWM pattern signal portions Q_{21} and Q_{22} of PWM pattern
10 signals Q_2 applied from the PWM pattern generating circuit
62. These PWM pattern signal portions Q_{21} and Q_{22}
correspond to the phase of 0 to $1/3\pi$ and the phase of $2/3\pi$
to π , respectively. In the short-circuit pulse generating
circuit 64, the PWM pattern signal portions Q_{21} and Q_{22}
15 are applied to AND gates together with the pulse train
signal Q_1 of predetermined pulse width d_s applied from the
frequency divider circuit 66, and the resultant short-
circuit pulse train signals Q_{31} and Q_{32} corresponding to
the PWM pattern signal portions Q_{21} and Q_{22} respectively
20 are applied to a composite signal generating circuit
65. In the composite signal generating circuit 65,
the short-circuit pulse train signals Q_{32} and Q_{31} are
added to the (0 to $1/3\pi$) and ($2/3\pi$ to π) phase portions
respectively of PWM pattern signals Q_5 generated from the
25 PWM pattern generating circuit 62 for controlling the
associated self-extinguish elements. The resultant PWM
pattern signals Q_6 are applied from the composite signal
generating circuit 65 to the drive circuit 63.

1 In the control apparatus having the structure
shown in FIG. 7, gate signals P_U , P_Z , P_V , P_X , P_W and P_Y
having waveforms as shown in FIG. 9 are generated from
the drive circuit 63. Thus, for example, in the period I
5 in FIG. 9, the self-extinguish element S_W is on-off
controlled by the gate signal P_W based on the PWM pattern
signal Q_{22} . On the other hand, the self-extinguish
element S_Z forming the pair with and connected in series
with the self-extinguish element S_W on the arm of the
10 same phase is on-off controlled by the gate signal P_Z
based on the short-circuit pulse train signal Q_{32} as
seen in FIG. 9. Similarly, the self-extinguish element
 S_U is on-off controlled by the gate signal P_U based on the
PWM pattern signal Q_{21} , and the self-extinguish element
15 S_X is on-off controlled by the gate signal P_X based on
the short-circuit pulse train signal Q_{31} . In other words,
the self-extinguish elements each forming the pair with
and connected on the same arm to the self-extinguish
element intermittently turned on in the periods I to
20 VI in FIG. 9 are turned on by the short-circuit pulse
train signals Q_3 , and, during the period of the pulse
width d_s , the DC voltage E_D is short-circuited through
the DC reactor 2. During this short-circuited period,
the output currents I_U , I_V and I_W are null, and, there-
25 fore, the output currents I_U , I_V and I_W have waveforms
as shown in FIG. 9. The waveforms of the currents to be
supplied to the load 4 are averaged by the function of
the output-terminal capacitors 5 so that the actual

1 currents I_U , I_V and I_W supplied to the load 4 have sinusoidal waveforms as indicated by the dotted curves in FIG. 9. According to this second embodiment, the mean values of the output currents I_U , I_V and I_W can be
5 controlled over a wide range by varying the pulse width d_s of the short-circuit pulses, and, also, the current waveforms are less distorted than in the case of the first embodiment.

FIGs. 10(a) and 10(b) show the waveform (the
10 half-cycle) of one of the output currents I_U , I_V and I_W at different pulse widths d_s of the short-circuit pulses. In the case of FIG. 10(a), in which the pulse width d_s is small, the mean value of the output current is large as indicated by the dotted curve. In contrast, in the
15 case of FIG. 10(b) in which the pulse width d_s is larger than that in FIG. 10(a), the mean value of the output current is small. It will thus be seen that the output currents of the inverter can be varied over a wide range (from about 0% to 100%) even when the value of the direct
20 current I_D is maintained constant. It is needless to mention that the minimum current value is controlled by the minimum allowable pulse width of the short-circuit pulses applied to the self-extinguish elements.

It will be seen from the aforementioned
25 embodiments of the control apparatus according to the present invention that a current type inverter can generate output currents of sinusoidal waveform, and the value of the output currents can be varied over a very

1 wide range.

FIG. 11 is a block diagram showing the structure of still another embodiment of the control apparatus according to the present invention. This embodiment is especially so constructed that pulse patterns of triggering or short-circuit pulses applied to self-extinguish elements are provided by comparing a function signal having the same period as or synchronous with PWM pattern signals with the command value of AC output currents required for the current type inverter.

Referring to FIG. 11, a clock signal having a frequency proportional to an inverter frequency command signal f is generated from a clock generating circuit 61. The frequency command signal f is also applied to a pattern select signal generating circuit 76 which generates a pattern select signal. The clock output signal from the clock generating circuit 61 is applied to a frequency divider circuit 79 which generates distribution signals R_U, R_Z, R_V, R_X, R_W and R_Y described in detail later. The clock signal is also applied to a reference pattern generating circuit 72 which generates a reference pattern signal P , and to a non-uniform-period triangular waveform generating circuit 77 which generates a triangular waveform signal W having a non-uniform period synchronous with the reference pattern signal P . The triangular waveform signal Q is compared with an AC output current command signal I_R^* in a short-circuit pulse generating circuit 64 which generates short-circuit pulses S for

1 simultaneously turning on one of the pairs of the self-extinguish elements connected to the positive and negative arms of the inverter thereby forcedly short-circuiting the DC circuit of the inverter. In response
5 to the application of the reference pattern signal P and short-circuit pulses S , a PWM pattern generating circuit 62 generates PWM pattern signals P_F and P_R corresponding to a front 60° period and a rear 60° period in the 180° period of the inverter operation. In response to the
10 application of the distribution signals R_U, R_Z, R_V, R_X, R_W and R_Y together with the PWM pattern signals P_F, P_R and short-circuit pulses S , a composite signal generating circuit 65 generates composite pattern signals, $P_U', P_Z', P_V', P_X', P_W'$ and P_Y' distributed to the three phases to
15 control each 180° period of the inverter operation. The gate signal patterns $P_U', P_Z', P_V', P_X', P_W'$ and P_Y' thus obtained are applied to a drive circuit 63 to provide gate signals P_U, P_Z, P_V, P_X, P_W and P_Y applied to the self-extinguish elements S_U, S_Z, S_V, S_X, S_W and S_Y
20 respectively.

FIG. 12 shows in further detail the process of generation of the signals above described. Referring to FIG. 12, the distribution signals R_U, R_Z, R_V, R_X, R_W and R_Y generated from the frequency divider circuit 79
25 have a pulse width T corresponding to the 60° period of the inverter operation and have a phase difference of 60° therebetween. The triangular waveform output signal Q from the non-uniform-period triangular waveform

(48)

1 generating circuit 77 has its maximum or peak value
2 I_{RMAX} at the rise time of the pulses of the reference
3 pattern signal P. This triangular waveform signal Q
4 is called the non-uniform-period triangular waveform
5 signal herein since the period of each pulse thereof is
6 determined by the pulse width of the corresponding
7 pulse of the reference pattern signal P and is therefore
8 non-uniform. The AC output current command signal I_R^*
9 is compared with the non-uniform-period triangular
10 waveform signal Q to provide the short-circuit pulse
11 train S as shown in FIG. 12. Then, the reference pattern
12 signal P and short-circuit pulse signal S are inverted
13 to provide an inverted reference pattern signal $\bar{P}$ and
14 an inverted short-circuit pulse signal $\bar{S}$ respectively.
15 The signals P and $\bar{S}$ are applied to an AND gate to obtain
16 the signal P_F , and the signals $\bar{P}$ and $\bar{S}$ are applied to
17 another AND gate to obtain the signal P_R . The signals P_F ,
18 R_Y , P_R , P_Z ; and S, R_X are applied to AND gates to obtain
19 signals P_F' , P_R' and S' respectively, and, then, the
20 signals P_F' , P_R' , S' and R_U are applied to an OR gate
21 to obtain the gate signal pattern P_U' applied to the
22 gate of the self-extinguish element S_U . Entirely
23 similarly, the gate signal patterns P_Z' , P_V' , P_X' , P_W'
24 and P_Y' for the other self-extinguish elements S_Z , S_V ,
25 S_X , S_W and S_Y respectively can be obtained. The output
currents I_U , I_V and I_W of the inverter controlled by the
gate signals P_U , P_Z , P_V , P_X , P_W and P_Y in each cycle of
the inverter operation have pulse-width modulated waveforms

1 over 360° as shown in FIG. 12.

FIG. 13 is an enlarged waveform diagram showing in further detail the waveforms of the triangular waveform signal Q , gate signal patterns P_U' , P_Z' , P_V' , P_X' , P_W' , P_Y' ,
5 and output currents I_U , I_V , I_W in the inverter operation period I shown in FIG. 12. In this period I, the short-circuit pulse train S obtained as a result of comparison between the triangular waveform signal Q and the output current command I_R^* corresponds to the gate signal
10 pattern P_V' .

The fact that the output currents I_U , I_V and I_W of the inverter are null in the short-circuited period will be described with reference to FIG. 14, and how the values of the output currents I_U , I_V and I_W can be
15 controlled by varying the value of the AC output current command I_R^* will then be described. FIG. 14 illustrates the operation of the inverter circuit before and after a signal V_2 of the gate signal pattern P_V' shown in FIG. 13 is applied. In FIG. 13, suppose that the output
20 current I_W rises at time t_0 , falls at time t_1 and rises again at time t_3 , while the output current I_V rises at time t_2 between the times t_1 and t_3 . Then, the operating conditions of the inverter from time t_0 to time t_3 are as shown in FIGs. 14(a), 14(b) and 14(c). In the periods
25 $t_0 \leq t \leq t_1$ and $t_2 \leq t \leq t_3$ shown in FIGs. 14(a) and 14(b) respectively, the inverter makes its usual switching operation. However, in the period $t_2 \leq t \leq t_3$ shown in FIG. 14(b), the gate signal V_2 , hence, the short-circuit

- 1 pulse S acts to turn on the self-extinguish element S_V ,
and the DC circuit is short-circuited by the self-extinguish
elements S_V and S_Y , with the result that the direct
current I_D flows under the DC short-circuited condition
5 of the inverter. At this time, the output currents of
U-phase, V-phase and W-phase are not supplied to the load
4. On the other hand, when the value of the AC output
current command I_R^* is varied from zero to the maximum
 I_{RMAX} , the short-circuit periods d_{S1} , d_{S2} and d_{S3} of
10 the output current I_U vary from d_1 , d_2 and d_3 to zero
respectively while maintaining the following relation:

$$\frac{d_{S1}}{d_1} = \frac{d_{S2}}{d_2} = \frac{d_{S3}}{d_3} = 1 - \frac{I_R^*}{I_{RMAX}} \dots\dots\dots (1)$$

The output current I_W is entirely similarly
controlled. In the case of the output current I_V too,
the periods d_{S1} , d_{S2} and d_{S3} vary while maintaining the
15 following relation:

$$\frac{d_{S1} + d_{S3}}{d_1 + d_3} = \frac{d_{S2} + d_{S2}}{d_2 + d_2} = \frac{d_{S3} + d_{S1}}{d_3 + d_1} = 1 - \frac{I_R^*}{I_{RMAX}} \dots\dots\dots (2)$$

The value of the effective current I_{RMS} at this time is
given by the following equation:

46

$$I_{RMS} = \sqrt{\frac{2(d_1+d_2+d_3)}{3(d_0+d_1+d_2+d_3)}} \times \sqrt{\frac{I_R^*}{I_{RMAX}}} \times I_D \dots\dots\dots (3)$$

1 The value of the effective current $I_{RMS} = 0$ when $I_R^* = 0$ and short-circuit continues throughout the periods, and I_{RMS} is given by the following equation when $I_R^* = I_{RMAX}$:

$$I_{EMS} = \sqrt{\frac{2(d_1+d_2+d_3)}{3(d_0+d_1+d_2+d_3)}} \times I_D \dots\dots\dots (4)$$

5 The value of I_{RMS} varies in proportion to $\sqrt{I_R^*}$ since the values of I_D , I_{RMAX} , and d_0 to d_3 are constant.

In the present embodiment, the PWM patterns corresponding to the intermediate 60° period in the 180° period of the inverter operation are similarly provided as shown in the waveforms of the output currents I_U , I_V and I_W in FIG. 12, and, therefore, the content of higher harmonics in the output currents can be decreased to a minimum. Further, the output currents can be controlled over the wide range of from zero to the maximum value given by the equation (4) determined by the PWM reference pattern signal P.

In the embodiment shown in FIG. 11, the short-circuit pulses have been included in the intermediate 60° period portion of the 180° period in which no PWM pattern signals are present. This period corresponds to, for

47

1 example, the inverter operation period V in the case of
the gate signal pattern P_U' in FIG. 12. However, the
short-circuit pulses may be included in the 120° period
portion of the 180° period in which no PWM pattern
5 signal is present and from which the intermediate 60°
period portion is excluded. For example, the short-
circuit pulses may be included in the inverter operation
periods IV and VI in the case of the gate signal pattern
 P_U' .

10 FIG. 15 is a block diagram of such a modification
of the control apparatus. This modification differs from
the embodiment shown in FIG. 11 in that short-circuit
pulse trains S_1 and S_2 are added to the outputs of the
PWM pattern generating circuit 62, and the function
15 of the composite signal generating circuit 65 is different
from that shown in FIG. 11. FIG. 16 shows the process of
signal formation in this modification. Referring to
FIGs. 15 and 16, the triangular waveform signal Q is
compared with the value of the AC output current command
20 I_R^* to produce the short-circuit pulse train S. Then,
the signals P and S are inverted to provide the inverted
signals $\bar{P}$ and $\bar{S}$, and the signals $\bar{P}$, S and P, S are applied
to AND gates to obtain short-circuit pulse trains S_2 and
 S_1 respectively. Then, in the composite signal generating
25 circuit 65, the signals $P_F (= P)$, R_Y ; $\bar{S}$, R_U ; $P_R (= P)$,
 R_Z ; S_1 , R_V ; and S_2 , R_W are applied to AND gates to obtain
signals P_F' , $\bar{S}'$, P_R' , S_1' and S_2' respectively, and these
signals P_F' , $\bar{S}'$, P_R' , S_1' and S_2' are applied to an OR

- 1 gate to obtain the gate signal pattern P_U' to be applied
to the self-extinguish element S_U . In an entirely
similar manner, the gate signal patterns for the other
self-extinguish elements can be provided. As a result,
5 the output currents I_U , I_V and I_W of the inverter
controlled by the gate signals P_U , P_Z , P_V , P_X , P_W and P_Y
in each cycle of the inverter operation have pulse-width
modulated waveforms over 360° as shown in FIG. 16.

- FIG. 17 is an enlarged waveform showing in
10 further detail the waveforms of the triangular waveform
signal Q , gate signal patterns P_U' , P_Z' , P_V' , P_X' , P_W' ,
 P_Y' and output currents I_U , I_V , I_W in the inverter operation
period I shown in FIG. 16. In this period I, the short-
circuit pulse train S obtained as a result of comparison
15 between the triangular waveform signal Q and the AC
output current command I_R^* is divided to be included
in the signals P_Z' and P_X' . FIG. 18 illustrates how the
inverter operates from time $t = t_0$ to time $t = t_3$ in
the diagram shown in FIG. 17. FIG. 18 illustrating the
20 states of the inverter circuit controlled by the control
apparatus shown in FIG. 15 differs from FIG. 14 illust-
rating the states of the inverter circuit controlled by
the control apparatus shown in FIG. 11 in that, whereas
the DC circuit is short-circuited in the V-phase in the
25 period $t_1 \leq t \leq t_2$ in the case of the latter, it occurs
in both of the W-phase and V-phase in the case of the
former. Except for the above difference, the manner of
output current control in the modification shown in

1 FIG. 15 is similar to that in the embodiment shown in
FIG. 11.

It will be seen from the diagrams of FIGs. 14 and
18 illustrating the circuit states of the embodiments
5 shown in FIGs. 11 and 15 respectively that the effect
of the present invention is entirely the same when these
two embodiments are combined so that short-circuit of the
DC circuit occurs in three periods in a fashion distributed
to the W-phase, V-phase and U-phase. In this case, the
10 short-circuit pulse train S is included in all of the
180° periods where no PWN pattern signals are present.

In the aforementioned embodiments, the short-
circuit pulse train S has been produced by comparing the
triangular waveform signal Q with the AC output current
15 command I_R^* . However, the effect of the present
invention is entirely the same when the triangular waveform
signal Q is split into two non-uniform-period sawtooth
waveform signals by bisecting at the peak of the signal Q.
As an example, whereas a triangular waveform signal Q
20 as shown in FIG. 12 is generated from the non-uniform-
period triangular waveform generating circuit 77 in the
embodiment shown in FIG. 11, such a signal Q may be split
into two sawtooth waveform signals Q_1 and Q_2 as shown in
FIG. 19, and these signals Q_1 and Q_2 may be compared with
25 the AC output current command I_R^* to obtain short-circuit
pulse trains S_1 and S_2 respectively. These pulse
trains S_1 and S_2 are then applied to an OR gate to derive
a pulse train entirely similar to the short-circuit pulse

1 train S shown in FIG. 12. Gate signals to be applied to
the self-extinguish elements can then be produced on the
basis of the short-circuit pulse train S as described with
reference to FIG. 12 thereby providing output currents
5 having entirely similar waveforms. Further, the value of
the output currents can be similarly varied as described.

Further, in the embodiment shown in FIG. 11 or
15, the PWM pattern signal P_F corresponding to the
front 60° period may be used as the reference pattern
10 signal P, and the PWM pattern signal P_R corresponding to
the rear 60° period may be used as the inverted signal
 $\bar{P}$. FIG. 20 shows the waveforms of the gate signal
patterns and output currents in the inverter operation
period I in such a case. FIG. 20 differs from FIG. 13
15 showing the operation of the embodiment shown in FIG. 11
in that, when, for example, a signal V_2 of the gate
signal pattern P_V' is in its high level in the period
 $t_1 \leq t \leq t_2$, a signal W_2 of the gate signal pattern P_W'
is in its high level in the period $t_0 \leq t \leq t_1'$ and a
20 signal U_2 of the gate signal pattern P_U' is in its high
level in the period $t_1' \leq t \leq t_3$. According to the diagram
shown in FIG. 20, during the transition from the circuit
state shown in FIG. 14(a) to that shown in FIG. 14(b),
the self-extinguish element S_V is turned on while
25 maintaining the self-extinguish element S_W in its on state,
and the self-extinguish element S_U is then turned on at
time $t = t_1'$ while maintaining the self-extinguish element
 S_V in its on state. Thereafter, the self-extinguish

1 element S_V is turned off at time $t = t_2$ to cause transition
of the circuit state from that shown in FIG. 14(b) to that
shown in FIG. 14(c). When the self-extinguish element S_W
continues to be turned on during transition of the
5 circuit state from that shown in FIG. 14(a) to that shown
in FIG. 14(b) while the load which may be an electric
motor is under regenerative operation, application of
the gate signal to the self-extinguish element S_V would
not turn on this self-extinguish element S_V and the
10 desired inverter operation would not be done since the
V-phase voltage is higher than the W-phase voltage.
Therefore, the embodiment described with reference to
FIG. 20 is as effective as the embodiments described
with reference to FIGs. 11 and 15 when a static load
15 or regenerative operation of the load is not taken into
consideration, since the desired operation of the inverter
is not done during the regenerative operation of the load,
although this specific embodiment is advantageous for
simplifying the structure of the PWM pattern generating
20 circuit 62. This specific embodiment is also effective
for operation with the sawtooth waveform signals having
the non-uniform period.

It will be understood from the foregoing detailed
description of the present invention that output currents
25 of a current type inverter can be controlled over a wide
range while suppressing the content of higher harmonics in
the output currents to a very small proportion. Especially
when the load is an electric motor, the noise can be



- 1 suppressed to a low level and the efficiency can also be increased. The present invention is further advantageous for simplifying the circuit structure of the inverter and improving the response of the inverter.



53

- 26 -

CLAIMS:

1. An apparatus for controlling a current type inverter including a plurality of self extinguishing elements connected in a bridge circuit; the self-extinguish elements being arranged to be triggered by pulse width modulation signals, said apparatus comprising:
 - 5 clock generator means for generating a clock signal in accordance with a frequency command;
pulse width modulation pattern generation circuit means for generating, in synchronism with said clock signal, pulse width modulation pattern signals for respective ones of said self-extinguish elements;
 - 10 short-circuit pulse generating circuit means for generating, in synchronism with said clock signal, short-circuit pulses having a predetermined pulse width for turning on ones of said self-extinguish elements connected in series with others of said self-extinguish elements to form pairs in said bridge circuit, the others of said self-extinguish
15 elements being arranged to be turned on by the corresponding pulse width modulation pattern signals, thereby enabling short-circuiting of a DC circuit of said inverter;
composite circuit means for generating trigger pattern signals for triggering said self-extinguish elements of said bridge circuit in
20 accordance with said pulse width modulation pattern signals and said short-circuit pulse signals; and
driver circuit means for delivering trigger signals to said self-extinguish elements of said bridge circuit in accordance with said trigger pattern signals.
- 25 2. A control apparatus as claimed in claim 1, wherein said short-circuit pulse generating circuit means enables variation of the pulse width of said short-circuit pulse signals in accordance with a desired output current value of said inverter.
3. A control apparatus as claimed in claim 1 or 2, wherein said
30 short-circuit pulse generating circuit means enables synchronization of said short-circuit pulse signals with rising edges of said pulse width modulation pattern signal.
4. A control apparatus as claimed in claim 1, 2 or 3, wherein said
short-circuit pulse generating circuit means generates said short-circuit
35 pulse signals having a pulse width smaller than any of pulse widths of said pulse width modulation pattern signals.

54



5. An apparatus as claimed in claim 1, including frequency dividing circuit means for generating a pulse train signal having a predetermined pulse width in synchronism with a frequency divided signal obtained by frequency dividing said clock signal; wherein the pulse train signal is arranged to be applied to the short-circuit pulse generating circuit means for ANDing said pulse train signal and portions of said pulse width modulation pattern signals having a phase of 0 to $1/3 \pi$ and a phase $2/3 \pi$ to π , and for generating said short-circuit pulse signals.
6. A control apparatus according to claim 5, wherein said frequency dividing circuit means enables variation of the pulse width of said pulse train signal in accordance with a desired output current value of said inverter.
7. An apparatus as claimed in claim 1, including reference pattern signal generating circuit means for generating, in synchronism with said clock signal, a reference pattern signal having a phase of 0 to $1/3 \pi$ of pulse width modulation pattern signals and being synchronous with respect to $1/3 \pi$ thereof; and non-uniform-period triangular waveform signal generator means for generating a non-uniform-period triangular waveform signal corresponding to said reference pattern signal in synchronism with said clock signal; wherein the short-circuit pulse generating circuit means for generating short-circuit pulse signals for turning on ones of said self-extinguish elements connected in series with others of said self-extinguish elements to form pairs in said bridge circuit, arranged to compare said non-uniform-period triangular waveform signal with a command value of an output current of said inverter, and the pulse width modulation pattern signal generating circuit means is arranged to generate pulse width modulation pattern signals for said self-extinguish elements of said bridge circuit in accordance with said reference pattern signal and said short-circuit pulse signals.
8. A control apparatus according to claim 7, wherein said short-circuit pulse generating circuit means forms said short-circuit pulse signals such that said short-circuit signals exist in a phase of $1/3 \pi$ to $2/3 \pi$ of a period π where said pulse width modulation pattern signals are not present.
9. A control apparatus according to claim 8, wherein said short-circuit pulse generating circuit means forms said short-circuit pulse signals such that said short-circuit pulse signals exist in a phase of 0 to $1/3 \pi$ or $2/3 \pi$ to π of a period π where said pulse width modulation pattern signals are not present.



55

- 28 -

10. A control apparatus for controlling a current type inverter substantially as hereinbefore described with reference to, or as illustrated in, Figs. 4 to 6; or Figs. 7 to 10; or Figs. 11 to 14; or Figs. 15 to 28; or Figs. 19 and 20 of the accompanying drawings.
