

ABSTRACT

A semiconductor device includes a semiconductor substrate having a chip region and an edge region, a lower dielectric layer on the semiconductor substrate, a chip pad on the lower dielectric layer of the chip region, an upper dielectric layer on the lower dielectric layer, which includes a first opening exposing the chip pad on the chip region and a second opening exposing the lower dielectric layer on the edge region, and a redistribution pad connected to the chip pad. The redistribution pad includes a via portion in the first opening and a pad portion extending from the via portion onto the upper dielectric layer.

FIG. 5B