CLAIMS:

1. An apparatus comprising:
a first memory cell comprising a first storage component having a first end coupled to a first plate line and a second end coupled to a first digit line;
a second memory cell comprising a second storage component having a first end coupled to a second digit line different from the first digit line and a second end coupled to a second plate line different from the first plate line;
a first set of alternating plate lines and digit lines – the first set comprising the first plate line and the second digit line, and the second digit line of the second memory cell adjacent to the first plate line of the first memory cell-; and
a second set of alternating plate lines and digit lines – the second set comprising the second plate line and the first digit line, and the first digit line of the first memory cell adjacent to the second plate line of the second memory cell.
2. The apparatus of Claim 1, further comprising:
a third memory cell comprising a third storage component having a first end coupled to a third plate line and a second end coupled to a third digit line,
wherein the second digit line of the second memory cell is adjacent to the third plate line of the third memory cell.
3. The apparatus of Claim 2, further comprising:
a first layer of memory cells; and
a second layer of memory cells that includes the first memory cell, the second memory cell, and the third memory cell.
4. The apparatus of Claim 3, further comprising:
a fourth memory cell included in the first layer of memory cells, the fourth memory cell comprising a fourth storage component having a first end coupled to a fourth plate line and a second end coupled to a fourth digit line;
wherein the fourth digit line of the fourth memory cell and the second digit line of the second memory cell are combined into a shared digit line.
5. The apparatus of claim 3, further comprising:
a fourth memory cell included in the first layer of memory cells, the fourth memory cell comprising a fourth storage component having a first end coupled to a fourth digit line and a second end coupled to a fourth plate line;

wherein the second digit line of the second memory cell is adjacent to the fourth plate line of the fourth memory cell.

6. The apparatus of claim 1, wherein the first end of the first storage component of the first memory cell is coupled to the first plate line through a first selection component.

7. The apparatus of claim 6, wherein the second end of the first storage component of the first memory cell is coupled to the first digit line through a second selection component.

8. The apparatus of claim 1, wherein the first and second storage components are dielectric capacitors.

9. The apparatus of claim 1, wherein the first and second storage components are ferroelectric capacitors.

10. An apparatus, comprising:

a first layer of memory cells;

a second layer of memory cells underlying the first layer of memory cells;

a first memory cell included in the first layer of memory cells - the first memory cell comprising a storage component having a first end coupled to a plate line and a second end coupled to a digit line-;

a second memory cell included in the second layer of memory cells - the second memory cell comprising a storage component having a first end coupled to a digit line and a second end coupled to a plate line-;

a third memory cell included in the first layer of memory cells – the third memory cell comprising a storage component having a first end coupled to a digit line and a second end coupled to a plate line-;

a fourth memory cell included in the second layer of memory cells – the fourth memory cell comprising a storage component having a first end coupled to a plate line and a second end coupled to a digit line-; and,

a set of alternating plate lines and digit lines,

wherein the digit line of the first memory cell and the digit line of the second memory cell are combined into a digit line shared between the first and second memory cells;

the plate line of the third memory cell and the plate line of the fourth memory cell are combined into a plate line shared between the third and fourth memory cells; and

the set of plate lines and digit lines includes the shared plate line and the shared digit line adjacent to the shared plate line.

11. The apparatus of Claim 10, comprising:

a fifth memory cell included in the first layer of memory cells – the fifth memory cell comprising a storage component having a first end coupled to digit line and a second end coupled to a plate line-; and,

a sixth memory cell included in the second layer of memory cells – the sixth memory cell comprising a storage component having a first end coupled to a plate line and a second end coupled to a digit line,

wherein the plate line of the fifth memory cell and the plate line of the sixth memory cell are combined into a plate line shared between the fifth and sixth memory cells; and

the shared digit line of the first and second memory cells is adjacent to the shared plate line of the fifth and sixth memory cells.

12. The apparatus of Claim 10, wherein:

the second end of the storage component of the first memory cell is connected to the digit line through a first selection component; and

the second end of the storage component of the second memory cell is connected to the plate line through a second selection component.

13. The apparatus of Claim 12, wherein:

the first end of the storage component of the first memory cell is connected to the plate line through a third selection component; and

the first end of the storage component of the second memory cell is connected to the digit line through a fourth selection component.

14. An apparatus, comprising:

a first memory layer;

a second memory layer underlying the first memory layer;

a memory cell including a first storage component in the first memory layer and a second storage component in the second memory layer; and

a set of alternating plate lines and digit lines,

wherein the first storage component includes a first end coupled to a plate line and a second end coupled to a digit line;

the second storage component includes a first end coupled to a plate line and a second end coupled to a digit line;

and the set of plate lines and digit lines includes the digit line of the first storage component and the plate line of the second storage component adjacent to the digit line of the first storage component.

15. The apparatus of claim 14, wherein the memory cell is a first memory cell, the apparatus further comprising:
a second memory cell including a first storage component in the first memory layer and a second storage component in the second memory layer; wherein
the first storage component of the second memory cell includes a first end coupled to a digit line and a second end coupled to a plate line;
the second storage component of the second memory cell includes a first end coupled to a digit line and a second end coupled to a plate line; and
the digit line of the first storage component of the first memory cell is adjacent to the plate line of the first storage component of the second memory cell.
16. The apparatus of Claim 15, further comprising:
a third memory cell including a first storage component in the first memory layer and a second storage component in the second memory layer, wherein:
the first storage component of the third memory cell includes a first end coupled to a digit line and a second end coupled to a plate line;
the second storage component of the third memory cell includes a first end coupled to a digit line and a second end coupled to a plate line; and
the digit line of the first storage component of the first memory cell is adjacent to the plate line of the first storage component of the third memory cell.
17. The apparatus of Claim 14, wherein:
the second end of the first storage component is connected to the digit line through a first selection component; and
the second end of the second storage component is connected to the digit line through a second selection component.
18. The apparatus of Claim 17, wherein:
the first end of the second storage component is connected to the digit line through a third selection component; and
the first end of the second storage component is connected to the digit line through a fourth selection component.