

ABSTRACT OF THE DISCLOSURE

A semiconductor memory device includes a cell array that includes a first row block and a second row block, a bit line sense amplifier block that senses data
5 stored in the first row block or the second row block, a local sense amplifier that latches the sensed data transferred from the bit line sense amplifier block, and a switch that connects the local sense amplifier with a selected one of a first global data line and a second global data line in response to a select signal. The second row block may be placed at an edge of the cell array, and the switch connects the local
10 sense amplifier with the first global data line when the first row block is activated and connects the local sense amplifier with the second global data line when the second row block is activated.

FIG. 2