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"Semiconductor read-only memory"

The present invention relates to a semiconductor read-only memory (hereinafter referred to as a "ROM"), and more particularly to a longitudinal type ROM.

As disclosed in the specification of U.S. Patent No.4,240,151, a longitudinal type ROM constituting a logic block (memory array) comprises a plurality of insulated-gate field effect transistors (hereinafter referred to as "MISFETs") which are connected in series. Each of the plurality of series MISFETs exhibits the depletion mode or the enhancement mode, depending upon the write information.

Amongst the MISFETs connected in series, one which is to be switched and controlled by an input signal exhibits the enhancement mode, and one which is not to be switched and controlled by an input signal exhibits the depletion mode.

The longitudinal type ROM has the following features. The source of one of the MISFETs adjacent to each other and the drain of the other MISFET are electrically connected in common. Accordingly, the source semiconductor region of one MISFET and the drain semiconductor region of the other MISFET which are formed in a single semiconductor substrate by the semiconductor integrated circuit technology can be

constituted by a common semiconductor region. Since the source region and drain region of the adjacent MISFETs can be connected without using an evaporated aluminium interconnection layer, the contact area on the semi-

5 conductor substrate can be reduced. In a semiconductor integrated circuit (IC), accordingly, the ROM can be formed on a comparatively small area. The longitudinal type ROM is suitable especially in the case where the IC is constructed of MISFETs, such as silicon gate MISFETs, in which
10 the source region and the drain region are formed in self-alignment with the gate electrode.

In the longitudinal type ROM, however, it must be remembered that the MISFETs whose number corresponds to the number of input terminals of the ROM are connected in
15 series, so that the "on" resistance value of the entire series connection of the MISFETs becomes comparatively large, and also that parasitic capacitances, which limit the operating speed of the circuit, increase due to an increase in the number of the MISFETs.

20 In a longitudinal type ROM which is employed as an OR array in a PLA (programmable logic array), a comparatively large number of MISFETs are connected in series in correspondence with the number of input terminals of the

ROM. As a result, the "on" resistance value of the whole series connection of the MISFETs becomes comparatively large and the parasitic capacitances increase. When the number of the input terminals to be supplied with address signals has increased in this manner, the speed of reading data is reduced.

By way of example, in order to fabricate a ROM having program addresses of 256 steps, 256 series MISFETs are required.

10 The problem concerning the speed can be solved by the use of a divided type longitudinal ROM which is disclosed in Japanese Laid-open Patent Application No.53-80931. In this ROM, MISFETs to be supplied with input signals are divided into a plurality of groups, and output signals from the serially-connected MISFETs in the respective groups are logically combined by logic circuits. The divided type longitudinal ROM exhibits comparatively-high operating speed characteristics because the number of the MISFETs to be connected in series is reduced.

20 It has been revealed, however, that when the divided type longitudinal ROM is put into the form of an IC, the circuit is liable to malfunction on account of undesirable capacitance coupling between one circuit node and another circuit node.

According to the present invention there is provided a semiconductor read-only memory including

(a) a plurality of first input lines which are supplied with first input signals including a signal which is set
5 at a first level when any of second input signals is not set at the first level in order to bring an enhancement-mode insulated-gate field effect transistor into the "off" state;

(b) a plurality of second input lines which are supplied
10 with said second input signals including a signal which is set at said first level when any of said first input signals is not set at said first level;

(c) a first series circuit which includes a plurality of insulated-gate field effect transistors connected in series
15 between a first output terminal and a first reference potential terminal and with their respective gates coupled to the corresponding first input lines;

(d) a second series circuit which includes a plurality of insulated-gate field effect transistors connected in
20 series between a second output terminal and said first reference potential terminal and with their respective gates coupled to the corresponding second input lines;

(e) first precharge means connected between a second reference potential terminal and said first output terminal and to be maintained in the "on" state when all said first input signals are set at a second level bringing the enhancement-mode insulated-gate field effect transistor into the "on" state; and

(f) second precharge means connected between said second reference potential terminal and said second output terminal which is maintained in the "on" state when all said second input signals are set at said second level.

The present invention will now be described in greater detail by way of example with reference to the accompanying drawings, wherein :-

Figure 1 is a logic circuit diagram showing a known longitudinal type ROM;

Figure 2 is a circuit diagram showing one known example of an output logic circuit for the circuit shown in Figure 1;

Figure 3 is a waveform diagram to assist in the explanation of the circuit shown in Figure 2;

Figure 4 is a logic circuit diagram of a preferred form of semiconductor read-only memory;

Figure 5 is a circuit diagram showing an essential section of the circuit shown in Fig. 4;

Figure 6 is a waveform diagram to assist in the explanation of the circuit shown in Figure 4;

5 Figure 7 is a block circuit diagram showing an example of the application of a semiconductor read-only memory;

Figure 8 is a waveform diagram to assist in the explanation of the circuit shown in Figure 7;

10 Figure 9 is a perspective view of the semiconductor read-only memory; and

Figure 10 is a circuit diagram of an output logic circuit.

Figure 1 shows the logic circuitry of a divided type
15 longitudinal ROM which has been considered in accordance with the idea taught in Japanese Laid-open Patent Application No.53-80931 which facilitates the IC implementation. In order to facilitate understanding of the present invention, the logic circuitry shown in Figure 1 will be
20 described before referring to the semiconductor read-only memory of the present invention.

In Figure 1, a longitudinal type ROM 1 has program addresses of 256 steps as a whole. According to the

concept of the division, the longitudinal type ROM 1 is divided into, for example, a longitudinal type ROM 1a receiving address decode signals $I_0 - I_{127}$ and a longitudinal type ROM 1b receiving address decode signals $I_{128} -$

5 I_{255} . Read signals a and b delivered from the respective divided longitudinal type ROMs 1a and 1b are supplied to a logic circuit 2. A read output signal OUT for all the address decode signals $I_0 - I_{255}$ is formed by a logic circuit 2.

10 In this example of the circuitry, the respective longitudinal type ROMs 1a and 1b include eight column lines $CL_{11} - CL_{18}$ and $CL_{21} - CL_{28}$. Some of the column lines $CL_{11} - CL_{18}$ and $CL_{21} - CL_{28}$ constitute column select portions 1a' and 1b' which receive 3-bit column select

15 signals $\bar{A} - C$ of a true level and a false level.

It should be understood that each of the column lines $CL_{11} - CL_{18}$ in the longitudinal type ROM 1a consists of a plurality of MISFETs whose sources and drains are connected in series and whose gates are respectively supplied with

20 the signals $\bar{A} - C$ and $I_0 - I_{127}$. Likewise, each of the column lines $CL_{21} - CL_{28}$ in the longitudinal type ROM 1b consists of a plurality of MISFETs connected in series. Amongst the MISFETs constituting each column line, those

to be switched and controlled by the input signals exhibit the enhancement mode, and the others exhibit the depletion mode.

Each of the column select portions $1a'$ and $1b'$ has the
5 modes of its MISFETs determined so that, amongst the eight column lines, only one corresponding to the 3-bit column select signal may be selected.

Each of the address decode signals $I_0 - I_{127}$ and
 $I_{128} - I_{255}$ provided from an address decoder (not shown)
10 has its non-selection level set at a level which brings the MISFETs in the column line into their "on" states, and has its selection level set at a level which brings the MISFETs of the enhancement mode in the column line into their "off" state.

15 Since the divided ROMs $1a$ and $1b$ have eight column lines respectively, the longitudinal type ROM shown in Figure 1 has addresses corresponding to 256×8 or 2,048 program steps. By adopting the divided structure and the column selecting structure in this manner, the number of
20 MISFETs which are connected in series within the longitudinal type ROM can be substantially reduced.

The longitudinal type ROM 1 shown in Figure 1 is formed as a ratioless type logic circuit for the following

reason. In the case where logic blocks are constructed of a large number of series MISFETs, it is difficult to properly set the mutual conductance ratio between load means and the series MISFETs. As a result, it becomes
5 difficult to form an output signal of a desired level. Therefore, an output load capacitance (not shown) is pre-charged by precharge MISFETs Q_1 and Q_2 which are switched and controlled by a clock pulse ϕ , whereupon discharge MISFETs (indicated by circles) which are located between
10 the series MISFETs and a supply voltage $-V_{DD}$ are turned "on" by the pulse ϕ . When the discharge MISFETs are turned "on", whether or not charges stored at output points a and b in advance are discharged is determined depending upon the "on" states or "off" states of the series MISFETs.

15 In the case where the IC consists of complementary MISFETs, channel types are selected by way of example so that the precharge MISFETs Q_1 and Q_2 may be of the p-channel type, whilst the series MISFETs including the column select portions and the discharge MISFETs may be of
20 the n-channel type.

The operation of the circuit shown in Figure 1 is as follows in the case where the column select signals $\bar{A} - C$ are set so as to select the column lines CL_{11} and

CL₂₁ and where the address decode signals I₀ - I₂₅₅ are set so as to select the first address input terminal.

First, the clock pulse ϕ is rendered to a low level substantially equal to the supply voltage $-V_{DD}$, whereby the precharge MISFETs Q₁ and Q₂ are brought into the "on" states, with the result that the output points a and b of the longitudinal type ROMs 1a and 1b are precharged substantially to earth potential.

Subsequently, the clock pulse ϕ is rendered to a high level substantially equal to earth potential, whereby the precharge MISFETs Q₁ and Q₂ are brought into the "off" states, and the discharge MISFETs are brought into the "on" states. At this time, the first address decode signal I₀ is at the selection level or the low level substantially equal to the supply voltage $-V_{DD}$, whilst the remaining address decode signals are at the non-selection level or the high level substantially equal to earth potential.

Accordingly, all the MISFETs constituting the column line CL₂₁ are brought into the "on" states even when they exhibit the enhancement mode. As a result, the output point b is discharged to the level approximately equal to the supply voltage $-V_{DD}$ in correspondence with the non-selection level of all the address decode signals I₁₂₈ - I₂₅₅. On the other

hand, when that one of the MISFETs constituting the column line CL_{11} which is supplied with the address decode signal I_0 of the selection level is held in the "off" state by being made the enhancement mode in advance, the output point a is maintained at the precharge level or the high level. In contrast, when the MISFET which receives the address decode signal I_0 of the selection level is made the depletion mode in advance, the output point a is changed to the low level. In other words, in the divided type longitudinal ROMs 1a and 1b, one supplied with the address decode signals of the selection level provides the signal of the high level or low level, and the other not supplied with the address decode signals of the selection level provides the signal of the low level.

The signals delivered to the output points a and b are supplied to the logic circuit 2 which essentially performs an OR operation, and are thus converted into one signal. In the case illustrated, the logic circuit 2 consists of a NAND circuit which receives the low level as the logic level "1".

The logic circuit 2 is shown in greater detail in Figure 2 and consists of a complementary circuit which is clock-driven by sampling pulses ϕ' and $\overline{\phi'}$. When the output

point b is at the low level as stated above, a p-channel MISFET Q_6 is brought into the "on" state and an n-channel MISFET Q_4 into the "off" state by the low level. At this time, when the output point a is at the high level, an n-channel MISFET Q_3 is brought into the "on" state and a p-channel MISFET Q_5 into the "off" state by the high level. As a result, when the MISFETs Q_7 and Q_8 are brought into the "on" states by the sampling pulses ϕ' and $\overline{\phi'}$, the output OUT is at the low level.

10 When a data signal or control signal of a plurality of bits needs to be provided from one address, the circuits as shown in Figure 1 are juxtaposed.

15 In the case of putting the circuit of Figure 1 into the form of an IC, the logic circuit 2 is located outside the ROMs 1a and 1b as in the circuit arrangement of Figure 1 with a view to shortening the interconnection to another circuit which receives the output thereof.

20 In the case where the logic circuit 2 is arranged outside the longitudinal type ROM 1a, the output line of the longitudinal type ROM 1b is extended above the column lines of the longitudinal type ROM 1a and then coupled with one input terminal of the logic circuit 2.

In such a divided type longitudinal ROM, however, an undesirable coupling capacitance (not shown) of a comparatively large value is formed between the output line of the longitudinal type ROM 1b and a specified column of the longitudinal type ROM 1a. For example, in the case where the output line of the longitudinal type ROM 1b is arranged in proximity to the column line CL_{16} of the longitudinal type ROM 1a, a coupling capacitance of comparatively large value is formed therebetween. Such coupling capacitance can cause the circuit of Figure 1 to malfunction.

By way of example, when the output point a of the longitudinal type ROM 1a ought to be at the high level by the specified column line CL_{16} , the situation is as follows.

In the case where the discharge operation has been initiated after the precharge operation, the output point b is changed to the low level approximately equal to the supply voltage $-V_{DD}$ as previously described because all the address decode signals $I_{128} - I_{255}$ are made the non-selection level. At this time, on account of the comparatively large coupling capacitance between the output point b or the output line of the longitudinal type ROM 1b and the column line CL_{16} , the potential of the column line CL_{16} is undesirably changed toward the low level as indicated

by a broken line in waveform B of Figure 3. During the period of the discharge operation, the precharge MISFET Q_1 is held in the "off" state, so that the output point a is held in its high impedance state. Accordingly, the

5 potential of the column line CL_{16} or the output point a lowered through the coupling capacitance is maintained at the lowered level until the precharge operation is started again. When the potential of the output point a has been lowered beyond the logic threshold voltage of the logic
10 circuit 2, a signal of an erroneous level or the high level is provided from the logic circuit 2 in response thereto.

The coupling capacitance is changed depending upon which of the address decode signals $I_0 - I_{127}$ is made the selection level.

15 In order to prevent the formation of the undesirable coupling capacitance as above described the logic circuit 2 is arranged in the intermediate area between the divided longitudinal type ROMs 1a and 1b. In such a case, note must be taken of the following.

20 In order to supply the output signal of the logic circuit 2 to another circuit arranged around the longitudinal ROM 1a or 1b, the output line of the logic circuit 2 needs to be extended above, for example, the ROM 1a or

ROM 1b. Therefore, a coupling capacitance similar to the foregoing is formed, and crosstalk results due to the malfunction of the circuit. On the other hand, it is possible to supply the output signal of the logic circuit arranged
5 between the longitudinal type ROMs 1a and 1b, to another circuit through a detour interconnection. In this case, however, a sufficient area for forming the detour interconnection must be secured between and around the longitudinal type ROMs 1a and 1b. As a result, the occupying area of a
10 monolithic IC chip must be increased.

In the case where the longitudinal type ROM is divided into three or more parts, the formation of the logic circuits amongst the divided longitudinal type ROMs as described above has no special significance in the decrease of the
15 coupling capacitance or the reduction of the detour interconnection area as described above.

In the case where the longitudinal type ROM is formed of complementary MISFETs as described above and where the logic circuit 2 is arranged around the divided longitudinal type ROMs 1a and 1b, a plurality of n-channel MISFETs constituting the longitudinal type ROMs 1a and 1b can be formed
20 within an identical p-type well region. As a result, the

density of integration of the IC can be enhanced.

According to the present invention, the precharge operation and discharge operation in the divided type longitudinal ROM are controlled by the control signal such as an address signal. During a discharge period or sampling period the output level of one of the plurality of divided longitudinal ROMs is changed depending upon the input signals thereof and the modes of the MISFETs included therein. The output level of any other divided longitudinal ROM is not changed by the control of the precharge operation. As a result, any erroneous circuit operation does not occur even in the presence of the undesirable coupling capacitance as mentioned above.

Referring now to Fig. 4, a longitudinal type ROM 1 is divided into two longitudinal ROMs 1a and 1b which include column select portions 1a' and 1b' respectively.

The divided longitudinal ROMs 1a and 1b include eight column lines $CL_{11} - CL_{18}$ and $CL_{21} - CL_{28}$, respectively.

The longitudinal ROM 1a is supplied with 3 bits of column select signals $\bar{A} - C$ having the true level and false level, and 128 bits of address decode signals $I_0 - I_{127}$ formed by an address decoder (not shown). Similarly the longitudinal ROM 1b is supplied with 3 bits of column select

signals $\bar{A} - C$ and 128 bits of address decode signals $I_{128} - I_{255}$.

Each of the column lines $CL_{11} - CL_{18}$ and $CL_{21} - CL_{28}$ consists of a plurality of MISFETs whose sources and drains
5 are connected in series.

Those serially-connected MISFETs in the longitudinal ROM $1a$ which are supplied with the address decode signals $I_0 - I_{127}$, and those serially-connected MISFETs in the longitudinal ROM $1b$ which are supplied with the address decode signals $I_{127} - I_{255}$ essentially constitute memory arrays.
10

Discharge means comprising n-channel type MISFETs (indicated by circles in Figure 4) are located between each of the longitudinal ROMs $1a$ and $1b$ and a supply voltage terminal $-V_{DD}$.

15 In addition, precharge means comprising p-channel type MISFETs Q_1 and Q_2 are respectively located between the column select portions $1a'$ and $1b'$ and a reference potential terminal at zero volts or earth potential.

Figure 5 shows a circuit of one column line of the longitudinal ROM $1a$, for example the column line CL_{11} .
20

The column line shown in Figure 5 comprises a series connection which consists of 6 n-channel type MISFETs $Q_{11} - Q_{16}$ constituting the column select portion, 128 n-channel type

MISFETs $Q_{17} - Q_{144}$ constituting the memory array, and a discharge MISFET Q_{145} . The precharge MISFET Q_1 of the p-channel type is connected between the column line and the reference potential terminal at zero volts, whilst the discharge MISFET Q_{145} is connected between the column line and the supply voltage terminal $-V_{DD}$.

The MISFETs such as the MISFET Q_{12} in which straight lines are drawn across their sources and drains exhibit the depletion mode. The other MISFETs exhibit the enhancement mode.

In the circuit of Figure 5, the serially-connected MISFETs $Q_{11} - Q_{16}$ constituting the column select portion 1a' have their modes determined as follows.

In the case of employing the column select signals A, $\bar{A} - C$, $\bar{C}$ corresponding to 3 bits of binary data $2^0 - 2^2$, in order to decode the first status of the column select signals A, $\bar{A} - C$, $\bar{C}$, the MISFETs Q_{11} , Q_{13} and Q_{15} (not shown) which receive the signals $\bar{A}$, $\bar{B}$, and $\bar{C}$ of the false level exhibit the enhancement mode, and the MISFETs Q_{12} , Q_{14} (not shown) and Q_{16} which receive the signals A, B and C of the true level exhibit the depletion mode. Accordingly, when the signals $\bar{A}$, $\bar{B}$ and $\bar{C}$ are at the high level, i.e., when the 3-bit binary data are put into the first status, the MISFETs Q_{11} ,

Q_{13} and Q_{15} are brought into their "on" states. As a result the first column line is coupled to the output point a.

If the second column line consists of the MISFETs $Q_{17} - Q_{144}$ in Figure 5, the MISFETs Q_{12} , Q_{13} and Q_{15} receiving the signals A , $\bar{B}$ and $\bar{C}$ exhibit the enhancement mode and the remaining MISFETs Q_{11} , Q_{14} and Q_{16} exhibit the depletion mode so as to decode the second status of the column select signals A , $\bar{A} - C$, $\bar{C}$. Likewise, if the eighth column line is constructed of the MISFETs $Q_{17} - Q_{144}$, the MISFETs Q_{12} , Q_{14} and Q_{16} receiving the signals A , B and C exhibit the enhancement mode and the remaining MISFETs exhibit the depletion mode so as to decode the eighth status of the column select signals A , $\bar{A} - C$, $\bar{C}$.

The MISFETs $Q_{17} - Q_{144}$ which constitute the memory array are set to exhibit the depletion mode or the enhancement mode in accordance with the write information.

The MISFETs Q_{17} , Q_{19} , Q_{22} and Q_{23} exhibit the enhancement mode, and the remaining MISFETs exhibit the depletion mode. That is, in the column of Figure 5, the MISFETs corresponding to addresses 0, 2, 5 and 6 exhibit the enhancement mode. Accordingly, when the column shown in Figure 5 is selected in correspondence with the first status of the column select signals A , $\bar{A} - C$, $\bar{C}$ and the address 0, 2, 5

or 6 is selected by the selection level (low level) of the address decode signal I_0 , I_2 , I_5 or I_6 , one of the enhancement mode MISFETs is responsively brought into the "off" state. In this case, the output a is set to the high level.

5 When any address other than the above referred to addresses is selected, the address decode signals I_0 , I_2 , I_5 and I_6 are set to the non-selection level (high level), whereby the MISFETs Q_{17} , Q_{19} , Q_{22} and Q_{23} are brought into the "on" states. Therefore, the output a is set to the low level.

10 Since the discharge MISFET Q_{145} needs to perform the switching operation, it is constructed to exhibit the enhancement mode.

The longitudinal ROM 1b is constructed in similar manner. It comprises divided longitudinal ROMs 1a and 1b
15 which provide a signal of 1 bit in response to an input address signal. Accordingly, a plurality of such longitudinal type ROMs 1 are arranged in parallel in order to provide from one address a predetermined program instruction constituting a plurality of bits.

20 The longitudinal type ROM described above can be formed on a single semiconductor substrate by the known semiconductor integrated circuit (IC) technology.

The p-channel type MISFETs are formed in the surface of a semiconductor substrate which is made of n-type single crystal silicon, and the n-channel type MISFETs are formed in the surface of a p-type well region which is
5 formed in the surface of the semiconductor substrate.

The p-channel type and n-channel type MISFETs are formed so as to have gate electrodes which are made of, for example, polycrystalline silicon layers. The source region and drain region of each MISFET are formed by the self-
10 alignment technique in which the corresponding gate electrode is utilized as a mask.

Figure 9 shows a partially sectional and broken perspective view of the MISFETs constituting the longitudinal ROM 1a. As shown a p-type well region 11 is formed in the
15 surface of an n-type semiconductor substrate 10. A field oxide film 12 of a comparatively great thickness of, e.g. approximately 1 μm is formed on the surface of the p-type well region 11 by a known selective thermal oxidation technique. A gate oxide film 13 of a comparatively small
20 thickness of, e.g. approximately 500 $\text{\AA}$ is formed on the surface of the p-type well region 11 not covered with the field oxide film 12, that is, the surface corresponding to an active region. A plurality of n-type polycrystalline

silicon layers 15a - 15e which constitute the input lines of the ROM and the gate electrodes of the MISFETs are extended on the field oxide film 12 and the gate oxide film 13.

5. In the surface of the p-type well region 11 covered with neither the field oxide film 12 nor the polycrystalline silicon layers 15a - 15e, there are formed n-type semiconductor regions 141a - 141e, 142a and 143a which function as the source regions and drain regions of the MISFETs.

10 The n-type semiconductor regions are formed by a known self-alignment technique in which the field oxide film 12 and the polycrystalline silicon layers are used as a mask for implanting the ions of an n-type impurity.

As will be seen from Figure 9, one of the plurality
15 of MISFETs constituting the column line CL₁₈ is formed from the n-type semiconductor regions 141a and 141b, the gate oxide film 13 and the n-type polycrystalline silicon layer 15a.

The MISFET in which an n-type semiconductor region
20 18 is formed in the surface of the p-type well region 11 underlying the gate electrode 15b exhibits the enhancement mode. The n-type semiconductor region 18 is formed by an ion implantation technique. After forming the gate oxide

film 13, a photoresist film is formed on the surface of the semiconductor substrate. Subsequently, the photoresist film is removed from parts which are to form the channel regions of the depletion mode MISFETs. At the next step, using the photoresist film as a mask, n-type impurity ions such as phosphorus ions are implanted into the surface of the p-type well region 11 through the gate oxide film 13. As a result, the n-type semiconductor region 18 is formed.

In the longitudinal type ROM, the depletion mode MISFET is not utilized as a switching element, but is utilized as the cross interconnection between the input line such as the polycrystalline silicon layer and the column line. In the case where the depletion mode MISFET is utilized as the cross interconnection in the above manner, it can be made the same size as that of the enhancement mode MISFET and does not require any special contact region, so that the arrangement of the MISFETs of the matrix arrangement in Figure 9 is facilitated.

An insulating film 16 of comparatively great thickness which is made of phosphosilicate glass and which serves as the interlayer insulating film of multilayer interconnections, is formed on the surface of the semiconductor substrate including the surfaces of the polycrystalline silicon

layers. An interconnection layer 17 which is made of evaporated aluminium is formed on the surface of the insulating film 16.

5 The interconnection layer 17 is used as the output interconnection of the longitudinal ROM 1b shown in Figure 4. The interconnection layer 17 is extended substantially on the field oxide film 12. That is, the interconnection layer 17 is extended so as to avoid positions over the MIS-FET forming regions to the utmost. Since, however, the
10 interconnection layer 17 is comparatively near to the column lines CL_{16} and CL_{17} , it forms unnegligible coupling capacitances with these column lines. With a view to reducing the coupling capacitances, that part of the field oxide film 12 on which the interconnection layer 17 is to be
15 extended can be widened. This measure, however, results in lowering the density of integration of the longitudinal ROM 1a.

In order to prevent any malfunction attributed to the coupling capacitances as stated above, clock pulses $\bar{\phi}$ are
20 applied to the respective precharge MISFETs Q_1 and Q_2 and discharge MISFETs of the longitudinal ROMs 1a and 1b through gate circuits G_1 and G_2 .

As shown in Figure 4, each of the gate circuits G_1 and G_2 is a 2-input NAND circuit. One input terminal of each of the gate circuits G_1 and G_2 is supplied with the clock pulse $\bar{\phi}$, whilst the other input terminals of the respective gate circuits G_1 and G_2 are supplied with gate control signals $\overline{A_7}$ and A_7 .

The gate control signal $\overline{A_7}$ is brought into its low level or negative logic level "1" in response to the fact that one of the address decode signals $I_0 - I_{127}$ is made the selection level or the low level substantially equal to the supply voltage $-V_{DD}$. On the other hand, the gate control signal A_7 is brought into its ~~high~~^{low} level in response to the fact that one of the address decode signals $I_{128} - I_{255}$ is made the selection level.

Accordingly, the gate control signals $\overline{A_7}$ and A_7 can be made coincident with the address input signal of the most significant bit which is applied to the address decoder circuit (not shown) for forming the 256 kinds of address decode signals $I_0 - I_{255}$.

As illustrated/waveform D of Figure 6, clock pulses ϕ_a which are output from the gate G_1 constitute a signal which is opposite in phase to the clock pulses $\bar{\phi}$ in the period of the low level of the gate control signal $\overline{A_7}$ and which is

maintained at the low level irrespective of the changes of the clock pulses ϕ during the period of the high level of the gate control signal $\overline{A_7}$. Likewise, clock pulses ϕ_b which are output from the gate circuit G_2 are changed according to the changes of the clock pulses ϕ in only the period of the low level of the gate control signal A_7 as illustrated in waveform E of Figure 6.

Owing to the provision of the gate circuits G_1 and G_2 , the operations of the longitudinal ROMs $1a$ and $1b$ are as follows.

When any of the address decode signals $I_0 - I_{127}$ is made the selection level by the address decoder circuit (not shown) the gate control signal $\overline{A_7}$ is brought into the low level as shown in waveform A of Figure 6, so that the clock pulse ϕ_a is changed in correspondence with the clock pulse ϕ .

When the clock pulse ϕ_a is held at the low level approximately equal to the supply voltage $-V_{DD}$, the pre-charge MISFET Q_1 is correspondingly held in the "on" state. Accordingly, the output point a of the longitudinal ROM $1a$ is precharged substantially to earth potential.

When the clock pulse ϕ_a is brought to the high level approximately equal to earth potential, the precharge

MISFET Q_1 is correspondingly brought into the "off" state, and the discharge MISFET Q_{145} is brought into the "on" state. As a result, the potential of the output point a is at a value which is determined by the arrangement of the memory array.

During the period in which the gate control signal $\overline{A_7}$ is held at the low level, the gate control signal A_7 is held at the high level as illustrated in waveform B of Figure 6. The clock pulse ϕ_b is maintained at the low level irrespective of the level change of the clock pulse $\overline{\phi}$. Since the precharge MISFET Q_2 is held in the "on" state by the clock pulse ϕ_b of the low level, the output line of the longitudinal ROM 1b is maintained at the precharge level or earth potential.

Since the output line of the longitudinal ROM 1b is maintained at the precharge level, the output point of the longitudinal ROM 1a is not subject to any noise which could undesirably lower its level.

In the case where the circuit arrangement as shown in Figure 4 is not conformed with, a potential change in the predetermined column line of the longitudinal ROM 1a is given to the output line of the longitudinal ROM 1b through the undesirable coupling capacitance.

In contrast, the circuit arrangement shown in Figure 4 is provided with the gate circuit G_1 as described above, so that the clock pulse ϕ_a is maintained at the low level when any of the address decode signals $I_{128} - I_{255}$ is set at the selection level.

Thus, when any of the address decode signals $I_{128} - I_{255}$ is selected, the output line of the longitudinal ROM $1a$ is maintained at the precharge level. As a result, the output line of the longitudinal ROM $1b$ does not receive any noise which could undesirably lower its level.

Since, in the circuit arrangement shown in Figure 4, the output level of one of the longitudinal ROMs $1a$ and $1b$ is maintained at the precharge level or high level, the logic circuit 2 is a 2-input NOR circuit which regards the high level input as the negative logic level "0". A preferred form of the negative logic NOR circuit is shown in Figure 10.

This NOR circuit consists of n-channel type MISFETs Q_3' , Q_4' and Q_7 which are connected in series between a supply voltage terminal $-V_{DD}$ and an output terminal OUT, and p-channel type MISFETs Q_8 , Q_5' and Q_6' which are connected between the output terminal OUT and earth.

The gates of the MISFETs Q_7 and Q_8 are respectively supplied with sampling pulses ϕ' and $\overline{\phi'}$.

The preferred form of logic circuit shown in Figure 10 has the following advantages.

5 The rate of change of an output signal at the output terminal OUT is limited by capacitances (not shown) such as stray capacitances coupled to the output terminal, and the "on" resistances of the switching MISFETs. In the case where all the MISFETs shown in Figure 10 have equal "on" resistances, the changing rate of the output signal from the high level (zero volts) to the low level ($-V_{DD}$) is greatly limited because the three MISFETs Q_3' , Q_4' and Q_7 are connected between the supply voltage terminal $-V_{DD}$ and the output terminal OUT and the two MISFETs Q_8 and Q_5' or 10 Q_8 and Q_6' are connected between the output terminal OUT and earth. In this respect, in order to increase the changing rate of the output signal from the high level to the low level, the "on" resistances of the MISFETs Q_3' , Q_4' and Q_7 need to be small in comparison with those of 15 the MISFETs Q_8 , Q_5' and Q_6' . 20

As is well known, the "on" resistance of a MISFET is proportional to the ratio W/L between the channel width W and channel length L thereof. In general, the channel

length L of the MISFET designed as part of an IC has its lower limit determined by the dimensional accuracy which can be achieved in the manufacture thereof. Accordingly, for a MISFET to exhibit a lower "on" resistance it must have a large channel width W which means that it will occupy a comparatively large area. Since an n-channel type MISFET has a comparatively great mobility for electrons, it exhibits a low "on" resistance as compared with a p-channel type MISFET even when made comparatively small in size.

10 In the circuit shown in Figure 10, the MISFETs Q_3' , Q_4' and Q_7 whose "on" resistances need to be especially low are of the n-channel type. Accordingly, the area on a semiconductor substrate for forming the MISFETs may be comparatively small.

15 In the known circuit shown in Figure 2, the MISFETs Q_8 , Q_5 and Q_6 whose "on" resistances need to be especially small are made the p-channel type. Accordingly, a comparatively large area of the semiconductor substrate is required for forming the MISFETs.

20 In the circuit arrangement shown in Figure 4, either one of the clock pulses ϕ_a and ϕ_b is maintained at the low level, whereby the discharge MISFETs in one of the

longitudinal ROMs 1a and 1b are held in the "off" states. That is, the discharge operation in one of the longitudinal ROMs 1a and 1b is inhibited. As a result, a reduction in the power dissipation of the circuit can be achieved together with the prevention of any malfunction as referred to above.

Figure 7 is a block diagram showing an embodiment in the case where the semiconductor read-only memory has been applied to a digital control circuit.

Unlike the circuit of the so-called static logic system wherein random logic circuits which are arranged individually in correspondence with various functions are used to execute the respective information processing operations as predetermined, the digital control circuit of this embodiment is a circuit of the so-called dynamic logic system (PLA or ROM-RAM system) wherein control instructions written in a ROM are successively read out to operate the circuit which is used in common for the various operations.

The digital control circuit includes a longitudinal type ROM 1. The ROM 1, in similar manner to those described above, consists of longitudinal ROMs 1a and 1b including column select portions 1a' and 1b' respectively, and a precharging circuit 1c. A plurality of program

instructions each having m bits are stored in the ROM 1.

Each of the longitudinal ROMs la and lb has 128 addresses.

Each of the column select portions la' and lb' receives 3 bits of column select signals. Accordingly, the longitudinal type ROM 1 has $(128 \times 2^3) \times 2$ or 2,048 program addresses.

A gate circuit G_1 is arranged in order to control the precharge operation and discharge operation, i.e., the sampling operation of the divided longitudinal ROM la . Likewise, a gate circuit G_2 is arranged in order to control the operation of the longitudinal ROM lb . Essentially, one gate circuit suffices for each of the gate circuits G_1 and G_2 . However, if necessary for driving precharge MISFETs and discharge MISFETs at high speed, a plurality of gate circuits for delivering the same signal may well be arranged so as to reduce the number of MISFETs which one gate circuit is to drive.

Output signals from the divided ROMs la and lb are supplied to a logic circuit 2. Accordingly, the program instruction word consisting of m bits is provided from the logic circuit 2.

The digital control circuit also includes an address decoder circuit 3 (or AND array). The address decoder circuit 3 decodes 8 bits of address signals $A_0, \overline{A_0} - A_7, \overline{A_7}$

delivered from a program counter 4, and thereby provides address decode signals to be supplied to the divided longitudinal ROMs 1a and 1b.

The address decoder circuit 3 substantially consists of a longitudinal ROM. Serially-connected MISFETs (not shown) which are supplied with the 8 bits of address signals $A_0, \overline{A_0} - A_7, \overline{A_7}$ either exhibit the enhancement mode or the depletion mode, whereby the selection level of the address decode signal is made a low level and the non-selection level a high level. In this case, a clock pulse ϕ_0 for operating the address decoder circuit 3, a clock pulse $\overline{\phi}$ for operating the longitudinal ROM 1 and sampling pulses ϕ' and $\overline{\phi'}$ for operating the logic circuit 2 have the waveforms shown in respective waveforms A to D of Figure 8 in order to effect appropriate operation of the circuit.

By making the clock pulse ϕ_0 the low level at a time t_{10} , the precharge operation of the address decoder circuit 3 is started. The clock pulse $\overline{\phi}$ to be supplied to the gate circuits G_1 and G_2 is set to the high level at the same time t_{10} . Accordingly, the precharge operation of the ROM 1 is also started at the time t_{10} .

By setting the clock pulse ϕ_0 to the high level at a time t_{11} , the discharge operation of the address decoder circuit 3 is started.

At a time t_{12} when the discharge operation of the address decoder circuit 3 has been substantially completed, that is, when one of the address decode signals has been set to the high level, the clock pulse $\bar{\phi}$ is set the low level,

5 As a result, the discharge operation of the ROM 1 is started.

At a time t_{13} when the discharge operation of the ROM 1 has been substantially completed the sampling pulses ϕ' and $\bar{\phi}'$ are set to the low level and the high level respectively.

As a result, signals which correspond to signals provided
10 from the ROM 1 are output from the logic circuit 2.

At a time t_{14} , the clock pulses ϕ_0 and $\bar{\phi}$ are respectively set to the low level and the high level again.

Accordingly, the precharge operations of the address decoder circuit 3 and the ROM 1 are started. The output signals of
15 the logic circuit 2 are held by capacitances existing at the corresponding output terminals until the sampling is started again.

The program counter 4 includes a portion 4a for holding 3 bits of address signals, and a portion 4b for
20 holding 8 bits of address signals. The 3 bits of address signals are directly supplied to the column select portions 1a' and 1b' of the respective longitudinal ROMs 1a and 1b as the column select signals. The 8 bits of address signals

are supplied to the address decoder circuit 3.

The digital control circuit also includes an information processing circuit 5 which receives the program instruction of m bits output from the logic circuit 2. The information processing circuit 5 includes : an instruction decoder circuit which decodes the instruction word to form firstly control signals required for a predetermined information processing operation, and secondly increment and jump control signals for the program counter; a RAM (random access memory) for holding data; a logic-arithmetic unit; a number of registers; and an input/output circuit (none of which are shown). It executes the predetermined information processing operation in accordance with the instruction words of the ROMs 1a and 1b.

It should be noted that whilst the longitudinal type ROM has been described as the complementary type circuit, it may well be constructed of only p-channel MISFETs or only n-channel MISFETs.

Moreover, the logic circuit 2, and the gate circuits G_1 and G_2 can be replaced with AND and OR circuits, depending upon signal levels.

The column select portions may well be omitted, and the ROM may well be divided into three or more parts.

In the logic circuit as shown in Figure 8, when the signals a and b are changed at a comparatively low speed, the p-channel MISFETs and the n-channel MISFETs are simultaneously brought into the "on" states. Unless the MISFETs

5 Q_7 and Q_8 are provided, this will result in causing a penetrating current to flow across the supply voltage terminals. Therefore, the circuit of Figure 10 includes the MISFETs Q_7 and Q_8 to be driven by the pulses ϕ' and $\overline{\phi'}$ in spite of being constructed of the CMOS circuit which has the
10 feature that direct current becomes substantially zero.

However, when the penetrating current may be neglected, the MISFETs Q_7 and Q_8 can be omitted. In this case, the output of the circuit of Figure 10 may be held by an appropriate sample-and-hold circuit such as flip-flop circuit.



CLAIMS :

1. A semiconductor read-only memory including :

(a) a plurality of first input lines which are supplied with first input signals including a signal which is set at a first level when any of second input signals is not set at the first level in order to bring an enhancement-mode insulated-gate field effect transistor into the "off" state;

(b) a plurality of second input lines which are supplied with said second input signals including a signal which is set at said first level when any of said first input signals is not set at said first level;

(c) a first series circuit which includes a plurality of insulated-gate field effect transistors connected in series between a first output terminal and a first reference potential terminal and with their respective gates coupled to the corresponding first input lines;

(d) a second series circuit which includes a plurality of insulated-gate field effect transistors connected in series between a second output terminal and said first reference potential terminal and with their respective gates coupled to the corresponding second input lines;



(e) first precharge means connected between a second reference potential terminal and said first output terminal and to be maintained in the "on" state when all said first input signals are set at a second level bringing the enhancement-mode insulated-gate field effect transistor into the "on" state; and

(f) second precharge means connected between said second reference potential terminal and said second output terminal which is maintained in the "on" state when all said second input signals are set at said second level.

2. A semiconductor read-only memory according to claim 1, further including :

(g) a third output terminal; and

(h) a logic circuit which logically combines a signal delivered to said first output terminal and a signal delivered to said second output terminal, in order to deliver a signal to said third output terminal.

3. A semiconductor read-only memory according to claim 2, wherein said first precharge means includes a first insulated-gate field effect transistor which is connected between said second reference potential terminal and said first output terminal, and a first gate circuit which



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supplies a clock pulse to a gate of said first insulated-gate field effect transistor; and wherein said second pre-charge means includes a second insulated-gate field effect transistor which is connected between said second reference
5 potential terminal and said second output terminal, and a second gate circuit which supplies a clock pulse to a gate of said second insulated-gate field effect transistor.

4. A semiconductor read-only memory according to claim 3, wherein said first series circuit includes a third
10 insulated-gate field effect transistor which is turned "on" and "off" in complementary manner to said first insulated-gate field effect transistor; and wherein said second series circuit includes a fourth insulated-gate field effect transistor which is turned "on" and "off" in comple-
15 mentary manner to said second insulated-gate field effect transistor.

5. A semiconductor read-only memory according to claim 4, wherein said insulated-gate field effect transistors constituting said first and second series circuits are of a
20 first conductivity type, and said first and second insulated-gate field effect transistors are of a second conductivity type.

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6. A semiconductor read-only memory according to claim 5, wherein said logic circuit has its operation controlled by a clock pulse.

5 7. A semiconductor read-only memory according to claim 4, further including a decode circuit which forms said first and second input signals by decoding binary signals of a plurality of bits.

10 8. A semiconductor read-only memory according to claim 7, wherein each of said first and second gate circuits receive firstly as a gate control signal a binary signal supplied to said decode circuit, and secondly a clock pulse.

15 9. A semiconductor read-only memory according to claim 4, wherein said circuits are formed on a single semiconductor substrate, and said second series circuit is connected to said second output terminal through an interconnection layer which is extended on an area forming said insulated-gate field effect transistors constituting said first series circuit.

20 10. A semiconductor read-only memory according to claim 9, wherein each of said first and second series circuits includes at least a first circuit which is formed from a plurality of insulated-gate field effect transistors connected in series, and a second circuit which is formed from a



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plurality of insulated-gate field effect transistors connected in series and which is connected in parallel with said first circuit.

11. A semiconductor read-only memory constructed substantially as herein described with reference to and as
5 illustrated in Figures 4 to 10 of the accompanying drawings.

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