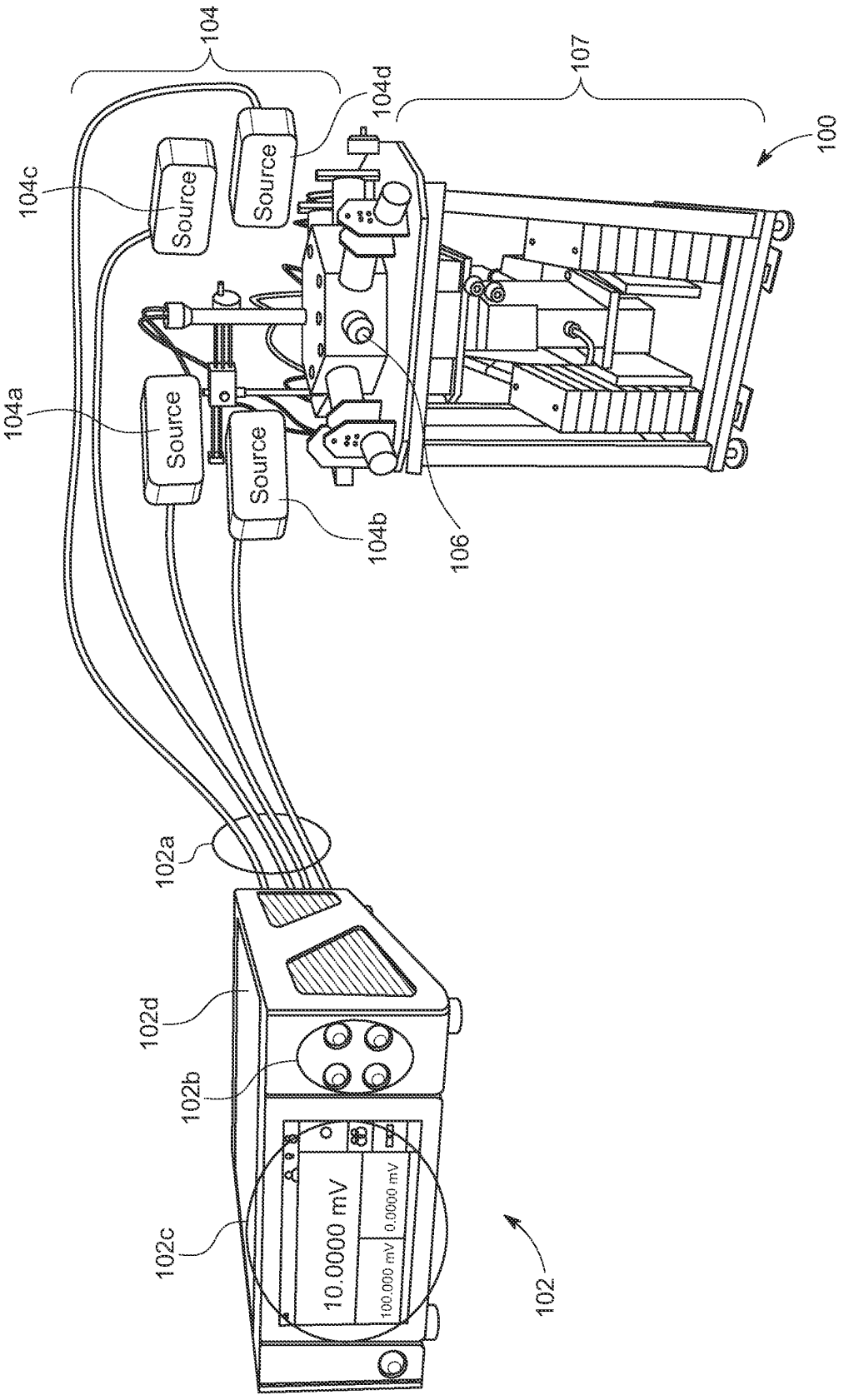

104
107
104d
100
104c
Source
Source
104a
Source
Source
104b
106
102a
102d
102b
102c
10.0000 mV
0.0000 mV
100.000 mV
102

FIG. 1

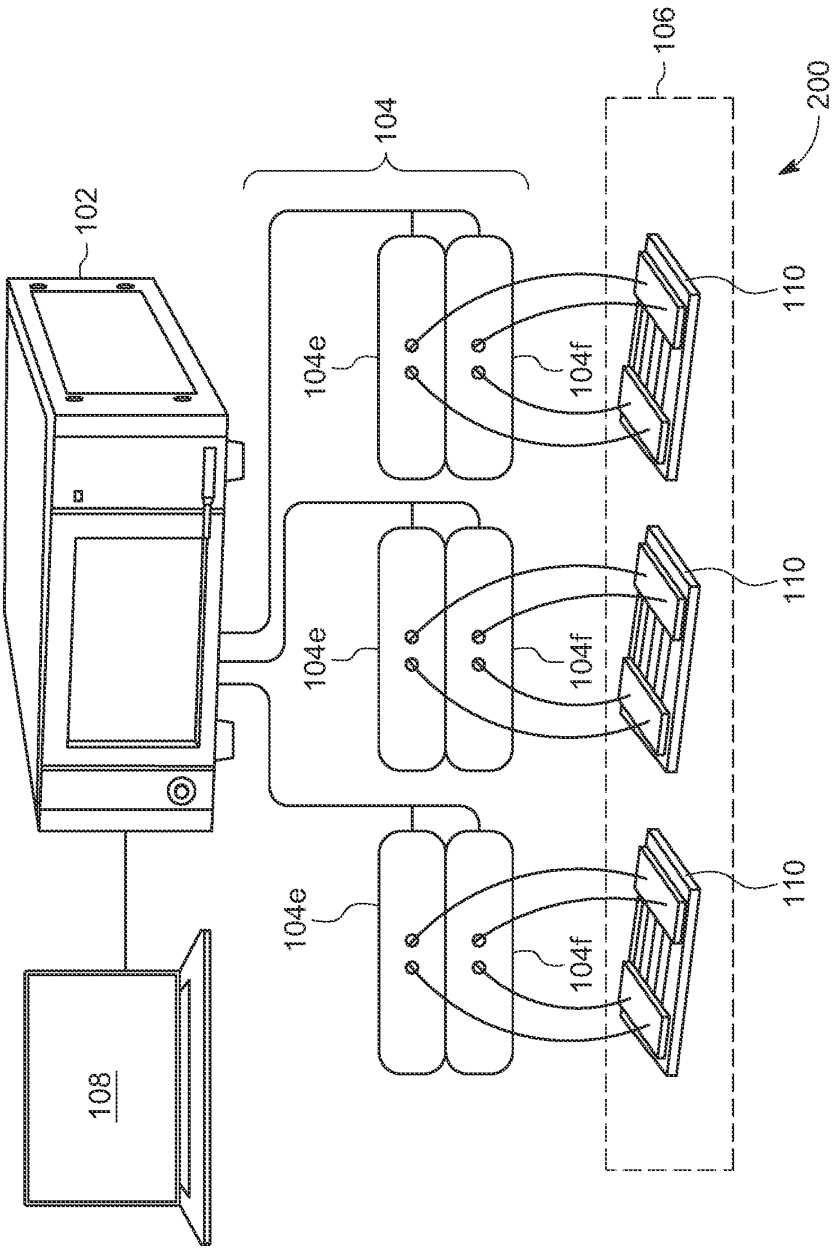


FIG. 2

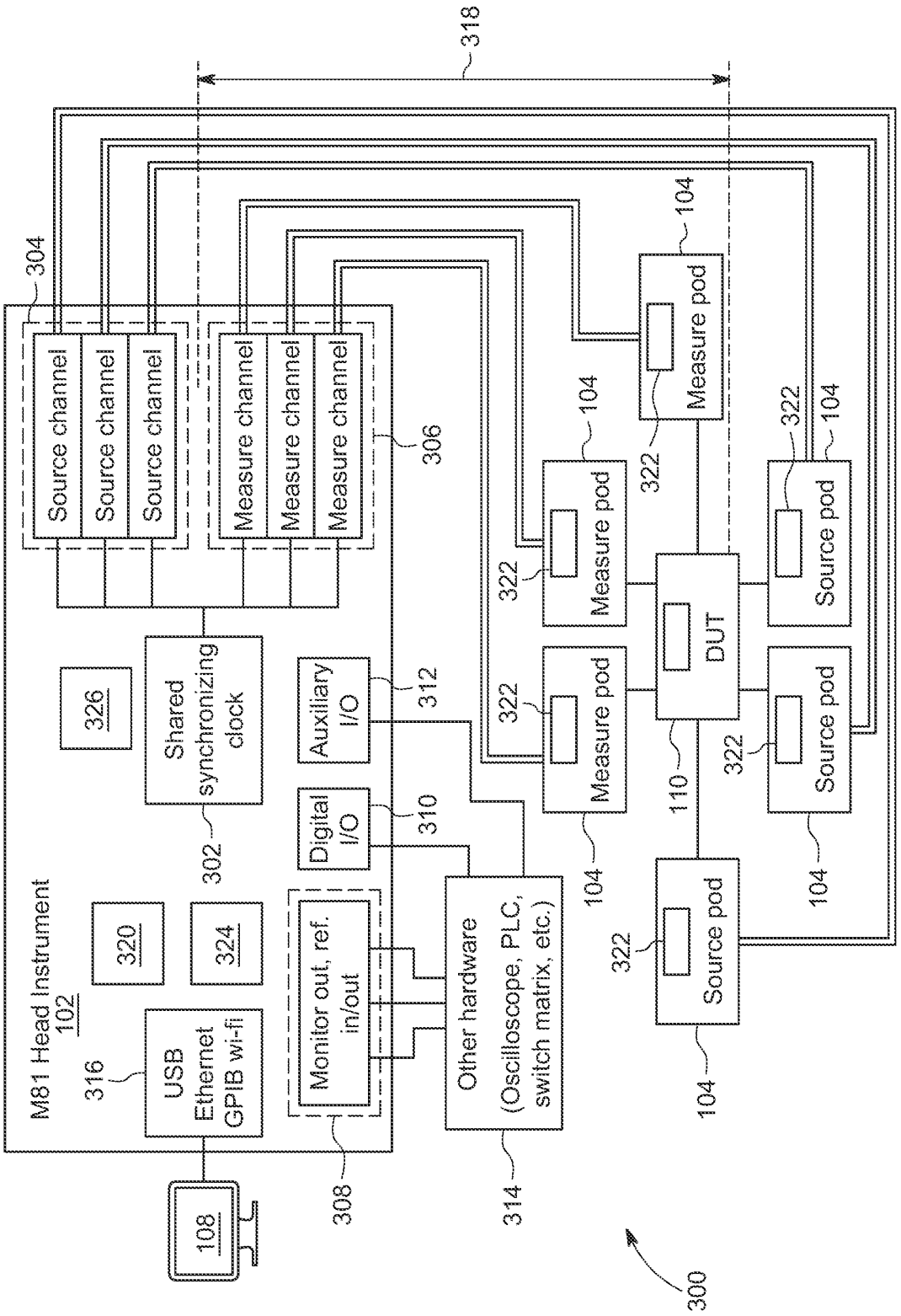

318
304
Source channel
Source channel
Source channel
Measure channel
Measure channel
Measure channel
306
326
Shared synchronizing clock
302
Auxiliary I/O
312
Digital I/O
310
M81 Head Instrument
102
320
324
316
USB
Ethernet
GPIB wi-fi
108
Monitor out, ref. in/out
308
Other hardware
(Oscilloscope, PLC, switch matrix, etc.)
314
104
Measure pod
322
DUT
110
Source pod
300

FIG. 3A

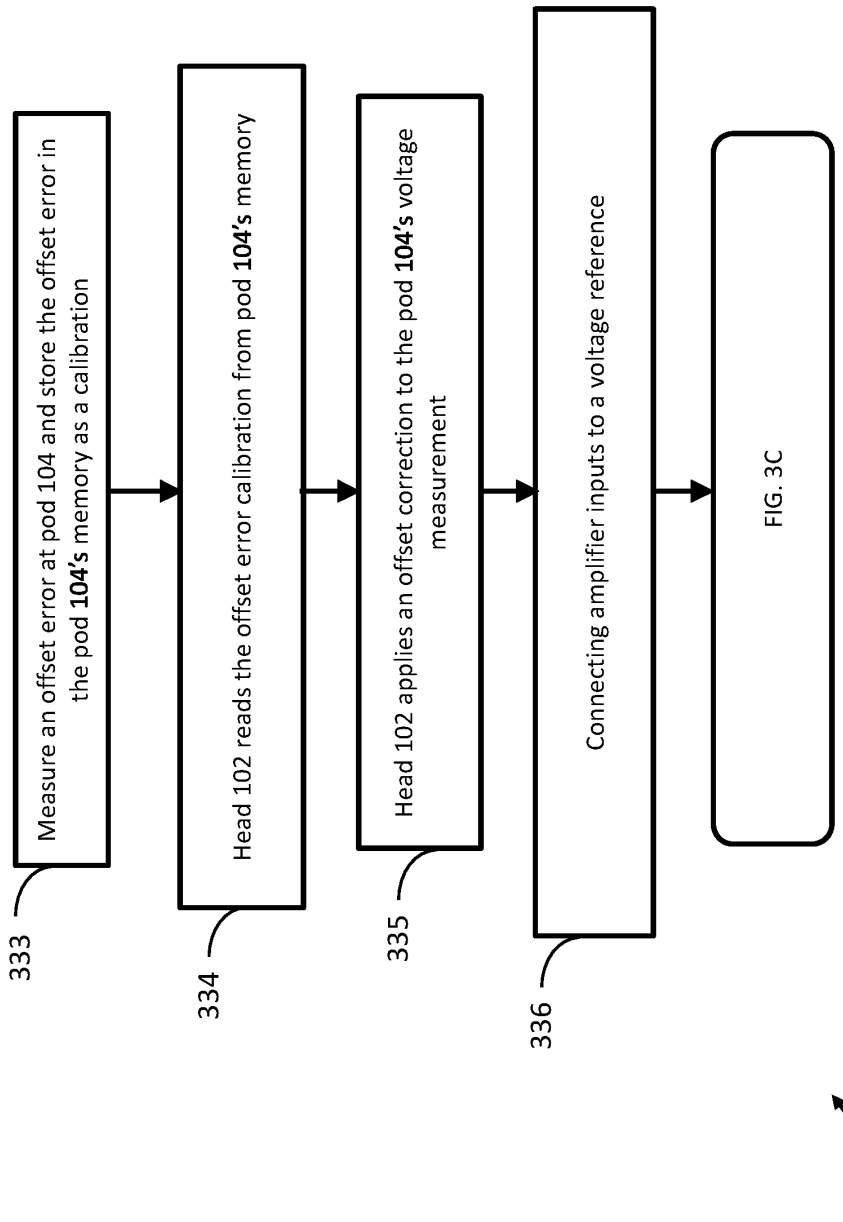

Measure an offset error at pod 104 and store the offset error in the pod 104's memory as a calibration
Head 102 reads the offset error calibration from pod 104's memory
Head 102 applies an offset correction to the pod 104's voltage measurement
Connecting amplifier inputs to a voltage reference
FIG. 3C
333
334
335
336
330

FIG. 3B

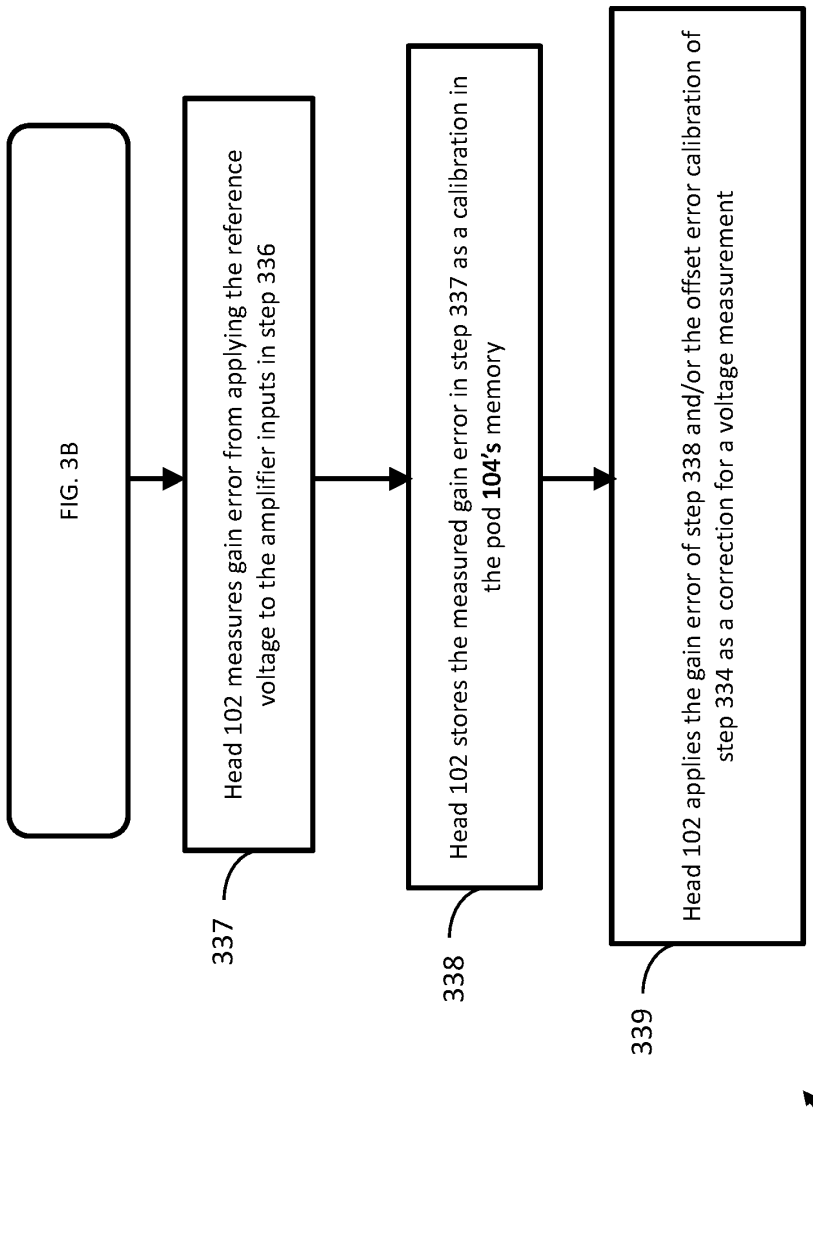


FIG. 3B
Head 102 measures gain error from applying the reference voltage to the amplifier inputs in step 336
337
Head 102 stores the measured gain error in step 337 as a calibration in the pod **104's** memory
338
Head 102 applies the gain error of step 338 and/or the offset error calibration of step 334 as a correction for a voltage measurement
339
330

FIG. 3C

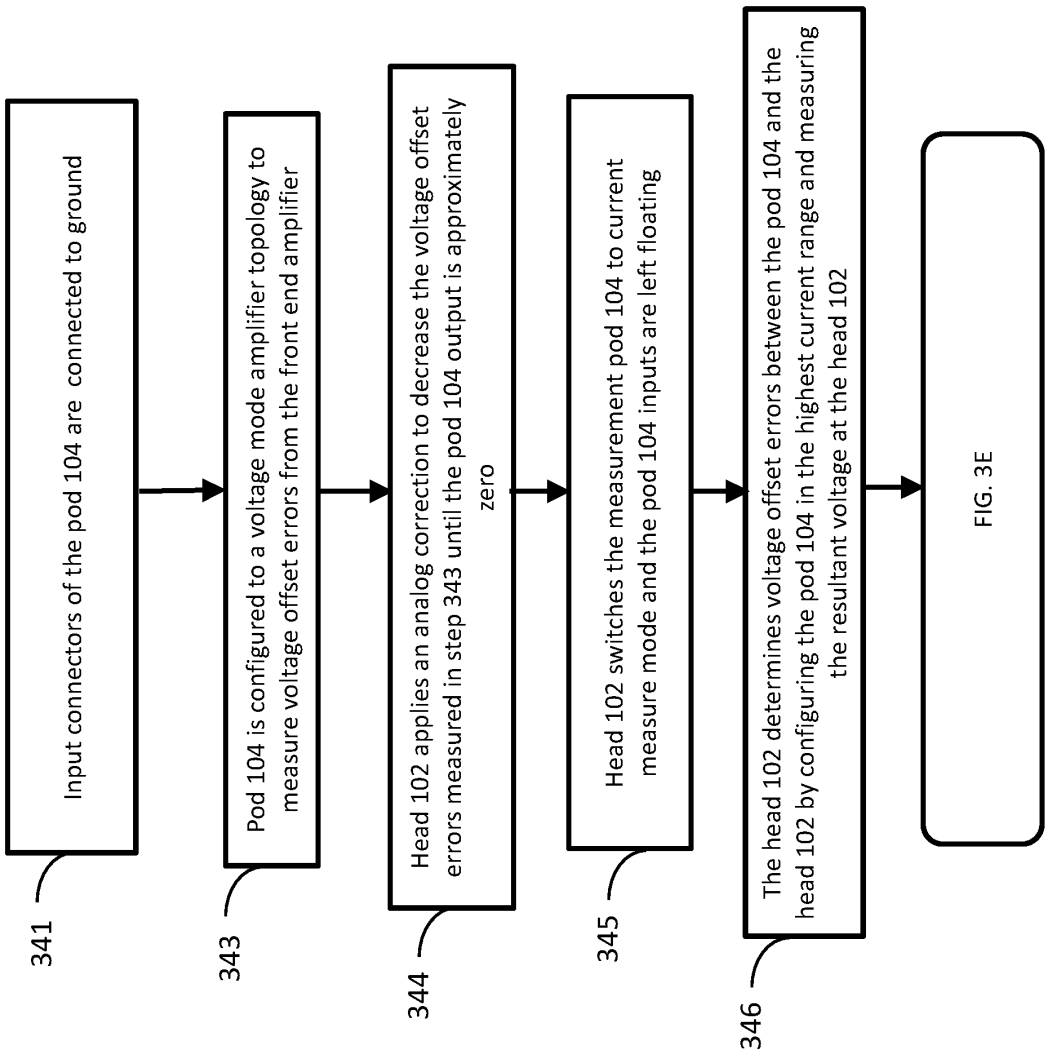

Input connectors of the pod 104 are connected to ground
Pod 104 is configured to a voltage mode amplifier topology to measure voltage offset errors from the front end amplifier
Head 102 applies an analog correction to decrease the voltage offset errors measured in step 343 until the pod 104 output is approximately zero
Head 102 switches the measurement pod 104 to current measure mode and the pod 104 inputs are left floating
The head 102 determines voltage offset errors between the pod 104 and the head 102 by configuring the pod 104 in the highest current range and measuring the resultant voltage at the head 102
FIG. 3E
341
343
344
345
346
340

FIG. 3D

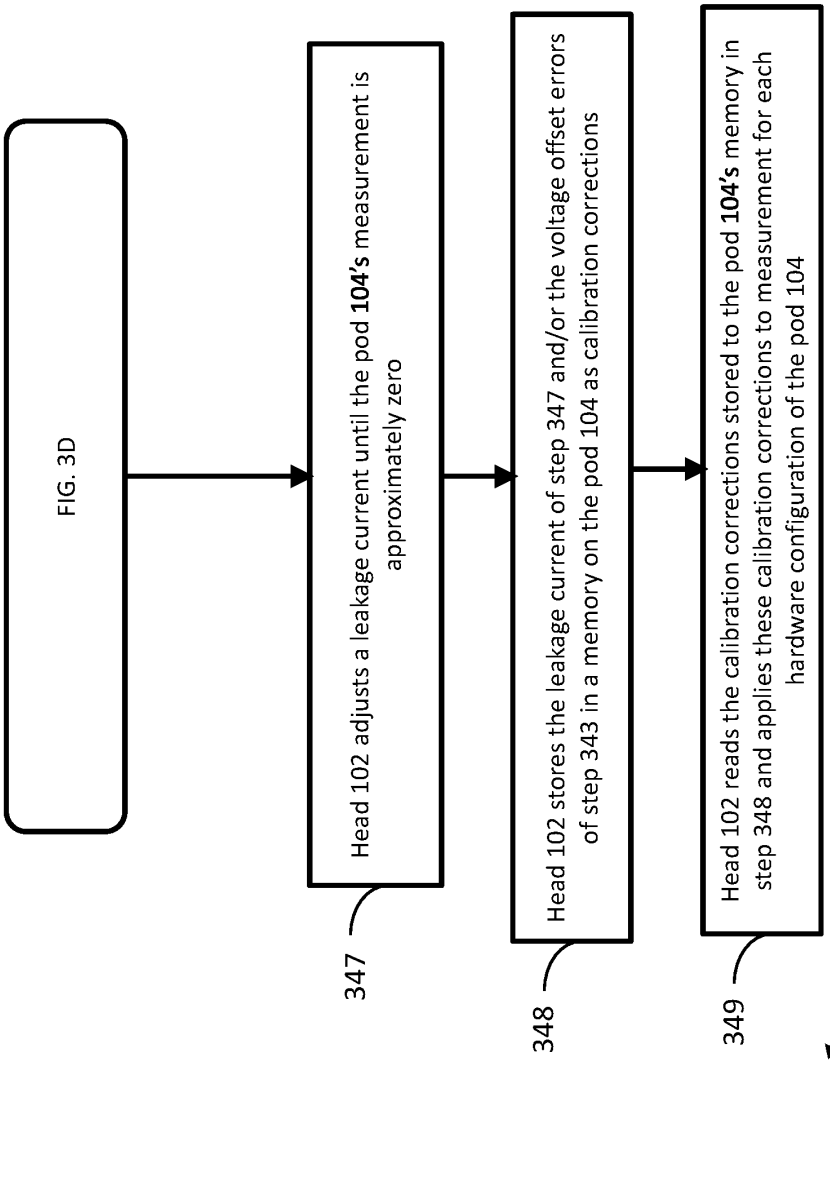


FIG. 3D
Head 102 adjusts a leakage current until the pod 104's measurement is approximately zero
347
Head 102 stores the leakage current of step 347 and/or the voltage offset errors of step 343 in a memory on the pod 104 as calibration corrections
348
Head 102 reads the calibration corrections stored to the pod 104's memory in step 348 and applies these calibration corrections to measurement for each hardware configuration of the pod 104
349
340

FIG. 3E

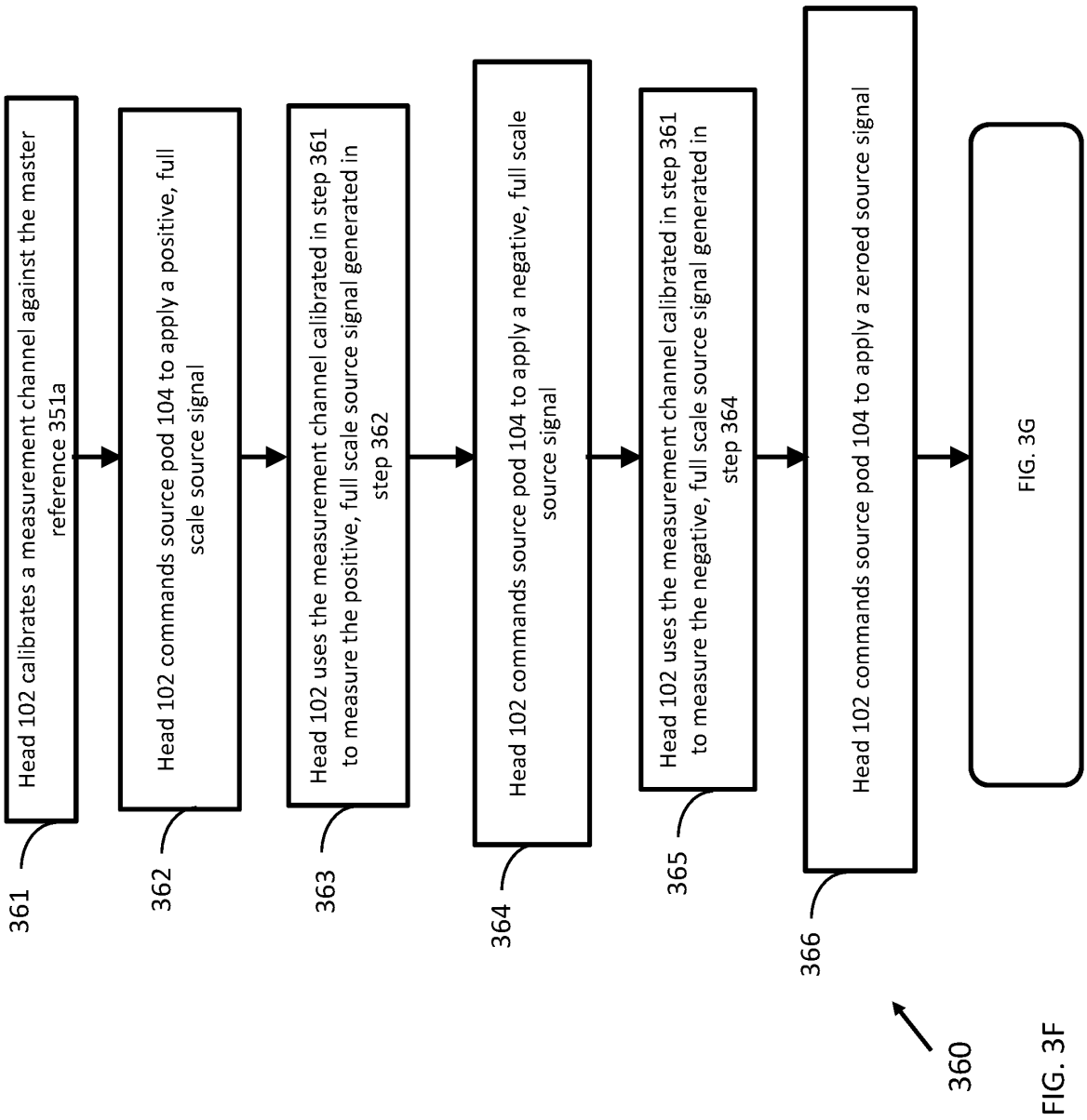

Head 102 calibrates a measurement channel against the master reference 351a
361
Head 102 commands source pod 104 to apply a positive, full scale source signal
362
Head 102 uses the measurement channel calibrated in step 361 to measure the positive, full scale source signal generated in step 362
363
Head 102 commands source pod 104 to apply a negative, full scale source signal
364
Head 102 uses the measurement channel calibrated in step 361 to measure the negative, full scale source signal generated in step 364
365
Head 102 commands source pod 104 to apply a zeroed source signal
366
FIG. 3G
360

FIG. 3F

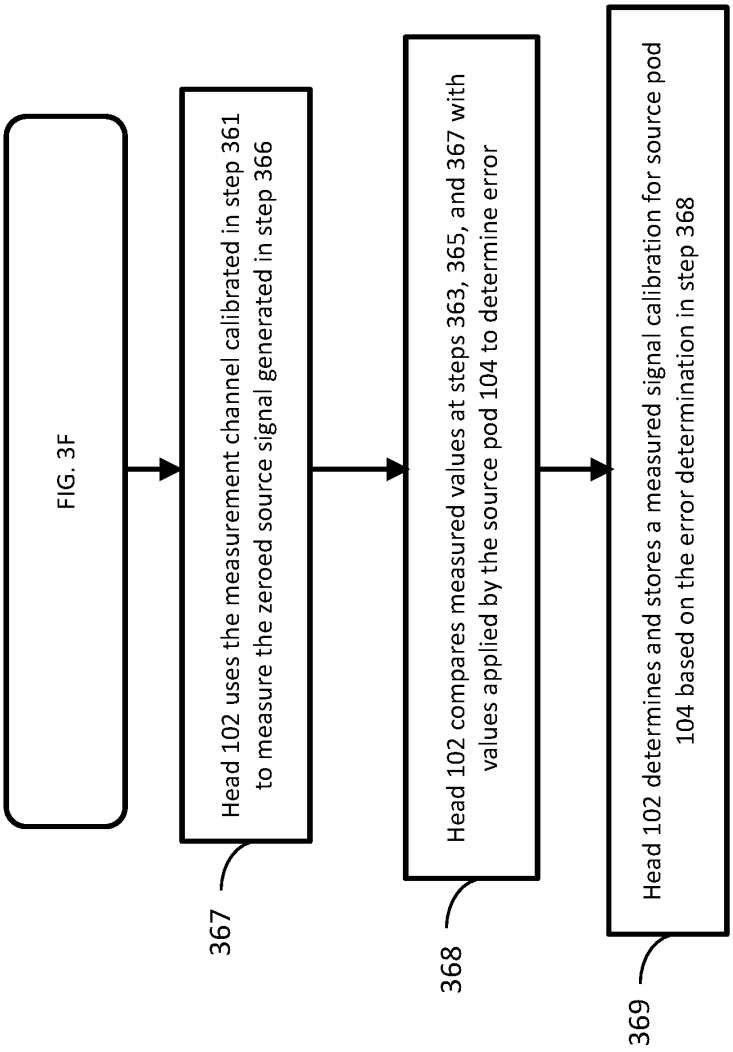


FIG. 3F
Head 102 uses the measurement channel calibrated in step 361 to measure the zeroed source signal generated in step 366
367
Head 102 compares measured values at steps 363, 365, and 367 with values applied by the source pod 104 to determine error
368
Head 102 determines and stores a measured signal calibration for source pod 104 based on the error determination in step 368
369
360

FIG. 3G

features	**Enhanced Combination Source/Measure Pod**	**Precision Source Pod**	**Balanced Current Source Pod**
Voltage source	✔	✔	
Current source	✔		✔
Common mode noise rejection			✔
Hybrid AC/DC sourcing	✔	✔	
DC up to	10 kHz	100 kHz	100 kHz
Source span	nV – 10 V or pA – 100 mA	nV – 10 V or pA – 100 mA	pA – 100 mA

FIG. 4

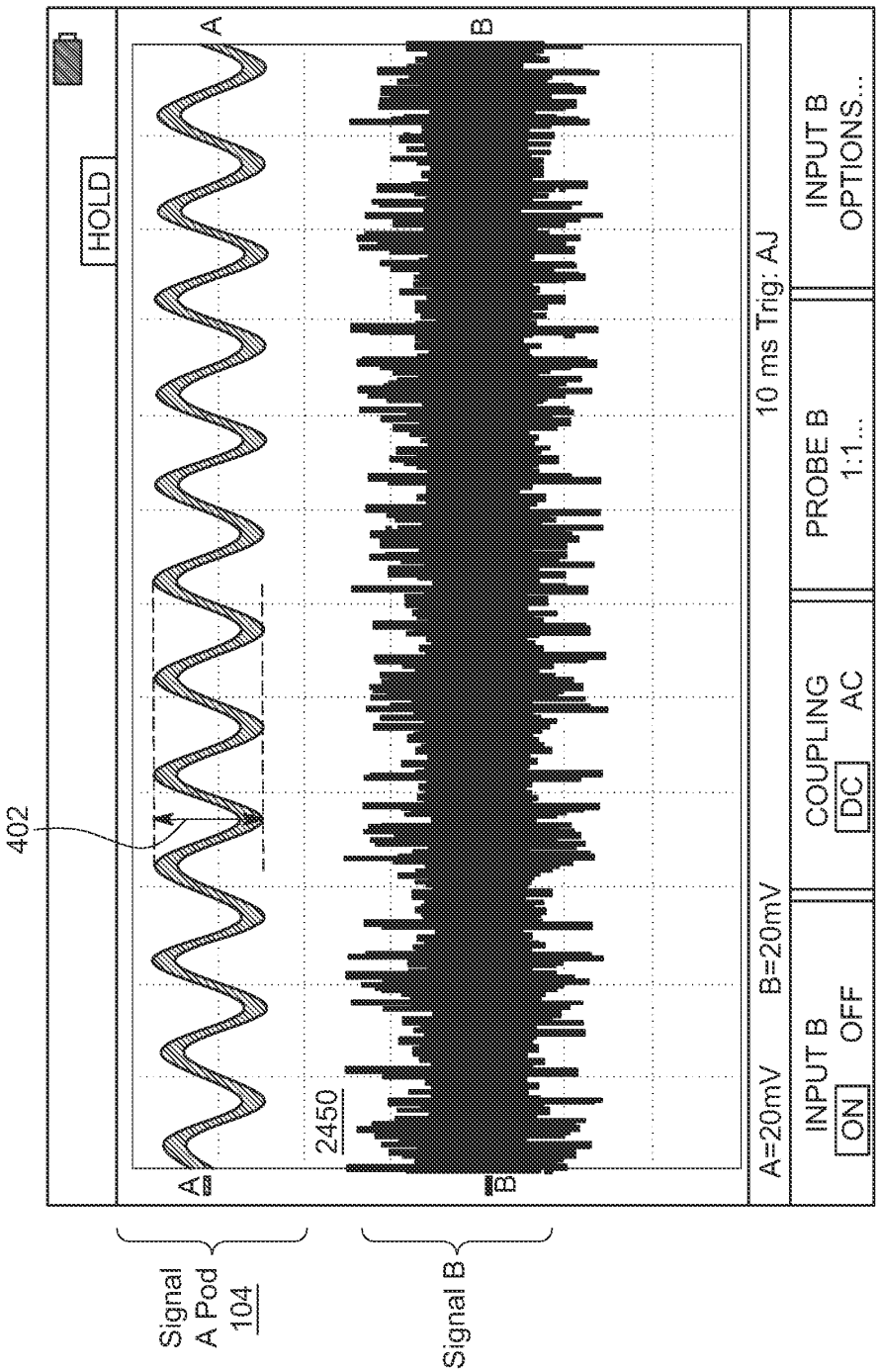

HOLD
A
B
402
2450
A=20mV
B=20mV
10 ms Trig: AJ
INPUT B
ON OFF
COUPLING
DC AC
PROBE B
1:1...
INPUT B
OPTIONS...
Signal
A Pod
104
Signal B

FIG. 5A

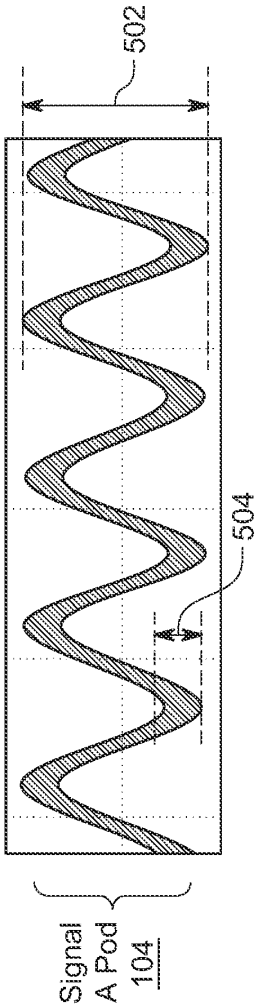


FIG. 5B

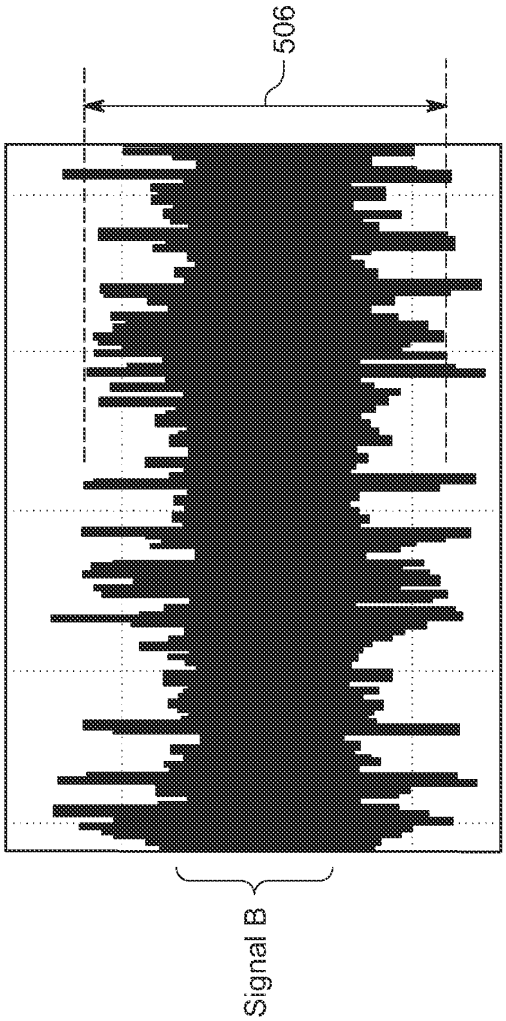


FIG. 5C

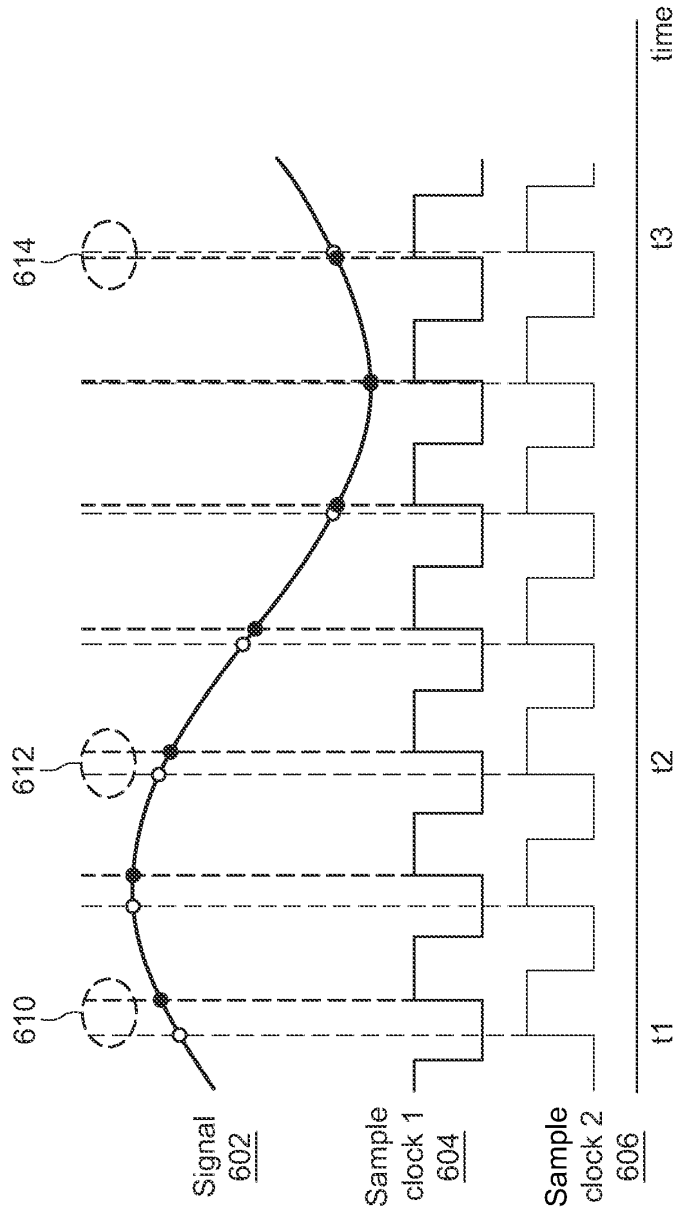

610
612
614
Signal
602
Sample
clock 1
604
Sample
clock 2
606
t1
t2
t3
time

FIG. 6A

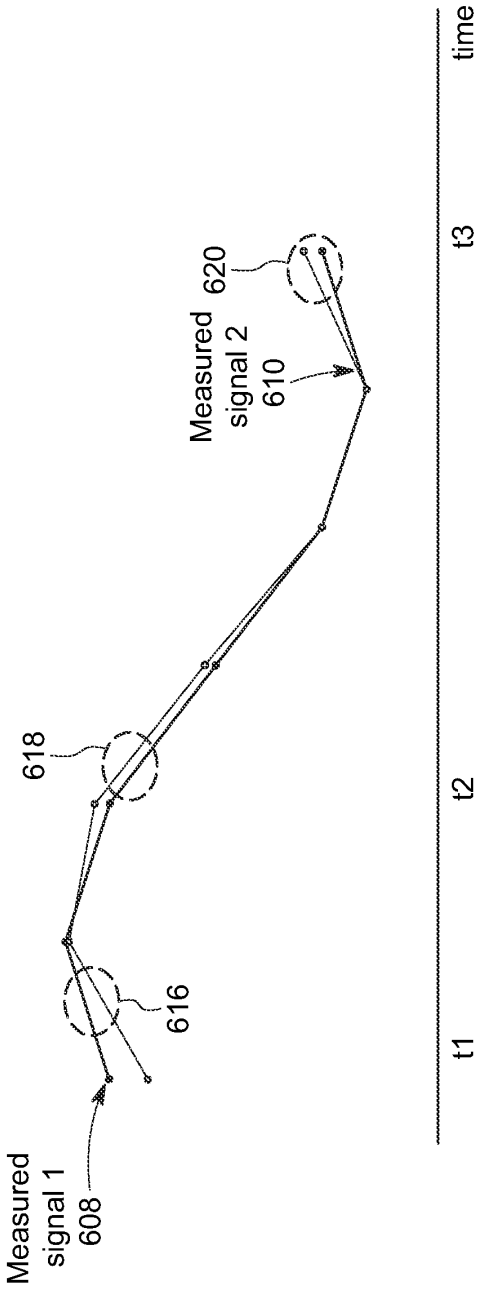

Measured signal 1 608
616
618
Measured signal 2 610
620
t1
t2
t3
time

FIG. 6B

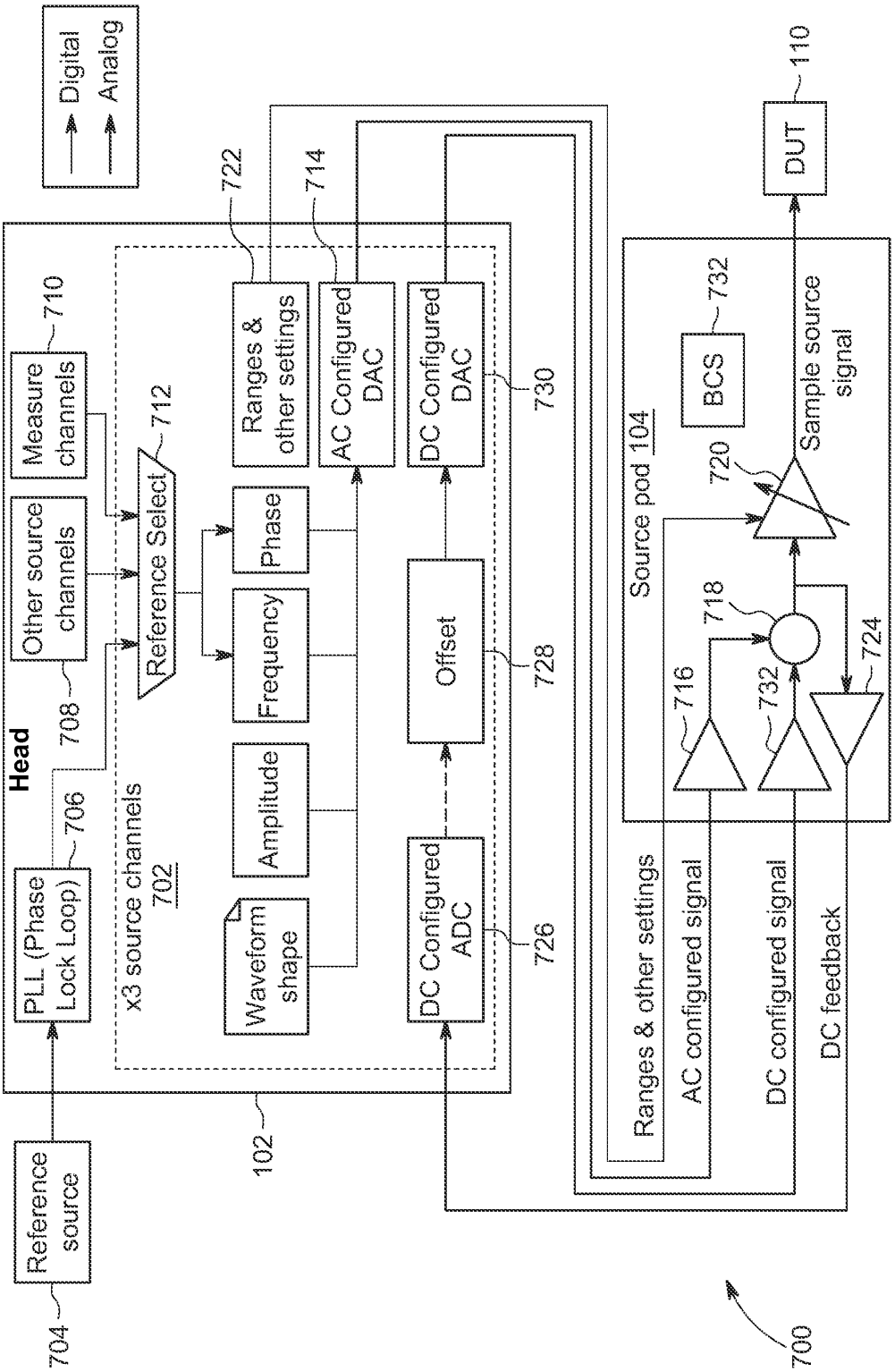

Digital
Analog
Head
PLL (Phase Lock Loop)
706
Other source channels
708
Measure channels
710
Reference Select
712
x3 source channels
702
Waveform shape
Amplitude
Frequency
Phase
Ranges & other settings
722
AC Configured DAC
714
DC Configured DAC
730
Offset
728
DC Configured ADC
726
102
Reference source
704
Source pod 104
Ranges & other settings
AC configured signal
DC configured signal
DC feedback
716
718
732
724
720
BCS
732
Sample source signal
DUT
110
700

FIG. 7

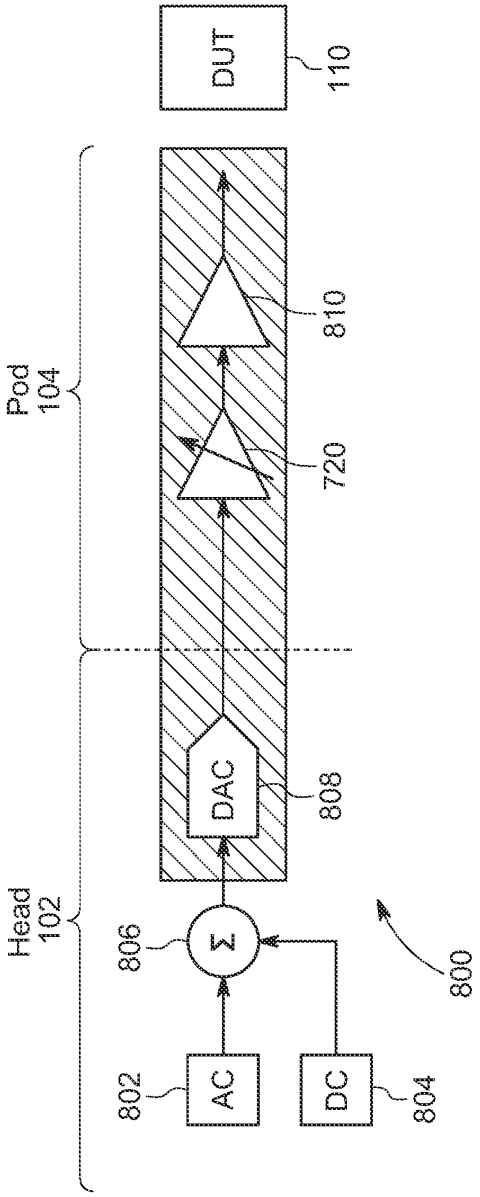


FIG. 8

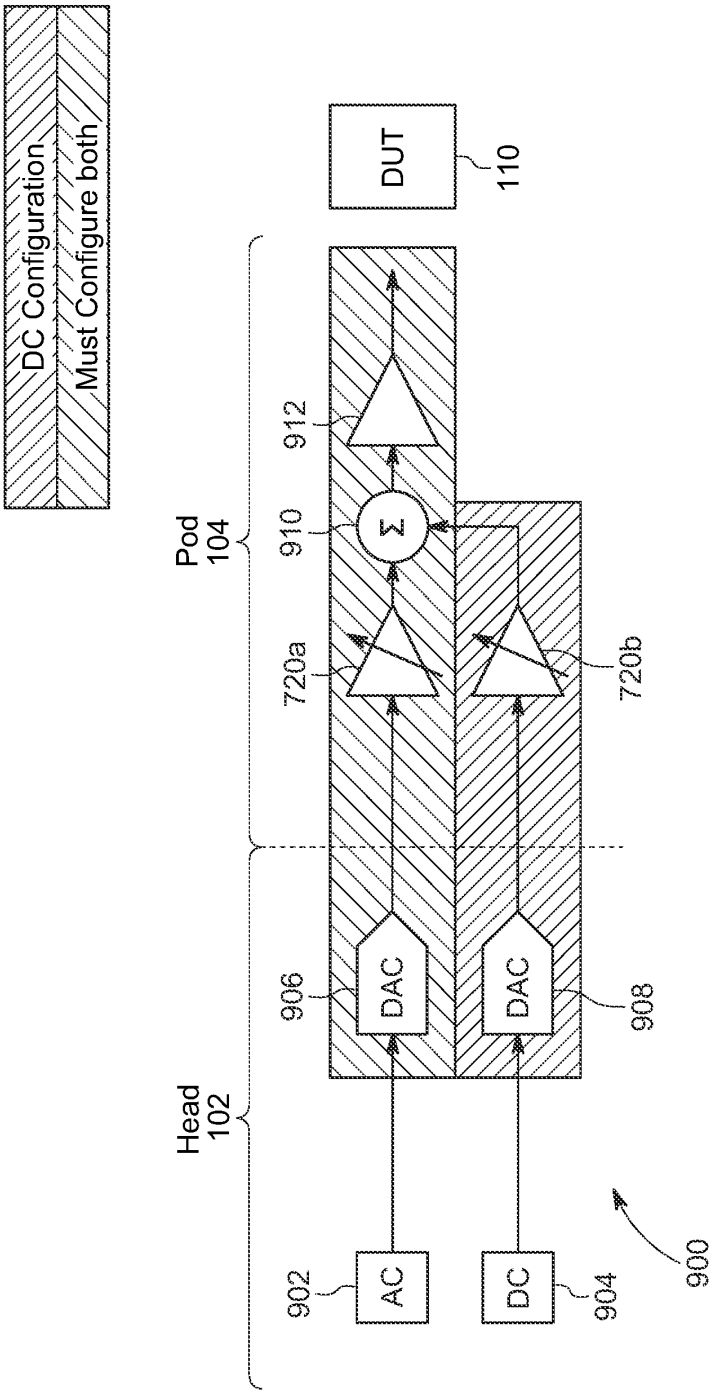

DC Configuration
Must Configure both
DUT
110
Pod
104
912
910
Σ
720a
720b
DAC
DAC
906
908
Head
102
902
AC
DC
904
900

FIG. 9

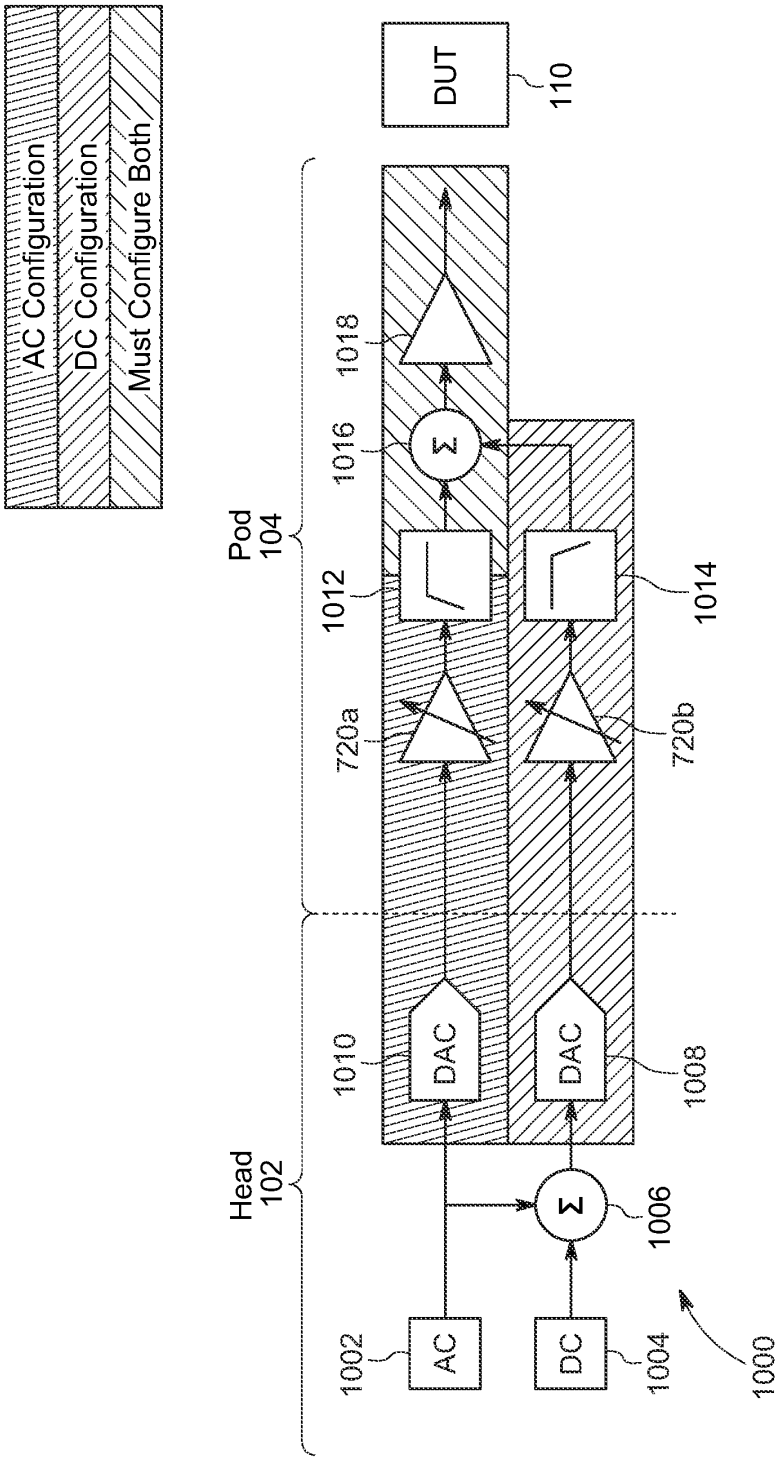

AC Configuration
DC Configuration
Must Configure Both
DUT
110
Pod
104
Head
102
1018
1016
Σ
1012
1014
720a
720b
1010
DAC
DAC
1008
1006
Σ
1002
AC
DC
1004
1000

FIG. 10

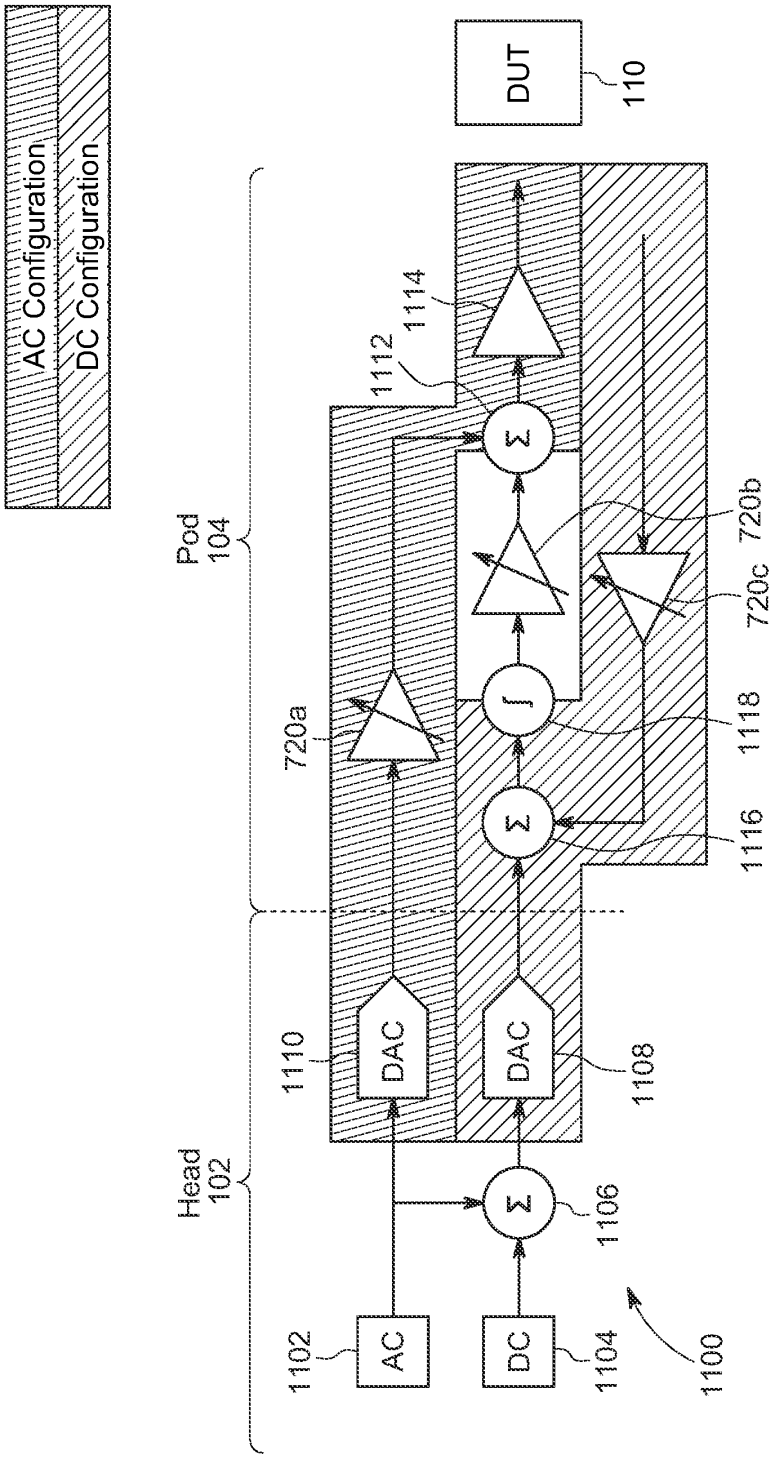

AC Configuration
DC Configuration
DUT
110
Pod
104
Head
102
1114
1112
720b
720c
720a
1118
1116
1110
1108
1106
1102
1104
1100
DAC
DAC
AC
DC
Σ
Σ
Σ
∫

FIG. 11

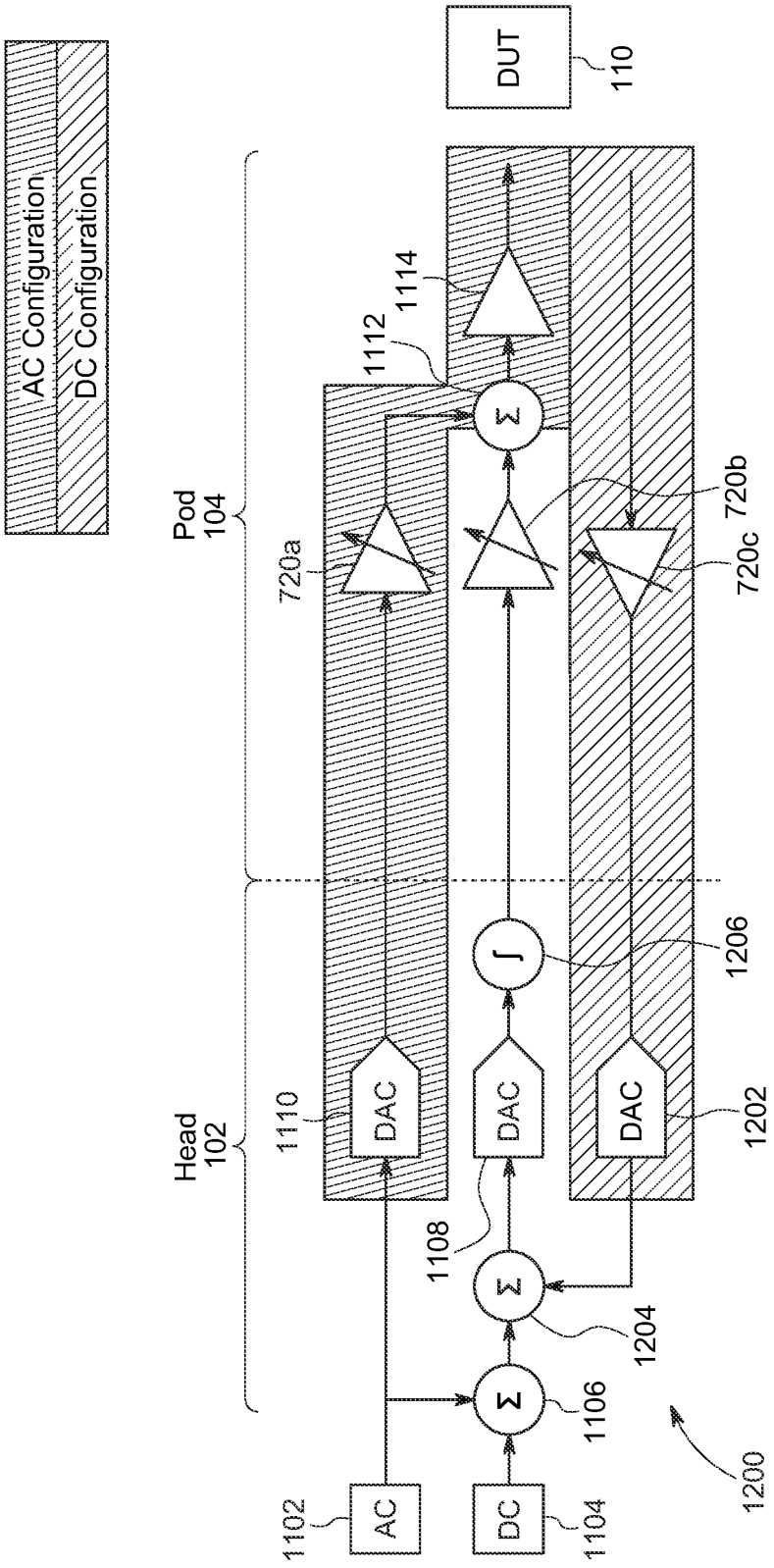

AC Configuration
DC Configuration
DUT
110
Pod
104
Head
102
1114
1112
720a
720b
720c
1110
1108
1206
1202
1204
1106
1102
1104
1200
DAC
AC
DC
Σ
∫

FIG. 12

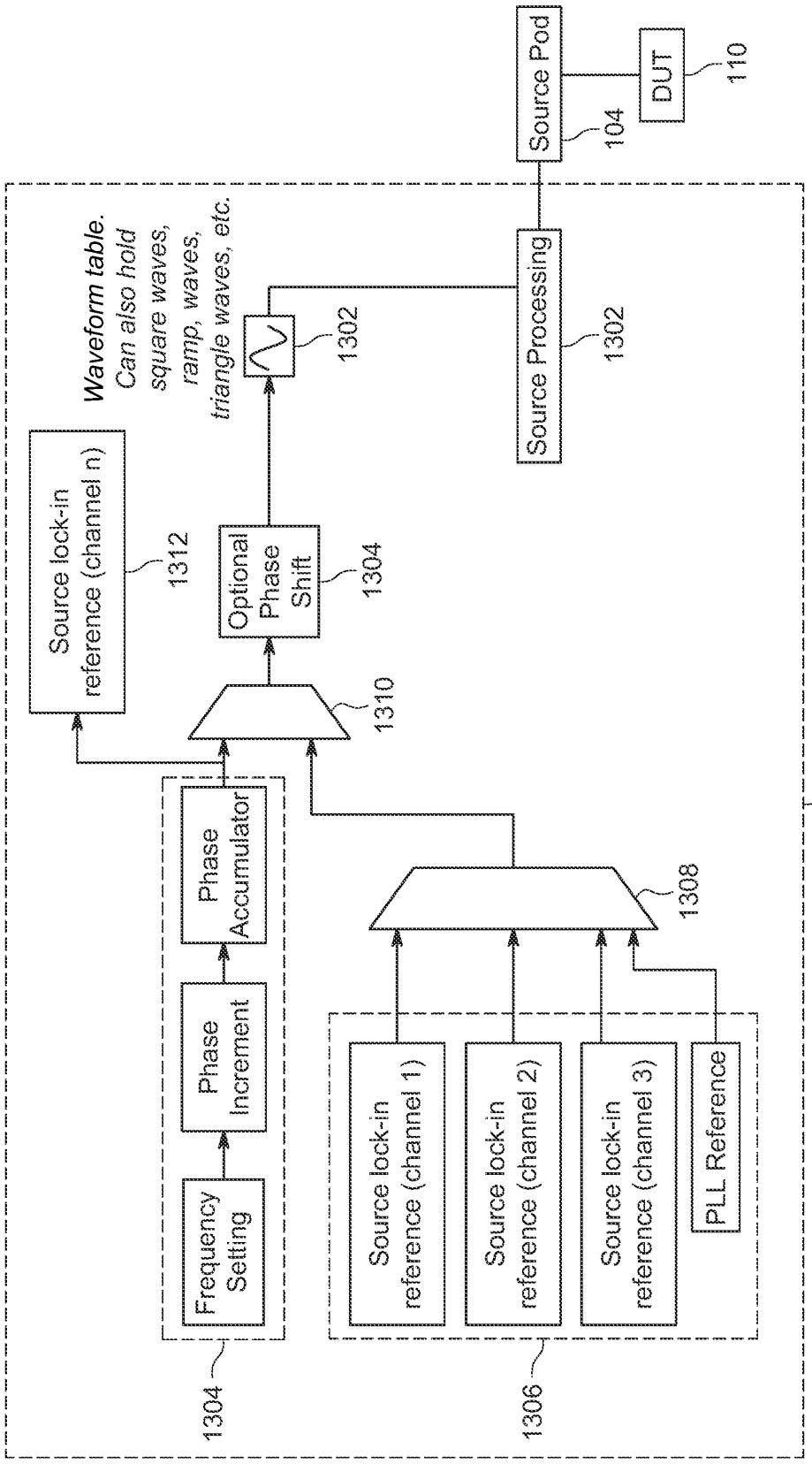

Source Pod
104
DUT
110
Source Processing
1302
1302
Waveform table.
Can also hold
square waves,
ramp, waves,
triangle waves, etc.
Source lock-in
reference (channel n)
1312
Optional
Phase
Shift
1304
1310
Phase
Accumulator
Phase
Increment
Frequency
Setting
1304
1308
Source lock-in
reference (channel 1)
Source lock-in
reference (channel 2)
Source lock-in
reference (channel 3)
PLL Reference
1306
1300

FIG. 13

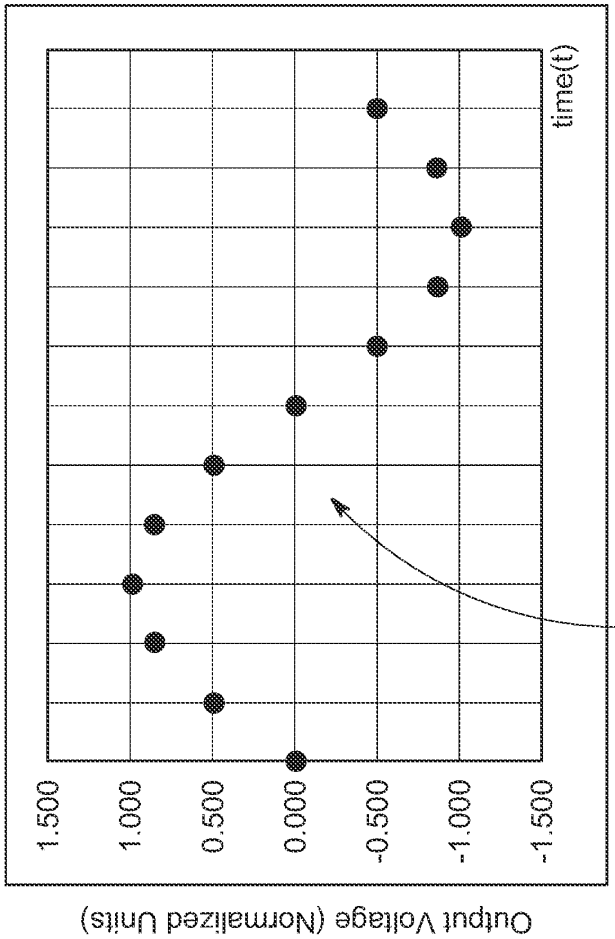


FIG. 15

1400

Position	Output
0	0.000
1	0.500
2	0.866
3	1.000
4	0.866
5	0.500
6	0.000
7	-0.500
8	-0.866
9	-1.000
10	-0.866
11	-0.500

FIG. 14

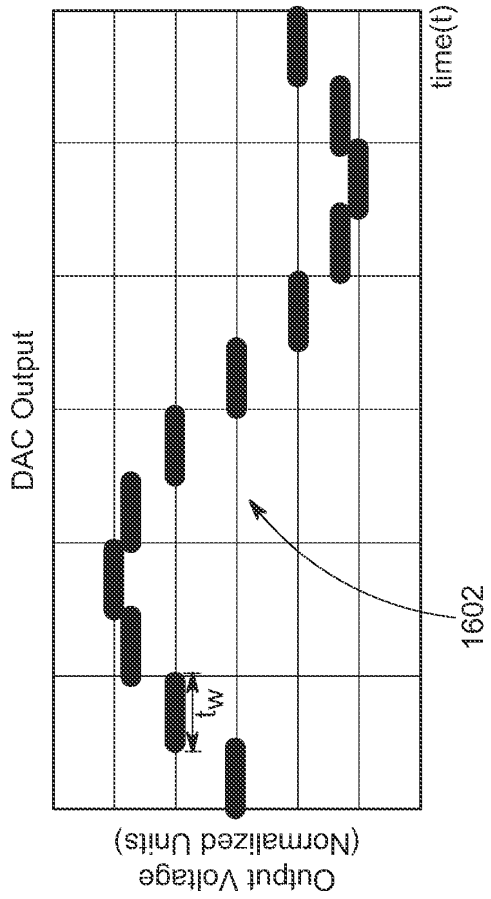


FIG. 16A

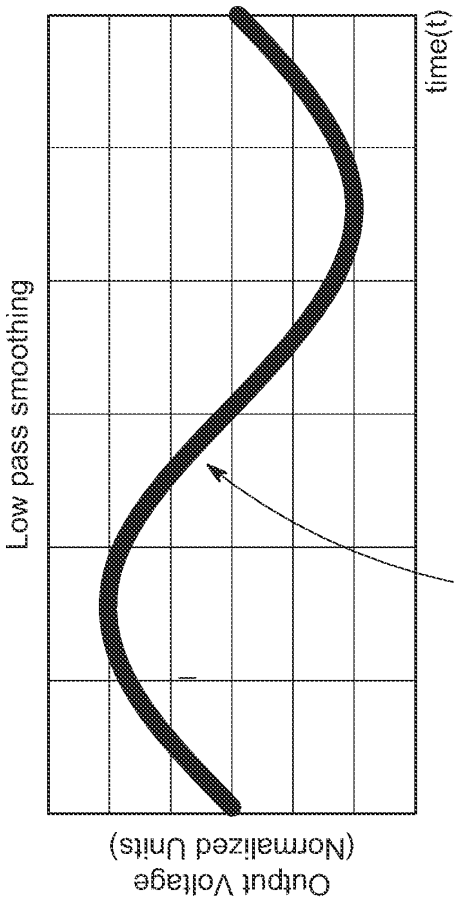

Low pass smoothing
time(t)
Output Voltage
(Normalized Units)
1604

FIG. 16B

features	**Enhanced Combination Source/Measure Pod**	**Voltage Measure Pod**	**Current Measure Pod**
Measures voltage	✔	✔	
Measures current	✔		✔
Lowest noise		✔	✔
Analog filters		✔	✔
Seamless ranging		✔	
DC up to	100 kHz	100 kHz	100 kHz
Measure span	nV – 10 V or pA – 100 mA	nV – 10 V	pA – 100 mA

FIG. 17

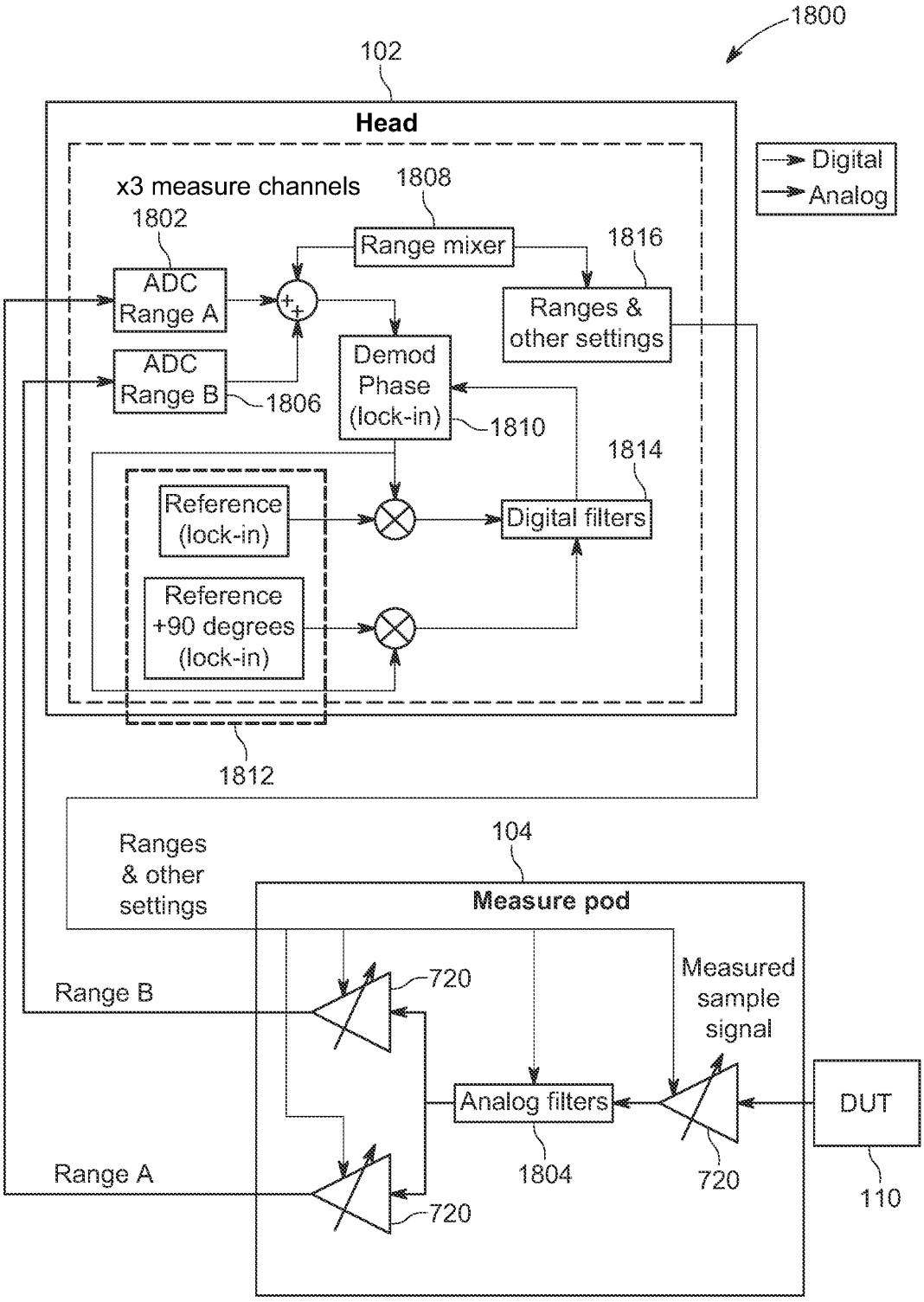

1800
102
Head
Digital
Analog
x3 measure channels
1808
1802
Range mixer
1816
ADC
Range A
Ranges &
other settings
ADC
Range B
1806
Demod
Phase
(lock-in)
1810
1814
Reference
(lock-in)
Digital filters
Reference
+90 degrees
(lock-in)
1812
Ranges
& other
settings
104
Measure pod
Measured
sample
signal
Range B
720
Analog filters
DUT
Range A
1804
720
110
720

FIG. 18

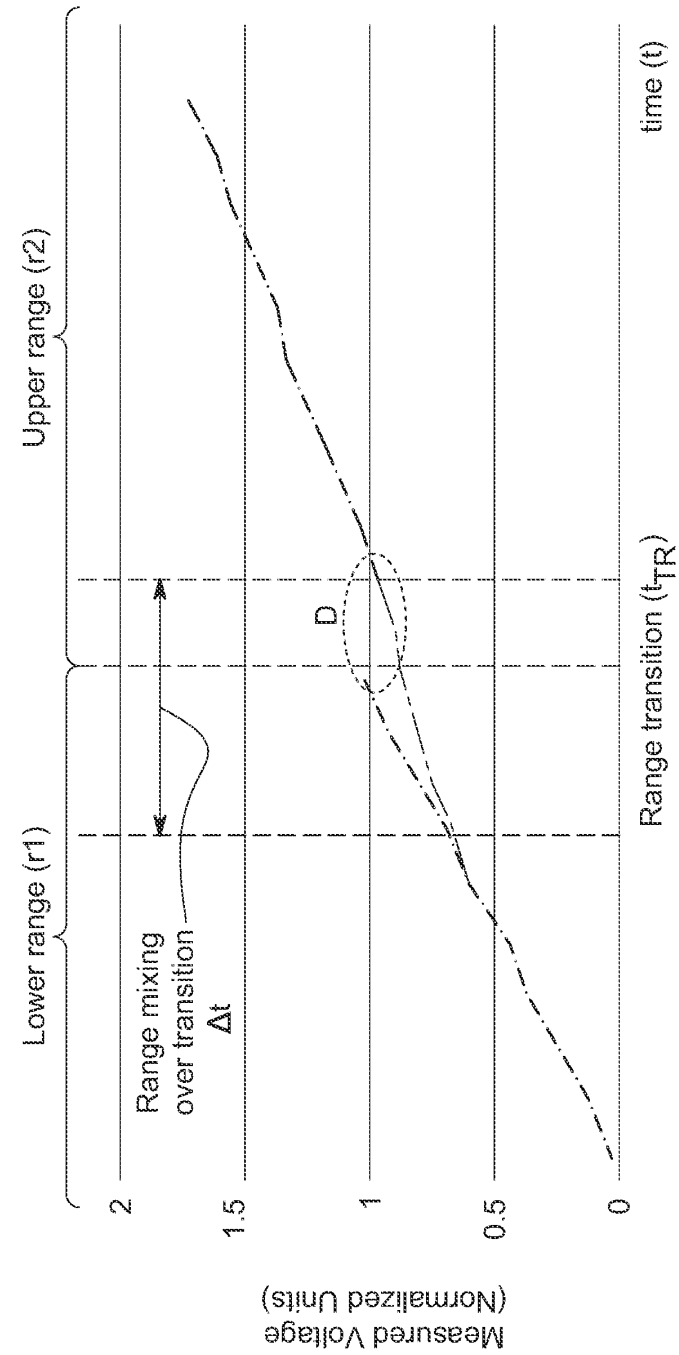

Lower range (r1)
Upper range (r2)
Range mixing
over transition
Δt
D
Range transition (t_{TR})
time (t)
Measured Voltage
(Normalized Units)
2
1.5
1
0.5
0
Continuous ranging data
(M81 100, 200, and 300)
1902
Conventional ranging data
1904

FIG. 19

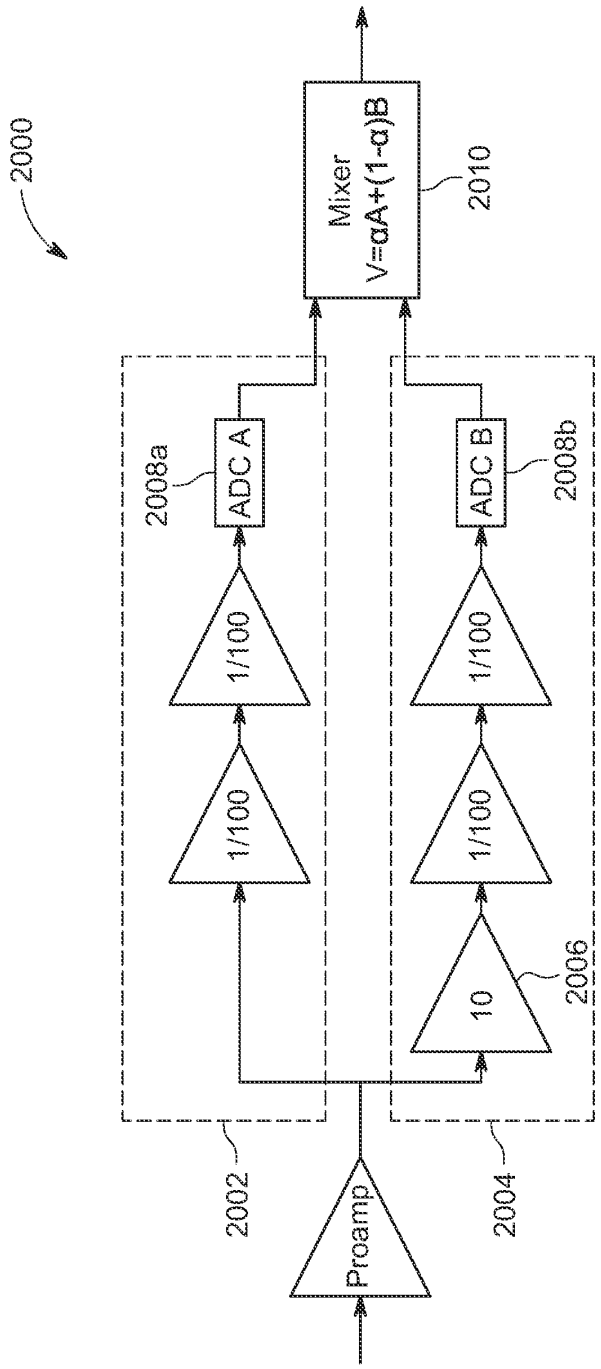

2000
Mixer
V=αA+(1-α)B
2010
2008a
ADC A
2008b
ADC B
1/100
1/100
1/100
1/100
10
2006
2002
2004
Proamp

FIG. 20

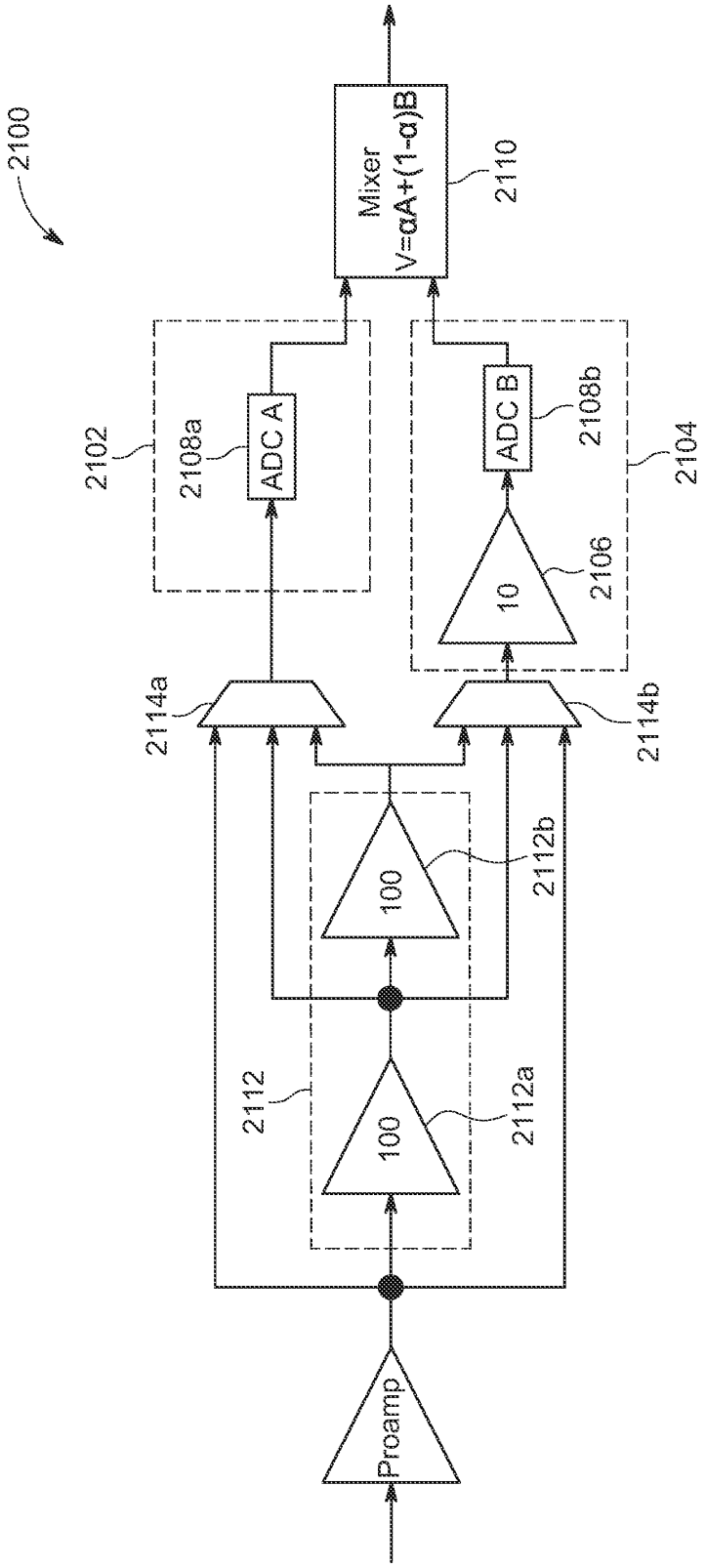

2100
Mixer
V=αA+(1-α)B
2110
2102
2108a
ADC A
ADC B
2108b
2104
10
2106
2114a
2114b
100
2112b
2112
100
2112a
Proamp

FIG. 21

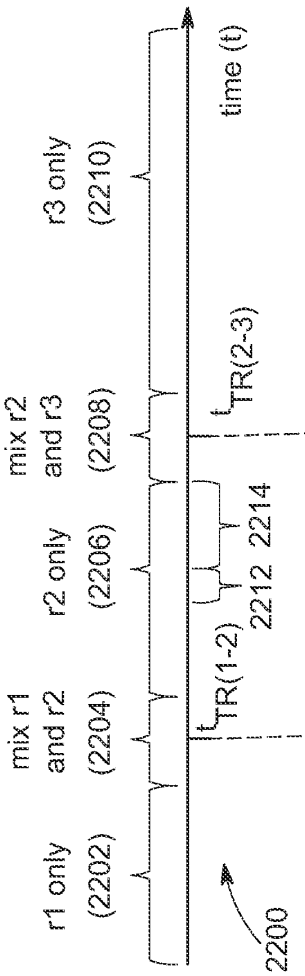


FIG. 22A

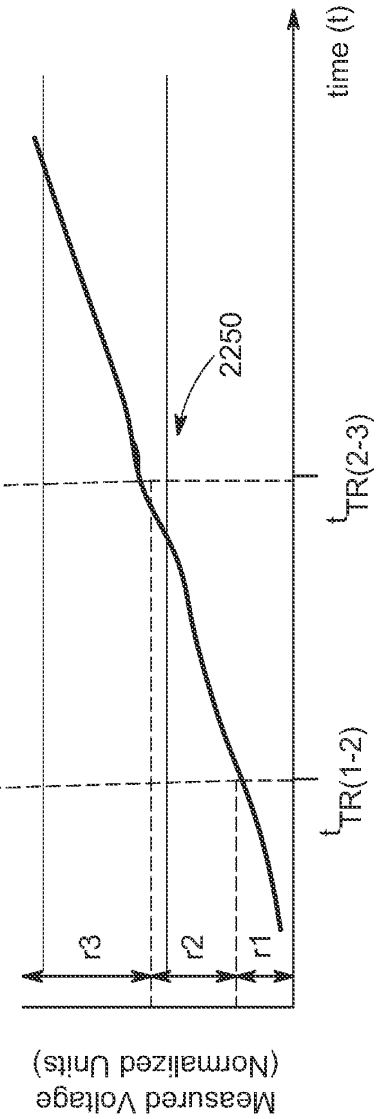
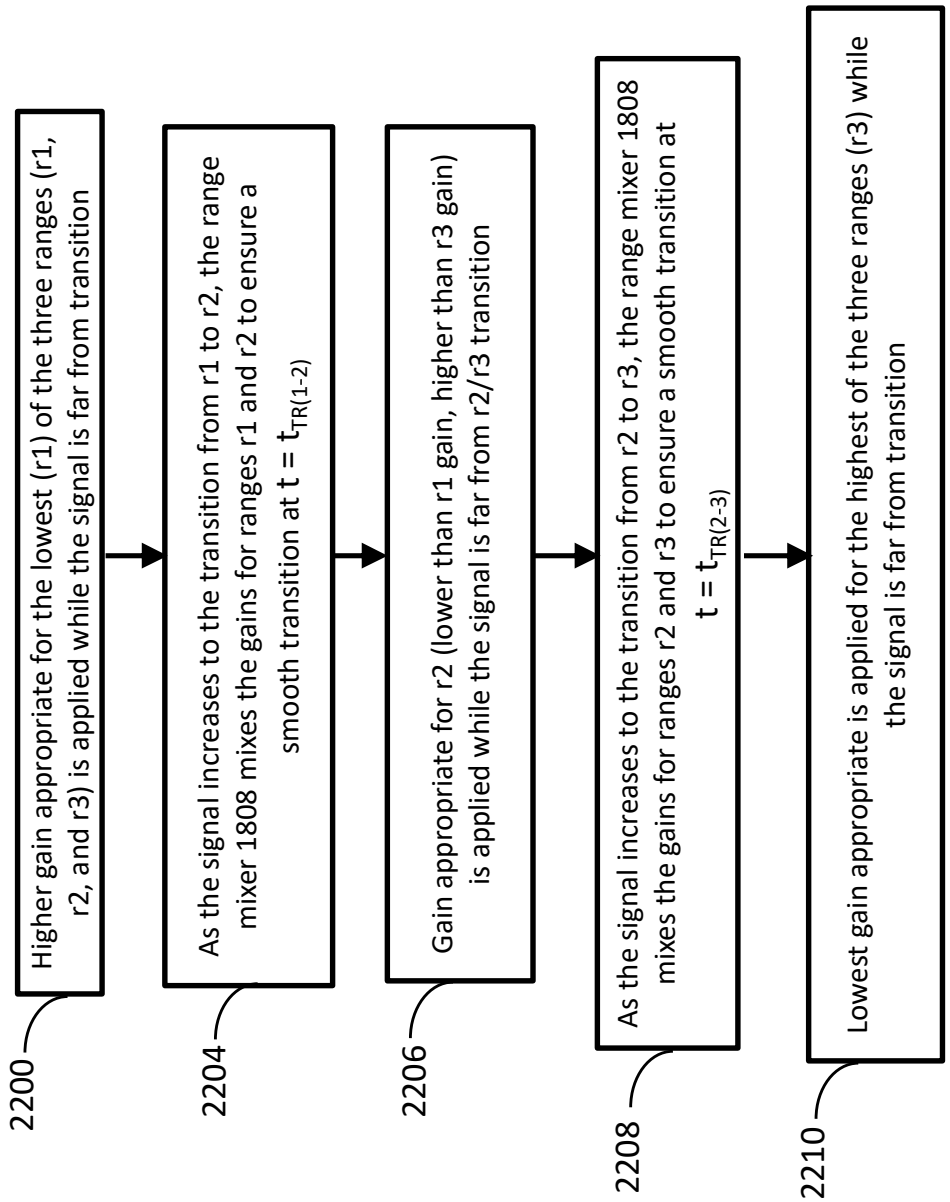


FIG. 22B


Higher gain appropriate for the lowest (r1) of the three ranges (r1, r2, and r3) is applied while the signal is far from transition
As the signal increases to the transition from r1 to r2, the range mixer 1808 mixes the gains for ranges r1 and r2 to ensure a smooth transition at $t = t_{TR(1-2)}$
Gain appropriate for r2 (lower than r1 gain, higher than r3 gain) is applied while the signal is far from r2/r3 transition
As the signal increases to the transition from r2 to r3, the range mixer 1808 mixes the gains for ranges r2 and r3 to ensure a smooth transition at $t = t_{TR(2-3)}$
Lowest gain appropriate is applied for the highest of the three ranges (r3) while the signal is far from transition
2200
2204
2206
2208
2210

2200

FIG. 22C

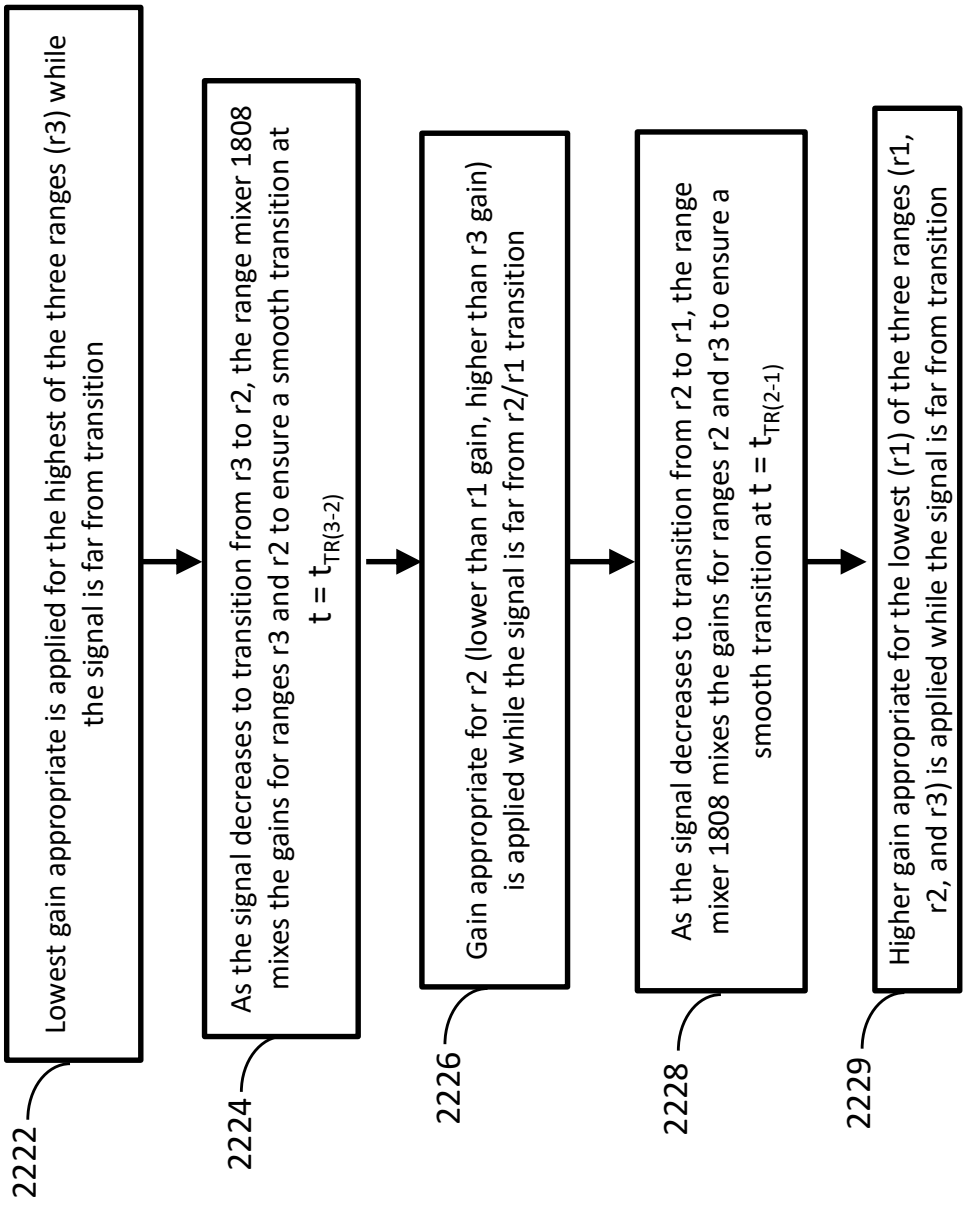

Lowest gain appropriate is applied for the highest of the three ranges (r3) while the signal is far from transition
2222
As the signal decreases to transition from r3 to r2, the range mixer 1808 mixes the gains for ranges r3 and r2 to ensure a smooth transition at $t = t_{TR(3-2)}$
2224
Gain appropriate for r2 (lower than r1 gain, higher than r3 gain) is applied while the signal is far from r2/r1 transition
2226
As the signal decreases to transition from r2 to r1, the range mixer 1808 mixes the gains for ranges r2 and r3 to ensure a smooth transition at $t = t_{TR(2-1)}$
2228
Higher gain appropriate for the lowest (r1) of the three ranges (r1, r2, and r3) is applied while the signal is far from transition
2229
2220

FIG. 22D

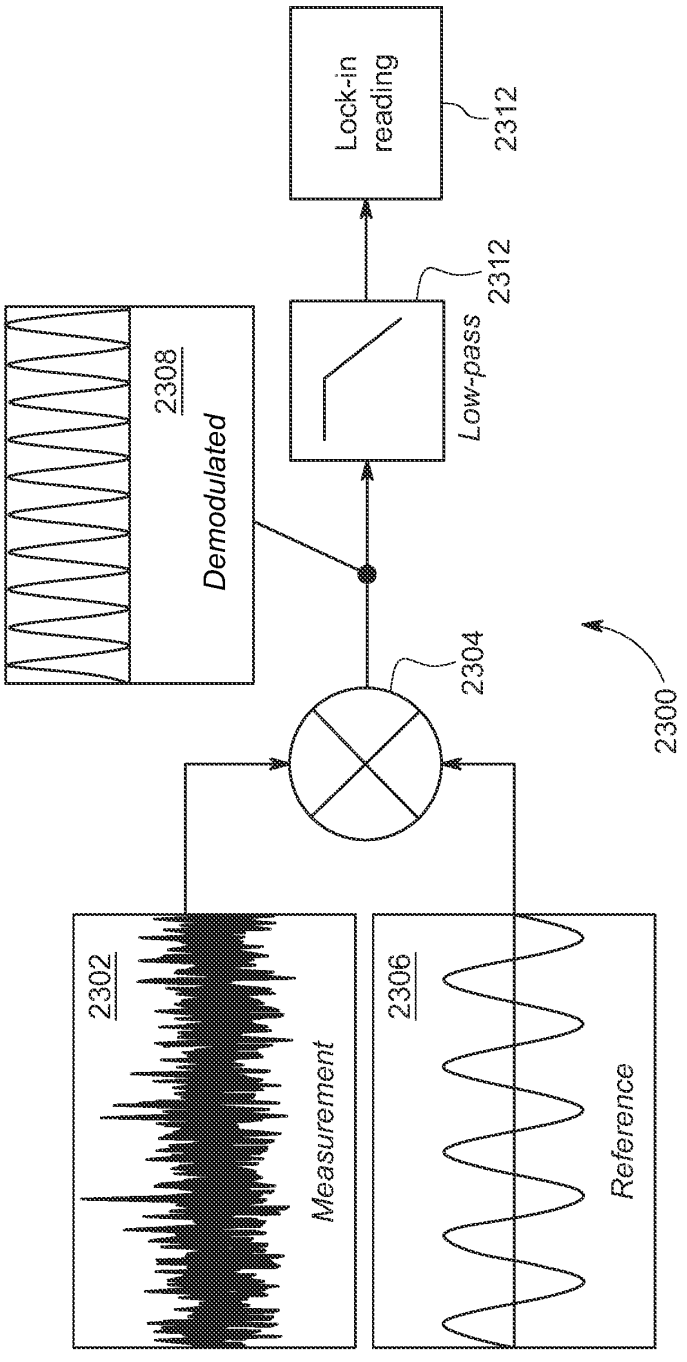

2302
Measurement
2306
Reference
2304
2308
Demodulated
Low-pass
2312
Lock-in reading
2312
2300

FIG. 23

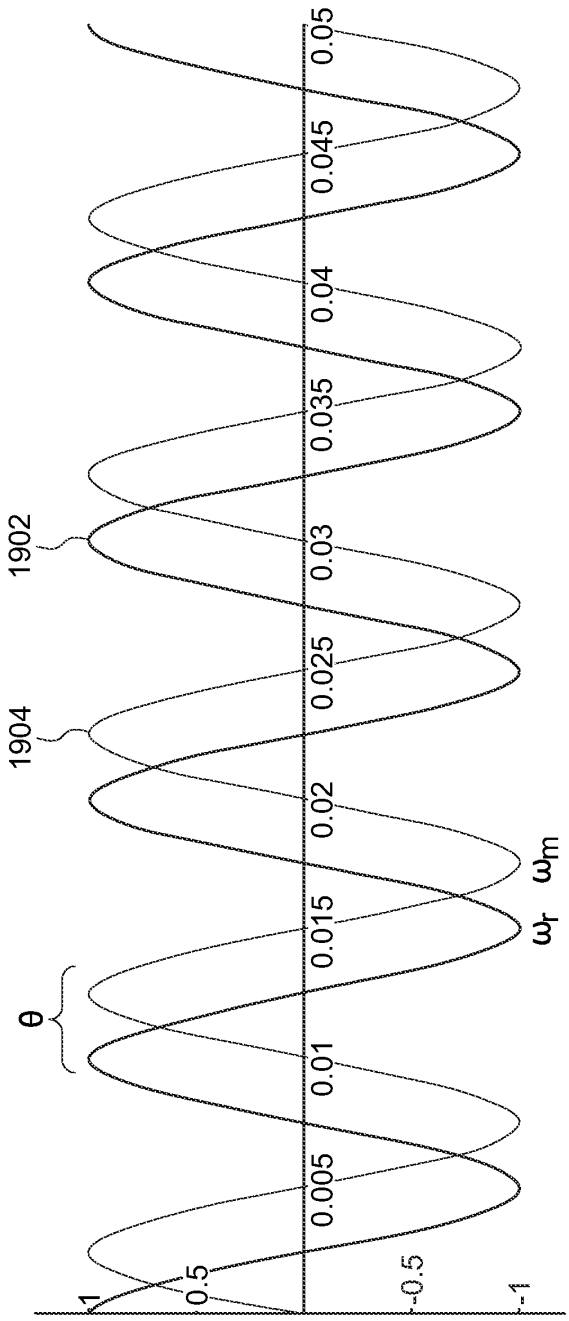

1
0.5
-0.5
-1
0.005
0.01
0.015
0.02
0.025
0.03
0.035
0.04
0.045
0.05
θ
1902
1904
ωr ωm

FIG. 24

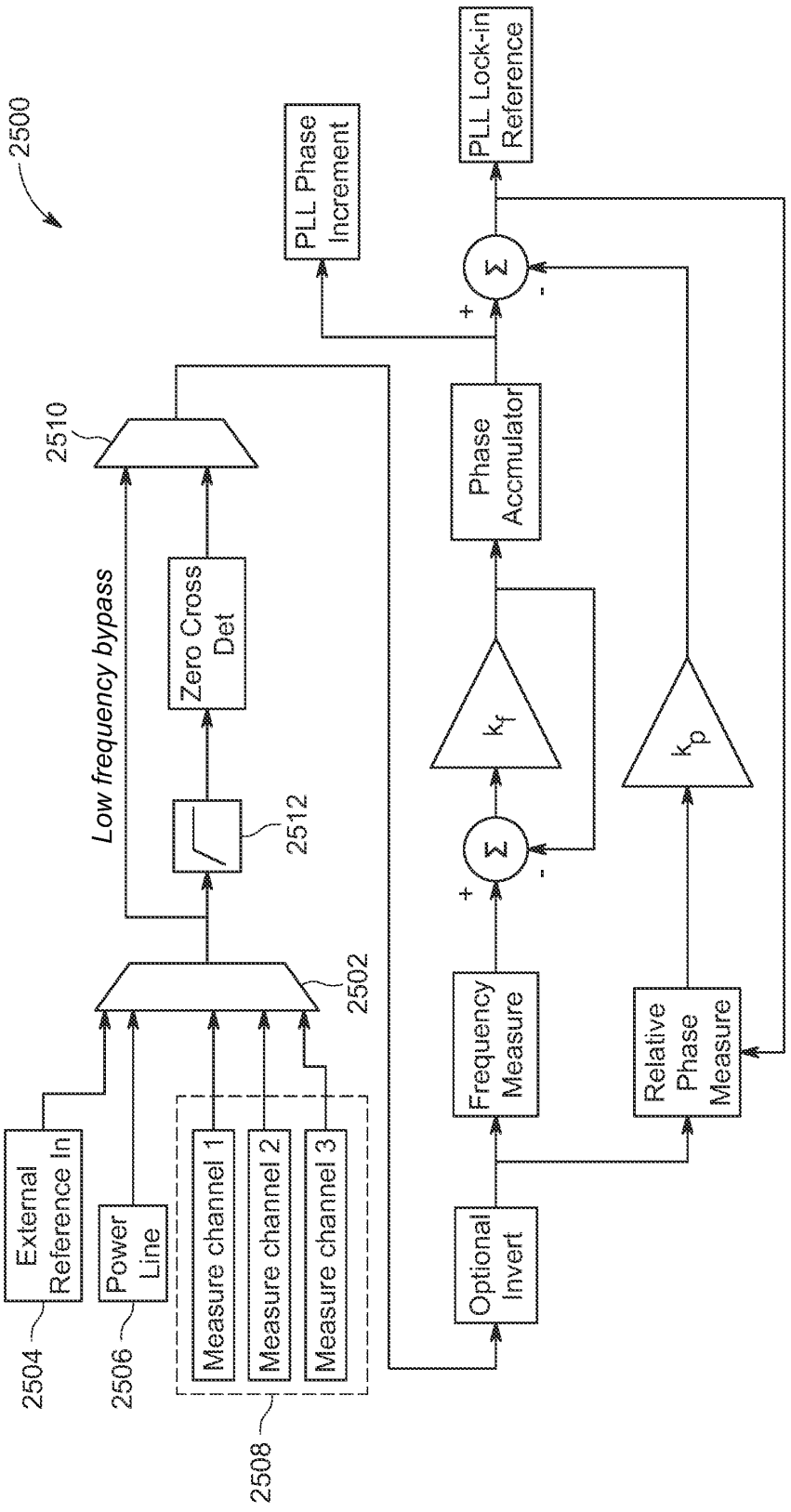

2500
External Reference In
Power Line
Measure channel 1
Measure channel 2
Measure channel 3
2504
2506
2508
2502
2512
Zero Cross Det
Low frequency bypass
2510
PLL Phase Increment
PLL Lock-in Reference
Phase Accmulator
Frequency Measure
Relative Phase Measure
Optional Invert
Σ
Σ
+
-
+
-
k_f
k_p

FIG. 25

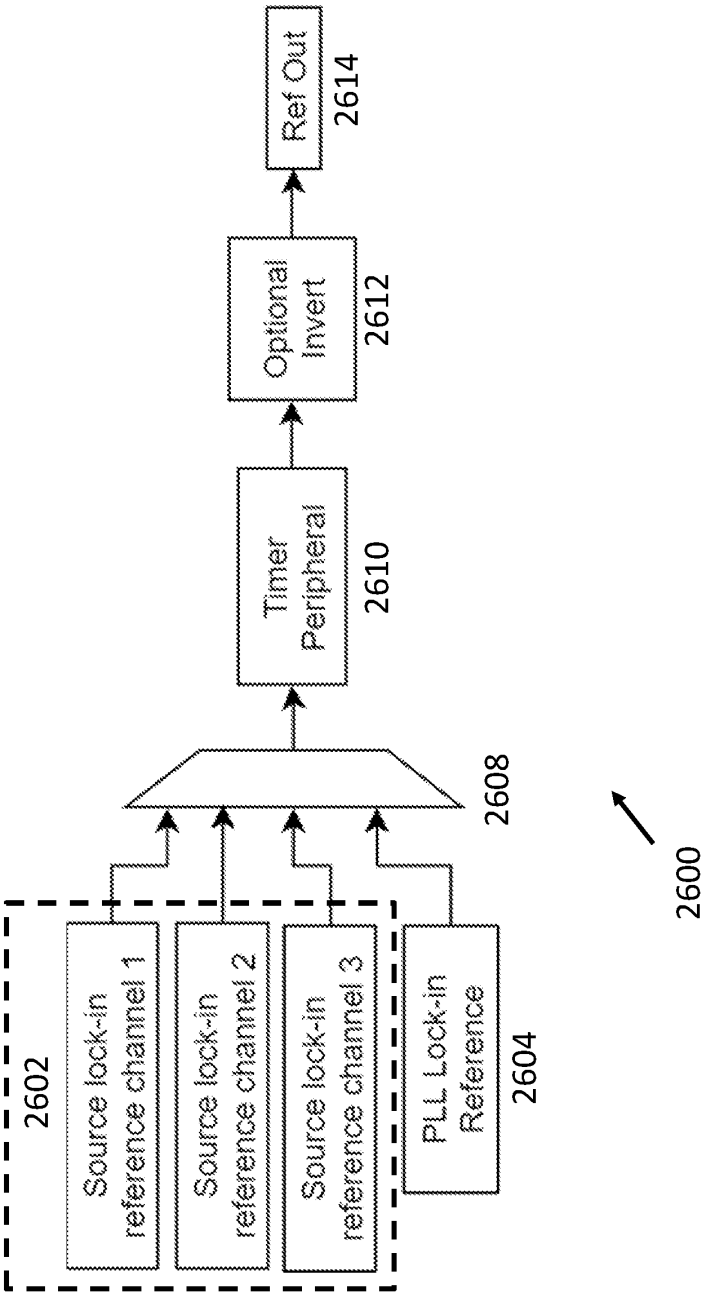

2602
Source lock-in reference channel 1
Source lock-in reference channel 2
Source lock-in reference channel 3
PLL Lock-in Reference
2604
2608
Timer Peripheral
2610
Optional Invert
2612
Ref Out
2614
2600

FIG. 26

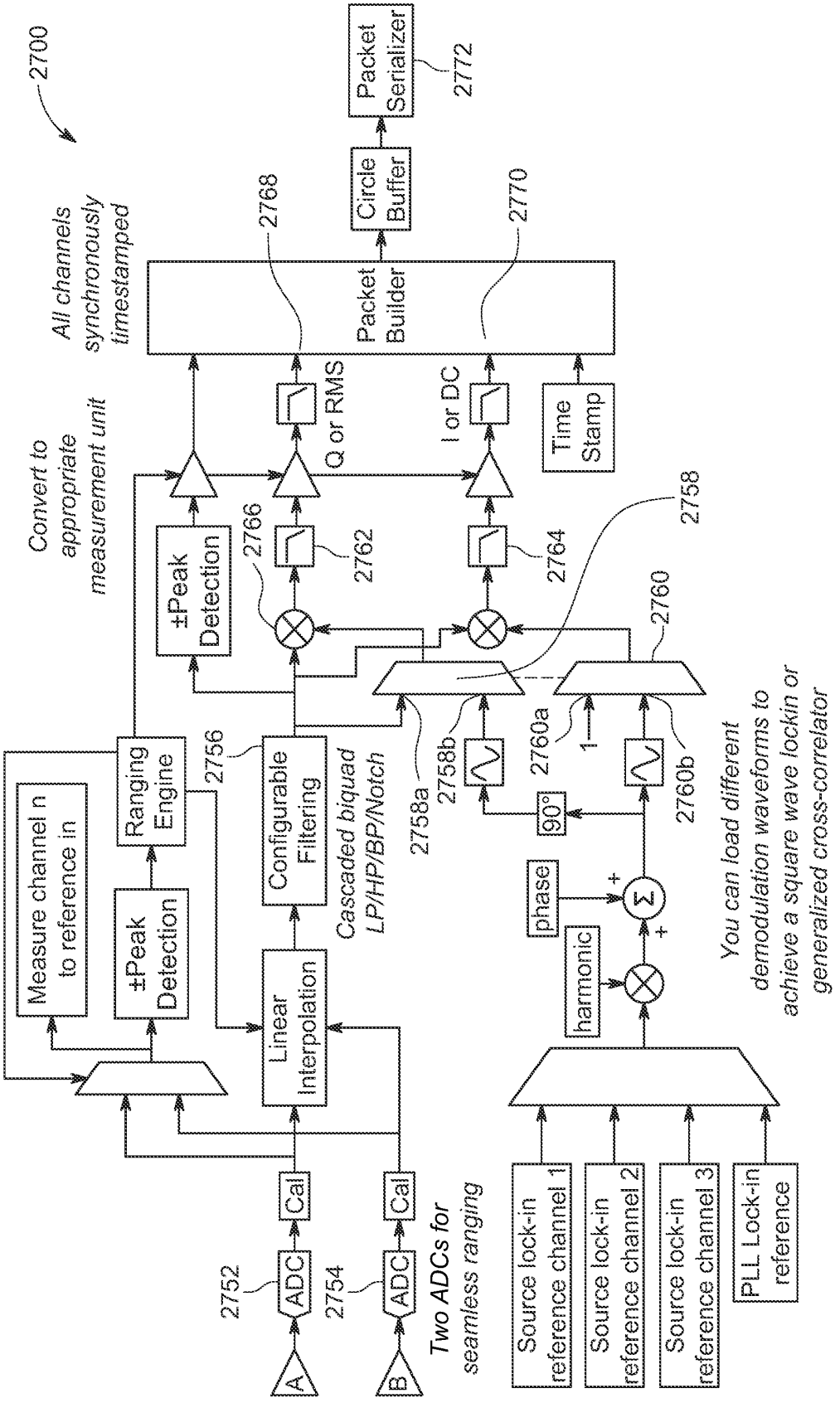

2700
All channels synchronously timestamped
Convert to appropriate measurement unit
Packet Serializer
2772
Circle Buffer
2768
2770
Packet Builder
Q or RMS
I or DC
Time Stamp
±Peak Detection
2766
2762
2764
2758
2760
Measure channel n to reference in
Ranging Engine
2756
Configurable Filtering
Cascaded biquad LP/HP/BP/Notch
2758a
2758b
2760a
1
2760b
90°
phase
harmonic
Σ
You can load different demodulation waveforms to achieve a square wave lockin or generalized cross-correlator
Linear Interpolation
Cal
Cal
2752
ADC
2754
ADC
A
B
Two ADCs for seamless ranging
Source lock-in reference channel 1
Source lock-in reference channel 2
Source lock-in reference channel 3
PLL Lock-in reference

FIG. 27

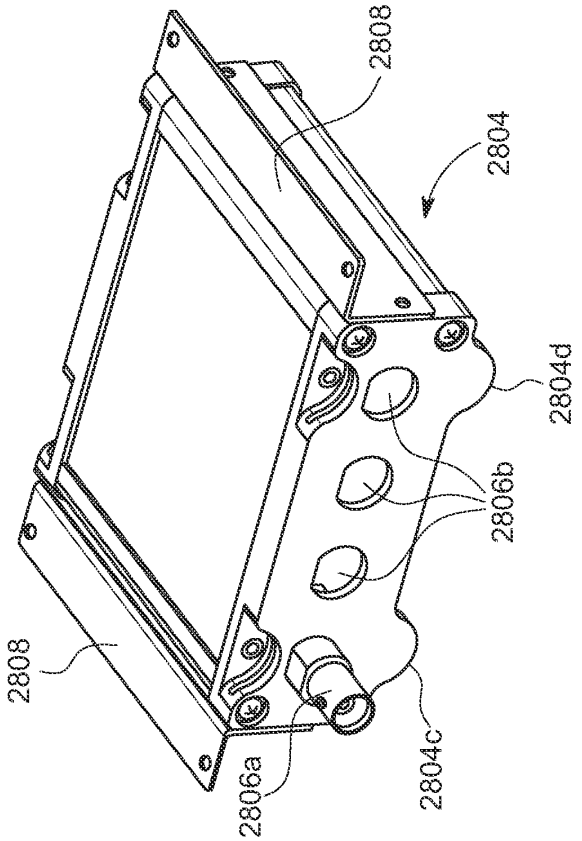


FIG. 28B

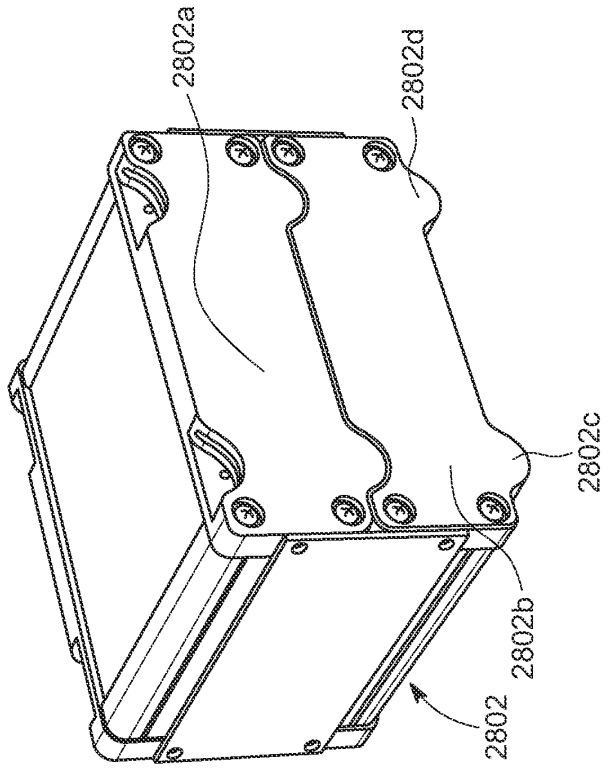


FIG. 28A

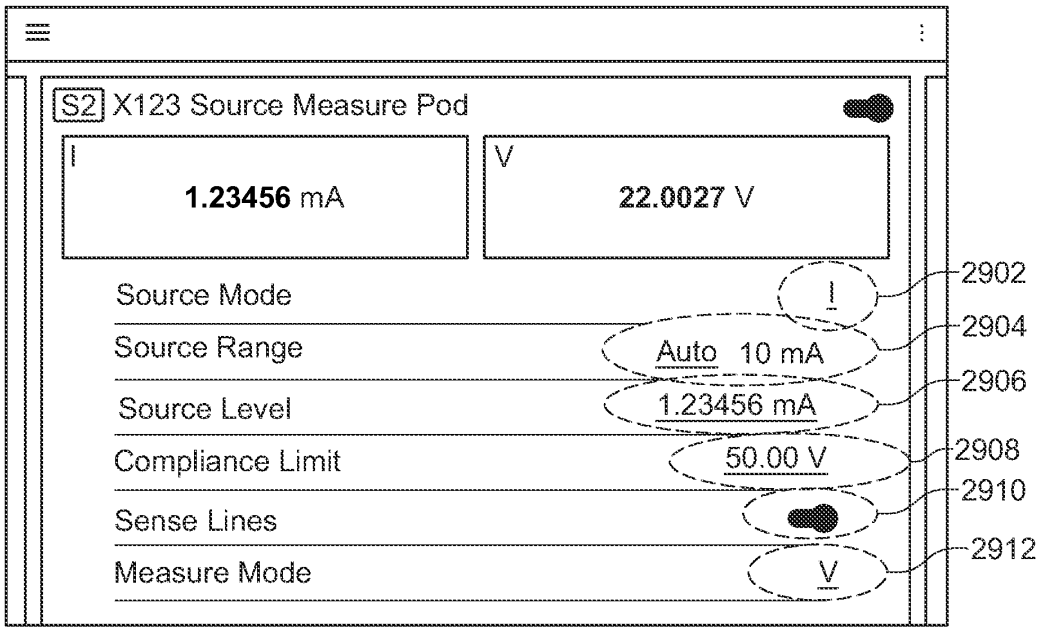


FIG. 29A

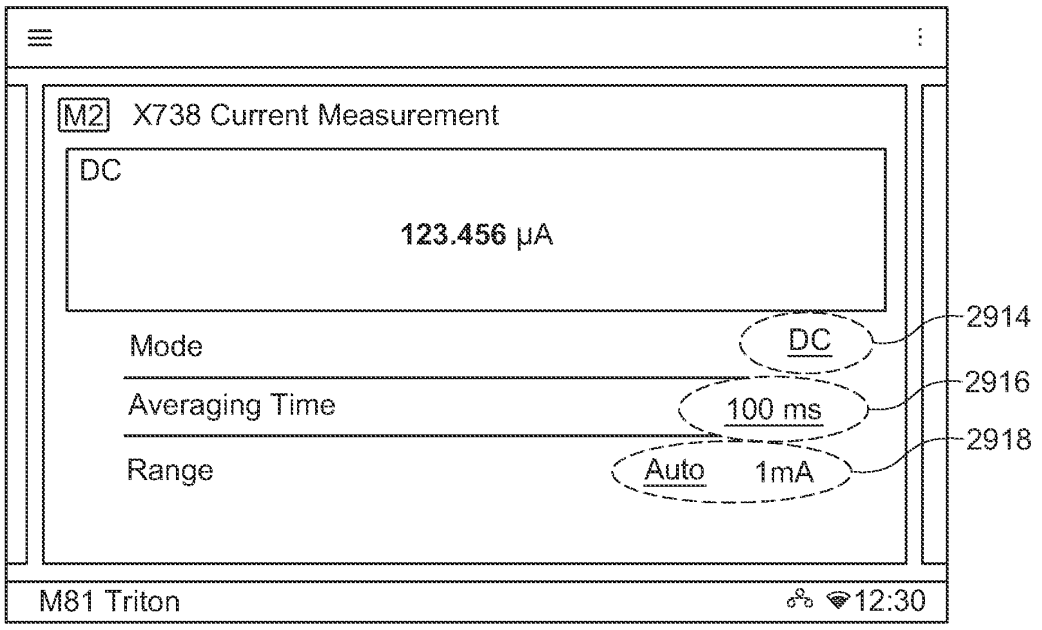


FIG. 29B