WHAT IS CLAIMED IS:

1. A method comprising:

forming a pre-patterned transistor layout by directed self-assembly (DSA);

forming a metal layer over the DSA pre-patterned transistor layout, comprising:

forming a plurality of horizontal metal lines; and

forming a plurality of vertical metal segments discontinuous from and between adjacent horizontal metal lines; and

forming one or more bridging dots each connecting one of the plurality of horizontal metal lines to one of the plurality of vertical metal segments,

wherein locations of the bridging dots determine logic functions of resulting transistor cells.

2. The method according to claim 1, comprising:

the plurality of horizontal metal lines separating the transistor layout into p-type field effect transistor (p-FET) regions, n-type field effect transistor (n-FET) regions, and input/output regions.

3. The method according to claim 1, further comprising:

dividing the plurality of horizontal metal lines into groups of at least four horizontal metal lines, each group including a power line and a ground line, and intra-cell routing and output metal lines therebetween.

4. The method according to claim 3, comprising:

forming the power line and the output metal line on opposite sides of a p-FET/n-FET region in the transistor layout; and

forming the ground line and the intra-cell routing line on opposite sides of an n-FET/p-FET region in the transistor layout.

5. The method according to claim 1, comprising:

forming a first row of the plurality of vertical metal segments aligned with gates within the transistor layout; and

forming second rows of the plurality of vertical metal segments on opposite sides of and adjacent to the first row, the vertical metal segments of the second rows being misaligned with the gates within the transistor layout.

6. The method according to claim 1, comprising:

forming the plurality of horizontal metal lines and the plurality of vertical metal segments through DSA chemical epitaxy with lamellae-forming block copolymers.

7. The method according to claim 1, comprising:

forming the bridging dots above the metal layer through DSA graphoepitaxy with cylinder and/or sphere-forming block copolymers.

8. The method according to claim 1, comprising:

forming holes within the metal layer by ultra high-resolution lithography corresponding to the locations of the bridging dots; and

filling the holes with metal forming the bridging dots within the metal layer.

9. An apparatus comprising:

a pre-patterned transistor layout formed by directed self-assembly (DSA);

a metal layer over the DSA pre-patterned transistor layout, comprising:

a plurality of horizontal metal lines; and

a plurality of vertical metal segments discontinuous from and between adjacent horizontal metal lines; and

one or more bridging dots each connecting one of the plurality of horizontal metal lines to one of the plurality of vertical metal segments,

wherein locations of the bridging dots determine logic functions of resulting transistor cells.

10. The apparatus according to claim 9, comprising:

the plurality of horizontal metal lines separating the transistor layout into p-type field effect transistor (p-FET) regions, n-type field effect transistor (n-FET) regions, and input/output regions.

11. The apparatus according to claim 9, further comprising:

the plurality of horizontal metal lines divided into groups of at least four horizontal metal lines, each group including a power line and a ground line, and intra-cell routing and output metal lines therebetween.

12. The apparatus according to claim 11, comprising:

the power line and the output metal line being on opposite sides of a p-FET/n-FET region in the transistor layout; and

the ground line and the intra-cell routing line on opposite sides of an n-FET/p-FET region in the transistor layout.

13. The apparatus according to claim 9, comprising:

a first row of the plurality of vertical metal segments being aligned with gates within the transistor layout; and

second rows of the plurality of vertical metal segments being on opposite sides of and adjacent to the first row, the vertical metal segments of the second rows being misaligned with the gates within the transistor layout.

14. The apparatus according to claim 9, comprising:

the plurality of horizontal metal lines and the plurality of vertical metal segments being formed through DSA chemical epitaxy with lamellae-forming block copolymers.

15. The apparatus according to claim 9, comprising:

the bridging dots being formed above the metal layer through DSA graphoepitaxy with cylinder and/or sphere-forming block copolymers.

16. The apparatus according to claim 9, comprising:

the bridging dots being formed within the metal layer by ultra high-resolution lithography.

17. A method comprising:

forming a pre-patterned transistor layout, comprising:

forming transistors over an active region in a substrate through directed self-assembly (DSA) chemical epitaxy of a block copolymer; and

forming contacts extending up from the active region and the transistors through DSA graphoepitaxy of the block copolymer;

forming a metal layer over the transistors and connected to the contacts, comprising:

forming a plurality of horizontal metal lines; and

forming a plurality of vertical metal segments discontinuous from and between adjacent horizontal metal lines; and

forming one or more bridging dots connecting one or more of the plurality of horizontal metal lines to one or more of the plurality of vertical metal segments,

wherein locations of the bridging dots determine logic functions of resulting transistor cells.

18. The method according to claim 17, comprising:

forming the plurality of horizontal metal lines and the plurality of vertical metal segments through DSA chemical epitaxy with lamellae-forming block copolymers.

19. The method according to claim 17, comprising:

forming the bridging dots above the metal layer through DSA graphoepitaxy with cylinder and/or sphere-forming block copolymers.

20. The method according to claim 17, comprising:

forming holes within the metal layer by ultra high-resolution lithography corresponding to the locations of the bridging dots; and

filling the holes with metal forming the bridging dots within the metal layer.

What is claimed is:

1. A method comprising: forming a pre-patterned transistor layout by directed self-assembly (DSA); forming a metal layer over the DSA pre-patterned transistor layout, comprising: forming a plurality of horizontal metal lines; and forming a plurality of vertical metal segments discontinuous from and between adjacent horizontal metal lines; forming one or more bridging dots each connecting one of the plurality of horizontal metal lines to one of the plurality of vertical metal segments; and forming the bridging dots above the metal layer through DSA graphoepitaxy with cylinder and/or sphere-forming block copolymers, wherein locations of the bridging dots determine logic functions of resulting transistor cells.

2. The method according to claim 1, comprising: the plurality of horizontal metal lines separating the transistor layout into p-type field effect transistor (p-FET) regions, n-type field effect transistor (n-FET) regions, and input/output regions.

3. The method according to claim 1, further comprising: dividing the plurality of horizontal metal lines into groups of at least four horizontal metal lines, each group including a power line and a ground line, and intra-cell routing and output metal lines therebetween.

4. The method according to claim 3, comprising: forming the power line and the output metal line on opposite sides of a p-FET/n-FET region in the transistor layout; and forming the ground line and the intra-cell routing line on opposite sides of an n-FET/p-FET region in the transistor layout.

5. The method according to claim 1, comprising: forming a first row of the plurality of vertical metal segments aligned with gates within the transistor layout; and forming second rows of the plurality of vertical metal segments on opposite sides of and adjacent to the first row, the vertical metal segments of the second rows being misaligned with the gates within the transistor layout.

6. The method according to claim 1, comprising: forming the plurality of horizontal metal lines and the plurality of vertical metal segments through DSA chemical epitaxy with lamellae-forming block copolymers.

7. The method according to claim 1, comprising: forming holes within the metal layer by ultra high-resolution lithography corresponding to the locations of the bridging dots; and filling the holes with metal forming the bridging dots within the metal layer.

8. A method comprising: forming a pre-patterned transistor layout, comprising: forming transistors over an active region in a substrate through directed self-assembly (DSA) chemical epitaxy of a block copolymer; and forming contacts extending up from the active region and the transistors through DSA graphoepitaxy of the block copolymer; forming a metal layer over the transistors and connected to the contacts, comprising: forming a plurality of horizontal metal lines; and forming a plurality of vertical metal segments discontinuous from and between adjacent horizontal metal lines; and forming one or more bridging dots connecting one or more of the plurality of horizontal metal lines to one or more of

the plurality of vertical metal segments, wherein locations of the bridging dots determine logic functions of resulting transistor cells.

9. The method according to claim 8, comprising: forming the plurality of horizontal metal lines and the plurality of vertical metal segments through DSA chemical epitaxy with lamellae-forming block copolymers.

10. The method according to claim 8, comprising: forming the bridging dots above the metal layer through DSA graphoepitaxy with cylinder and/or sphere-forming block copolymers.

11. The method according to claim 8, comprising: forming holes within the metal layer by ultra high-resolution lithography corresponding to the locations of the bridging dots; and filling the holes with metal forming the bridging dots within the metal layer.

12. A semiconductor device formed in accordance with the method of any one of the preceding claims.

13. A standard transistor layout formed in accordance with the method of any one of the claims 1-11.