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ABSTRACT

A NOVEL DIODE-LIKE PLASMA INDUCED DAMAGE PROTECTION STRUCTURE

A novel structure for a diode-like PID protection (DLPP) device structure and process are described. An N-well, three associate N⁺ regions and a P⁺ region are formed on a P substrate. The DLPP is structured as a butting diode with a polysilicon gate above the butting region. The gate is connected to a metal antenna element and to the zener like trigger element of the device. The N-well functions as a resistor and capacitor buffer between the poly gate and antenna and the substrate. The antenna picks up a portion of the plasma charge to provide a gate voltage. There is an inversion layer or accumulation layer for positive or negative plasma charge formed under the poly gate. The junction of the effective zener diode is found in the interface between the N-type inversion layer and P⁺, or N⁺ and P-type accumulation layer. Changing the shape and the size of the antenna changes the gate voltage, and subsequently the trigger voltage of the DLPP. During normal IC operation, any charge on the poly gate or associated antenna has been discharged through the N-well resistor and therefore no channel exists under the poly gate minimizing any device leakage. An alternative embodiment uses a N doped substrate with appropriately doped well and contact regions.

FIGURE 5



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