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ABSTRACT

A METHOD TO FORM ELEVATED SOURCE/DRAIN USING POLY SPACER

A method for forming a sub-quarter micron MOSFET having an elevated source/drain structure is described. A gate electrode is formed over a gate dielectric on a semiconductor substrate. Ions are implanted into the semiconductor substrate to form lightly doped regions using the gate electrode as a mask. Thereafter, dielectric spacers are formed on sidewalls of the gate electrode. A polysilicon layer is deposited overlying the semiconductor substrate, gate electrode, and dielectric spacers wherein the polysilicon layer is heavily doped. The polysilicon layer is etched back to leave polysilicon spacers on the dielectric spacers. Dopant is diffused from the polysilicon spacers into the semiconductor substrate to form source and drain regions underlying the polysilicon spacers. The polysilicon spacer on an end of the gate electrode is removed to separate the polysilicon spacers into a source polysilicon spacer and a drain polysilicon spacer thereby completing formation of a MOSFET having an elevated source/drain structure in the fabrication of an integrated circuit device.

FIGURE 7A

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