Claims

What is claimed:

1. A method of making a semiconductor device, comprising:

providing a substrate;

forming a cavity ~~in~~through a first surface of the substrate;

depositing ~~an~~ a non-conductive encapsulant in the cavity;

forming an insulating layer over the substrate and the non-conductive encapsulant;

removing a portion of the insulating layer to expose the non-conductive encapsulant;

forming a first conductive layer over the non-conductive encapsulant; and

mounting a semiconductor package over the cavity, the semiconductor package being electrically connected to the first conductive layer, wherein the non-conductive encapsulant has a coefficient of thermal expansion (CTE) selected similar to ~~the~~a CTE of the semiconductor package to reduce stress between the semiconductor package and the substrate.

2. The method of claim 1, further including forming a solder masking layer over the first conductive layer.

3. The method of claim 1, further including forming bumps between the semiconductor package and first conductive layer.

4. The method of claim 1, further including:

forming a second conductive layer in the substrate; and

forming bumps on a second surface of the substrate opposite the first surface of the substrate, the second conductive layer being electrically connected to the bumps.

5. The method of claim 1, further including:

depositing the non-conductive encapsulant with a jetting dispense process; and

molding the non-conductive encapsulant such that a surface of the non-conductive encapsulant is co-planar with the first surface of the substrate.

6. The method of claim 1, wherein the semiconductor package is a large array wafer level chip scale package.

7. A method of making a semiconductor device, comprising:

providing a substrate;

forming a cavity ~~in~~through a ~~first~~ surface of the substrate;

~~mounting~~disposing a stress compensating structure including an insulating material or a dummy die in the cavity;

planarizing a surface of the substrate with a surface of the stress compensating structure;

forming an insulating layer over the planarized surface of the substrate and the stress compensating structure;

removing a portion of the insulating layer to expose the stress compensating structure;

forming a conductive layer over the stress compensating structure; and

~~mounting~~disposing a semiconductor package over the cavity, the semiconductor package being electrically connected to the conductive layer, wherein the stress compensating structure has a coefficient of thermal expansion (CTE) selected similar to ~~the~~a CTE of the semiconductor package to reduce stress between the semiconductor package and substrate.

8. The method of claim 7, wherein the stress compensating structure includes an encapsulant.

9. The method of claim 7, wherein the stress compensating structure includes a dummy die.

10. The method of claim 9, further including depositing an encapsulant over the dummy die.

11~~1~~2. The method of claim 7, further including forming a solder masking layer over the conductive layer.

12~~1~~1. The method of claim ~~7~~9, further including forming an inductor ~~on a surface of~~over the dummy die.

13. The method of claim 7, wherein the semiconductor package is a large array wafer level chip scale package.

14. A method of making a semiconductor device, comprising:

providing a substrate;

forming a cavity ~~in~~through a ~~first~~ surface of the substrate;

disposing a stress compensating structure including an insulating or semiconductor material in the cavity with a surface of the stress compensating structure co-planar with the surface of the substrate;

forming a conductive layer over the stress compensating structure; and

~~mounting~~disposing a semiconductor package over the cavity, the semiconductor package being electrically connected to the conductive layer, wherein the stress compensating structure has a coefficient of thermal expansion (CTE) ~~selected~~ similar to ~~the~~a CTE of the semiconductor package to reduce stress between the semiconductor package and substrate.

15. The method of claim 14, further including:

forming an insulating layer over the substrate and the stress compensating structure; and

removing a portion of the insulating layer to expose the stress compensating structure.

16. The method of claim 14, wherein the stress compensating structure includes an encapsulant.

17. The method of claim 16, further including~~:~~

depositing the encapsulant with a jetting dispense process~~; and~~

~~molding the encapsulant co-planar with the first surface of the substrate~~.

18. The method of claim 14, wherein the stress compensating structure includes a dummy die.

19. The method of claim 14, further including forming a solder masking layer over the conductive layer.

20. The method of claim 14, further including forming bumps between the semiconductor package and the conductive layer.

21. A semiconductor device, comprising:

a substrate ~~having~~including a cavity formed ~~in~~through a ~~first~~ surface of the substrate;

a stress compensating structure including an insulating material or a dummy die disposed in the cavity with a surface of the stress compensating structure co-planar with the surface of the substrate an insulating layer formed over the substrate and a first portion of the stress compensating structure including an opening in the insulating layer over the stress compensating structure;

a conductive layer formed over the insulating layer stress compensating structure and in contact with the stress compensating structure; and

a semiconductor package ~~mounted~~disposed over the cavity, the semiconductor package being electrically connected to the conductive layer, wherein the stress compensating structure has a coefficient of thermal expansion (CTE) ~~selected~~ similar to ~~the~~

a CTE of the semiconductor package to reduce stress between the semiconductor package and substrate.

22. The semiconductor device of claim 21, wherein the stress compensating structure includes an encapsulant.

23. The semiconductor device of claim 21, wherein the stress compensating structure includes a dummy die with an inductor formed over the surface of the stress compensating structure ~~on its top surface~~.

24. The semiconductor device of claim 21, further including bumps formed between the semiconductor package and the conductive layer.

25. The semiconductor device of claim 21, wherein the semiconductor package is a large array wafer level chip scale package.

26. A method of making a semiconductor device, comprising:

providing a substrate;

forming a cavity through a surface of the substrate;

disposing a stress compensating structure in the cavity, wherein the stress compensating structure includes a dummy die;

forming an insulating layer over the substrate and the stress compensating structure; forming an opening in the insulating layer over the stress compensating structure;

forming an interconnect structure over the insulating layer and the stress compensating structure; and

disposing a semiconductor package including first and second contact pads over the interconnect structure with the

first and second contact pads disposed within a footprint of the cavity.

27. The method of claim 26, wherein the stress compensating structure has a coefficient of thermal expansion (CTE) similar to a CTE of the semiconductor package to reduce stress between the semiconductor package and the substrate.

28. The method of claim 26, wherein the stress compensating structure includes an insulating material.

29. The method of claim 26, further including depositing an encapsulant over the dummy die.

30. The method of claim 29, wherein a surface of the stress compensating structure is coplanar with the surface of the substrate.

31. The method of claim 26, further including:

forming an insulating layer over the substrate and the stress compensating structure; and

removing a portion of the insulating layer to expose the stress compensating structure.