CLAIMS

1. A semiconductor structure, comprising:

a base, comprising bit lines and semiconductor channels that are respectively arranged at intervals, wherein a bit line extends in a first direction, a semiconductor channel is located on partial top surface of the bit line, and in a direction perpendicular to the top surface of the bit line, and the semiconductor channel comprises a first region, a second region and a third region arranged in sequence;

a dielectric layer, located between two adjacent ones of the bit lines and on a surface of the semiconductor channel;

a first gate layer, surrounding the dielectric layer of the second region and extending in a second direction, wherein the first direction is different from the second direction;

a second gate layer, surrounding the dielectric layer of the third region, wherein, in the direction perpendicular to the top surface of the bit line, the second gate layer is spaced apart from the first gate layer; and

an insulation layer, located between two adjacent ones of the semiconductor channels on the same bit line and isolating the first gate layers and the second gate layers on two adjacent ones of the dielectric layers;

wherein the single first gate layer extends in the second direction, and surrounds two adjacent ones of the semiconductor channels respectively located on two adjacent ones of the bit lines; and the single second gate layer only surrounds the single semiconductor channel.

2. The semiconductor structure of claim 1, wherein, in a plane perpendicular to a sidewall of the semiconductor channel, the semiconductor channel surrounded by the first gate layer has a first cross section, the semiconductor channel surrounded by the second gate layer has a second cross section; and an area of the first cross section is greater than an area of the second cross section;

wherein, in a direction from the bit line pointing to the semiconductor channel, a length of the first gate layer is greater than a length of the second gate layer; and/or

wherein, in a direction perpendicular to a sidewall of the semiconductor channel, a thickness of the first gate layer is greater than a thickness of the second gate layer.

3. The semiconductor structure of claim 1, wherein the second gate layer comprises zirconium and/or at least one of lanthanide elements.

4. The semiconductor structure of claim 1, further comprises an electrical contact structure, located on a surface of the second gate layer away from the bit line and located on part of a surface of the dielectric layer of the third region.

5. The semiconductor structure of claim 1, further comprising a metal semiconductor compound structure, located at least in the bit line directly facing a bottom surface of the insulation layer.

6. The semiconductor structure of claim 5, wherein, in directions from the semiconductor channels on two sides of the insulation layer pointing to the insulation layer, a depth of the metal semiconductor compound structure is gradually increased.

7. The semiconductor structure of claim 1, wherein, in a plane perpendicular to a sidewall of the semiconductor channel, a cross-sectional area of the semiconductor channel of the first region, a cross-sectional area of the semiconductor channel of the second region, and a cross-sectional area of the semiconductor channel of the third region are decreased in sequence.

8. The semiconductor structure of claim 7, wherein the dielectric layer comprises:

a first dielectric layer, located between the adjacent bit lines and between the first regions of the semiconductor channels respectively on the adjacent bit lines;

a second dielectric layer, located on a sidewall of the semiconductor channel of the first region and a sidewall of the first dielectric layer of the first region;

a third dielectric layer, surrounding the sidewall of the semiconductor channel of the second region; and

a fourth dielectric layer, surrounding the sidewall of the semiconductor channel of the third region and located on a top surface of the semiconductor channel.

9. The semiconductor structure of claim 8, wherein the first gate layer is at least located on part of a top surface of the first dielectric layer and part of a top surface of the second dielectric layer; and the second gate layer is at least located on part of a top surface of the third dielectric layer.

10. The semiconductor structure of claim 1, wherein the insulation layer comprises:

a first insulation layer, located between the dielectric layers and between the first gate layers of two adjacent ones of the semiconductor channels, and extending in the second direction, wherein a top surface of the first insulation layer is not lower than a top surface of the third region;

a second insulation layer, located on a top surface of the first gate layer, and between the first insulation layer and the second gate layer; and

a third insulation layer, located on a top surface of the second gate layer, and between the second insulation layer and the dielectric layer.

11. A method for manufacturing a semiconductor structure, comprising:

providing a base, comprising bit lines and semiconductor channels that are respectively arranged at intervals, wherein a bit line extends in a first direction, a semiconductor channel is located on partial top surface of the bit line, and in a direction perpendicular to a top surface of the bit line, the semiconductor channel comprises a first region, a second region, and a third region arranged in sequence;

forming a dielectric layer, wherein the dielectric layer is located between two adjacent ones of the bit lines and on a surface of the semiconductor channel;

forming a first gate layer, wherein the first gate layer surrounds the dielectric layer of the second region and extends in a second direction, the first direction being different from the second direction;

forming a second gate layer, wherein the second gate layer surrounds the dielectric layer of the third region and in the direction perpendicular to the top surface of the bit line, the second gate layer is spaced apart from the first gate layer; and

forming an insulation layer, wherein the insulation layer is located between two adjacent ones of the semiconductor channels on the same bit line;

wherein the single first gate layer extends in the second direction, and surrounds two adjacent ones of the semiconductor channels respectively located on two adjacent ones of the bit lines; and the single second gate layer only surrounds the single semiconductor channel.

12. The manufacturing method according to claim 11, wherein providing the base comprises:

providing an initial base, wherein initial first dielectric layers extending in the first direction are provided in the initial base; and

patterning the initial base and the initial first dielectric layers, to form the bit lines and the semiconductor channels that are respectively arranged at intervals, and the initial first dielectric layers located between adjacent bit lines, wherein top surfaces of the initial first

dielectric layers are not lower than top surfaces of the semiconductor channels; grooves are defined by sidewalls of the semiconductor channels, sidewalls of the initial first dielectric layers, and partial top surfaces of the bit lines; and the grooves extend in a second direction.

13. The manufacturing method of claim 12, wherein forming the dielectric layer, the first gate layer, the second gate layer and the insulation layer comprises:

forming a first dielectric layer between the two adjacent bit lines and between the first regions of the semiconductor channels respectively on the two adjacent bit lines;

forming second dielectric layers on sidewalls of a groove of the first region;

forming a first insulation layer, wherein the first insulation layer is located in the groove and isolates the adjacent second dielectric layers, and a top surface of the first insulation layer is not lower than a top surface of the semiconductor channel;

forming a third dielectric layer and the first gate layer on a sidewall of the groove of the second region, wherein a top surface of the third dielectric layer is higher than a top surface of the first gate layer;

forming a second insulation layer, wherein the second insulation layer is located between the first insulation layer and the third dielectric layer;

forming a fourth dielectric layer and the second gate layer on the sidewall of the groove of the third region, wherein a top surface of the fourth dielectric layer is higher than a top surface of the second gate layer; and

forming a third insulation layer, wherein the third insulation layer is located between the second insulation layer and the fourth dielectric layer; and wherein the first dielectric layer, the second dielectric layer, the third dielectric layer and the fourth dielectric layer together constitute the dielectric layer; and the first insulation layer, the second insulation layer and the third insulation layer together constitute the insulation layer.

14. The manufacturing method of claim 13, wherein the step of forming the first dielectric layer, the second dielectric layer and the first insulation layer comprises:

forming initial second dielectric layers on the sidewalls of the groove, wherein a first gap is provided between the adjacent initial second dielectric layers;

forming the first insulation layer in the first gap; and

etching the initial first dielectric layers and the initial second dielectric layers by using the first insulation layer as a mask, to form the first dielectric layer and the second dielectric layer.

15. The manufacturing method of claim 14, wherein, before the first insulation layer is formed, and after the initial second dielectric layer is formed, metal silicidation is performed on part of the top surface of the bit line exposed from the initial second dielectric layers, to form a metal semiconductor compound structure.

16. The manufacturing method of claim 13, wherein forming the third dielectric layer, the first gate layer and the second insulation layer comprises:

forming an initial third dielectric layer on the sidewall of the semiconductor channel of the second region and the third region, wherein a second gap is provided between the initial third dielectric layer and the first insulation layer;

forming the first gate layer in part of the second gap of the second region;

forming the second insulation layer in the remaining second gap; and

etching the initial third dielectric layer by using the second insulation layer as a mask, to form the third dielectric layer.

17. The manufacturing method of claim 13, wherein forming the fourth dielectric layer, the second gate layer and the third insulation layer comprises:

forming the fourth dielectric layer on the sidewall of the third region, wherein a third gap is provided between the fourth dielectric layer and the second insulation layer;

forming the second gate layer in part of the third gap; and

forming the third insulation layer in the remaining third gap.

18. The manufacturing method of claim 17, wherein, after the second gate layer is formed, and before the third insulation layer is formed, the method further comprises doping zirconium and/or at least one of lanthanide elements in the second gate layer.

19. The manufacturing method according to claim 12, further comprising forming an electrical contact structure, which comprises:

patterning the insulation layer to expose the second gate layer to form a through via; and

forming the electrical contact structure in the through via.