(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
25 January 2001 (25.01.2001)

PCT

(10) International Publication Number
WO 01/06421 A1

(51) International Patent Classification[7]: G06F 17/50, 9/455

(74) Agent: NEWMAN, David, B., Jr.; David Newman Chartered, P.O. Box 2728, La Plata, MD 20646-2728 (US).

(21) International Application Number: PCT/US00/14257

(22) International Filing Date: 24 May 2000 (24.05.2000)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
09/354,955 16 July 1999 (16.07.1999) US

(71) Applicant: ATMEL CORPORATION [US/US]; 2325 Orchard Parkway, San Jose, CA 95131 (US).

(72) Inventors: MASON, Martin, Thomas; 2249 Cherrystone Drive, San Jose, CA 95128 (US). MCCONNELL, David, Andrew; 3208 Fiji Lane, Alameda, CA 94502 (US). DASARI, Ajithkumar, Venkata; Apartment 236, 100 Buckingham Drive, Santa Clara, CA 95051 (US).

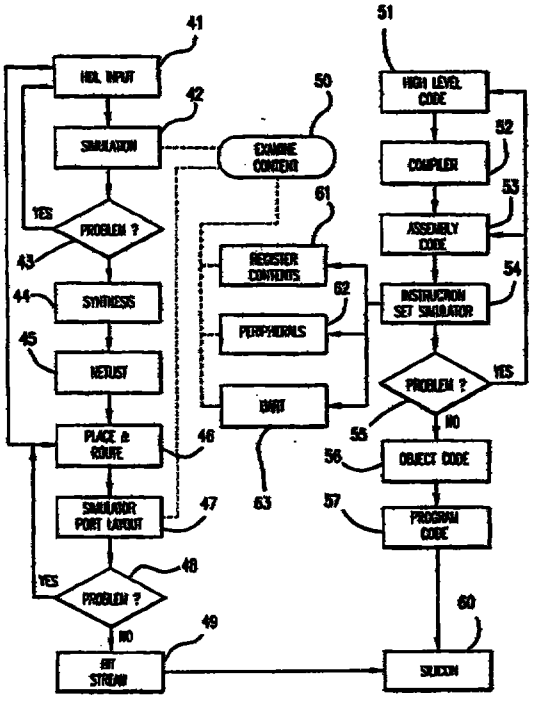
(81) Designated States *(national)*: AM, AT, AU, BB, BG, BR, BY, CA, CH, CN, CZ, DE, DK, EE, ES, FI, GB, GE, HU, IS, JP, KE, KG, KP, KR, KZ, LK, LR, LT, LU, LV, MD, MG, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, TJ, TM, TT, UA, UG, UZ, VN.

(84) Designated States *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZW), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).

Published:
— *With international search report.*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: SOFTWARE TOOL TO ALLOW FILED PROGRAMMABLE SYSTEM LEVEL DEVICES



(57) Abstract: A method and system for co-verifying a hardware simulation of a field-programmable-system-level integrated circuit (FPSLIC) and a software simulation of the field-programmable-system level integrated circuit. An FPSLIC is simulated (42) in hardware, and a simulator-port layout (47) of the FPSLIC device is generated. In software, the method separately simulates, with an instruction-set simulator (54), the FPSLIC device and outputs register contents (61) from the instruction-set software. The contents from the simulator-port layout (47) are verified with the register contents (61). Additionally, the method may further include outputting peripheral contents (62) from the instruction-set simulator (54), and verifying contents (50) from the simulator-port layout (47) with the peripheral contents (62). UART contents (63) also may be outputted form the instruction-set simulator (54), and verified with contents from the simulator-port layout (47) with the UART contents (63).

WO 01/06421 A1