SILVER-SELENIDE/CHALCOGENIDE GLASS STACK FOR RESISTANCE VARIABLE MEMORY

FIELD OF THE INVENTION

[0001] The invention relates to the field of random access memory (RAM) devices formed using a resistance variable material, and in particular to a resistance variable memory element formed using chalcogenide glass.

BACKGROUND OF THE INVENTION

[0002] A well known semiconductor component is semiconductor memory, such as a random access memory (RAM). RAM permits repeated read and write operations on memory elements. Typically, RAM devices are volatile, in that stored data is lost once the power source is disconnected or removed. Non-limiting examples of RAM devices include dynamic random access memory (DRAM), synchronized dynamic random access memory (SDRAM) and static random access memory (SRAM). In addition, DRAMS and SDRAMS also typically store data in capacitors which require periodic refreshing to maintain the stored data.

[0003] In recent years, the number and density of memory elements in memory devices have been increasing. Accordingly, the size of each element has been shrinking, which in the case of DRAMs also shortens the element's data holding time. Typically, a DRAM memory device relies on element capacity for data storage and receives a refresh command in a conventional standardized cycle, about every 100 milliseconds. However, with increasing element number and density, it is becoming more and more difficult to refresh all memory elements at least once within a refresh period. In addition, refresh operations consume power.

[0004] Recently resistance variable memory elements, which includes programmable conductor memory elements, have been investigated for suitability as semi-volatile and non-volatile random access memory elements. Kozicki et al. in

U.S. Patent Nos. 5,761,115; 5,896,312; 5,914,893; and 6,084,796, discloses a programmable conductor memory element including an insulating dielectric material formed of a chalcogenide glass disposed between two electrodes. A conductive material, such as silver, is incorporated into the dielectric material. The resistance of the dielectric material can be changed between high resistance and low resistance states. The programmable conductor memory is normally in a high resistance state when at rest. A write operation to a low resistance state is performed by applying a voltage potential across the two electrodes. The mechanism by which the resistance of the element is changed is not fully understood. In one theory suggested by Kozicki et al., the conductively-doped dielectric material undergoes a structural change at a certain applied voltage with the growth of a conductive dendrite or filament between the electrodes effectively interconnecting the two electrodes and setting the memory element in a low resistance state. The dendrite is thought to grow through the resistance variable material in a path of least resistance.

[0005] The low resistance state will remain intact for days or weeks after the voltage potentials are removed. Such material can be returned to its high resistance state by applying a reverse voltage potential between the electrodes of at least the same order of magnitude as used to write the element to the low resistance state. Again, the highly resistive state is maintained once the voltage potential is removed. This way, such a device can function, for example, as a resistance variable memory element having two resistance states, which can define two logic states.

[0006] One preferred resistance variable material comprises a chalcogenide glass. A specific example is germanium-selenide (Ge_xSe_{100-x}) comprising silver (Ag). One method of providing silver to the germanium-selenide composition is to initially form a germanium-selenide glass and then deposit a thin layer of silver upon the glass, for example by sputtering, physical vapor deposition, or other known techniques in the art. The layer of silver is irradiated, preferably with electromagnetic energy at a wavelength less than 600 nanometers, so that the energy passes through the silver and to the silver/glass interface, to break a chalcogenide

bond of the chalcogenide material such that the glass is doped or photodoped with silver. Silver may also be provided to the glass by processing the glass with silver, as in the case of a silver-germanium-selenide glass. Another method for providing metal to the glass is to provide a layer of silver-selenide on a germanium-selenide glass.

[0007] In accordance with the current methods of incorporating silver into the glass, the degree and nature of the crystallinity of the chalcogenide material of the memory element has a direct bearing upon its programming characteristics. Accordingly, current processes for incorporating silver require the precise control of the amounts of Ge_xSe_{100-x} glass and silver, so as not to incorrectly dope the glass and improperly alter the crystallinity of the chalcogenide material. Current processes also require careful selection of the exact stoichiometry of the glass to ensure that silver is incorporated into the glass while the glass backbone remains in the glass forming region.

[0008] Furthermore, during semiconductor processing and/or packaging of a fabricated original structure that incorporates the memory element, the element undergoes thermal cycling or heat processing. Heat processing can result in substantial amounts of silver migrating into the memory element uncontrollably. Too much silver incorporated into the memory element may result in faster degradation, i.e., a short life, and eventually device failure.

[0009] Accordingly, there is a need for a resistance variable memory element having improved memory retention and switching characteristics. There is also a need for a chalcogenide glass memory element that is resistant to silver migration during thermal processing.

BRIEF SUMMARY OF THE INVENTION

[0010] In a first embodiment, the invention provides a resistance variable memory element and a method of forming the resistance variable memory element in which a metal containing layer is formed between a first chalcogenide glass layer

and a second glass layer. One or both of the glass layers may be doped with a metal and one or more metal containing layers may be provided between the glass layers.

[0011] In a narrower aspect of the first embodiment, the invention provides a memory element and a method of forming the memory element in which at least one layer of silver-selenide is formed between a first chalcogenide glass layer and a second glass layer. The second glass layer may also be a chalcogenide glass layer. The stack of layers comprising a first chalcogenide glass, a silver-selenide layer, and a second glass layer are formed between two conductive layers or electrodes. In a variation of the first embodiment of the invention, the stack of layers may contain more than one silver-selenide layer between the chalcogenide glass layer and the second glass layer. In another variation of the first embodiment, the first chalcogenide glass layer may contain multiple chalcogenide glass layers and the second glass layer may contain multiple glass layers. Thus the stack of layers may contain one or more silver selenide layers in serial contact with each other formed between a multi-layered chalcogenide glass layer and a multi-layered second glass layer. In yet another variation of the first embodiment, one or more of each of the first chalcogenide glass layers and the second glass layers may contain a metal dopant, for example, a silver dopant.

[0012] According to a second embodiment, the invention provides a memory element and a method of forming a memory element comprising a plurality of alternating layers of chalcogenide glass and metal containing layers, whereby the layers start with a first chlacogenide glass layer and end with a last chalcogenide glass layer, with the first chalcogenide glass layer contacting a first electrode and the last chalcogenide glass layer contacting a second electrode. Thus, the plurality of alternating layers of chalcogenide glass layers and metal containing layers are stacked between two electrodes. The metal containing layers preferably comprises a silver-chalcogenide, such as silver-selenide. In a variation of the second embodiment, the metal containing layers may each contain a plurality of metal containing layers. In another variation of the second embodiment, the chalcogenide glass layers may each

contain a plurality of chalcogenide glass layers. In yet another variation of this embodiment, one or more of the chalcogenide glass layers may contain a metal dopant, for example, a silver dopant.

BRIEF DESCRIPTION OF THE DRAWINGS

[0013] These and other features and advantages of the invention will be better understood from the following detailed description, which is provided in connection with the accompanying drawings.

[0014] FIG. 1 illustrates a cross-sectional view of a memory element fabricated in accordance with a first embodiment of the invention and at an initial stage of processing.

[0015] FIG. 2 illustrates a cross-sectional view of the memory element of FIG. 1 at a stage of processing subsequent to that shown in FIG. 1.

[0016] FIG. 3 illustrates a cross-sectional view of the memory element of FIG. 1 at a stage of processing subsequent to that shown in FIG. 2.

[0017] FIG. 4 illustrates a cross-sectional view of the memory element of FIG. 1 at a stage of processing subsequent to that shown in FIG. 3.

[0018] FIG. 5 illustrates a cross-sectional view of the memory element of FIG. 1 at a stage of processing subsequent to that shown in FIG. 4.

[0019] FIG. 6 illustrates a cross-sectional view of the memory element of FIG. 1 at a stage of processing subsequent to that shown in FIG. 5.

[0020] FIG. 7 illustrates a cross-sectional view of the memory element of FIG. 1 at a stage of processing subsequent to that shown in FIG. 6.

[0021] FIG. 8 illustrates a cross-sectional view of the memory element of FIG. 1 in accordance with a variation of the first embodiment of the invention at a stage of processing subsequent to that shown in FIG. 4.

[0022] FIG. 9 illustrates a cross-sectional view of a second embodiment of the memory element of the invention at a stage of processing subsequent to that shown in FIG. 4.

[0023] FIG. 10 illustrates a cross-sectional view of a variation of the second embodiment of the memory element of the invention at a stage of processing subsequent to that shown in FIG. 4.

[0024] FIG. 11 illustrates a computer system having a memory element formed according to the invention.

DETAILED DESCRIPTION OF THE INVENTION

[0025] In the following detailed description, reference is made to various specific embodiments of the invention. These embodiments are described with sufficient detail to enable those skilled in the art to practice the invention. It is to be understood that other embodiments may be employed, and that various structural, logical and electrical changes may be made without departing from the spirit or scope of the invention.

[0026] The term "substrate" used in the following description may include any supporting structure including but not limited to a semiconductor substrate that has an exposed substrate surface. A semiconductor substrate should be understood to include silicon-on-insulator (SOI), silicon-on-sapphire (SOS), doped and undoped semiconductors, epitaxial layers of silicon supported by a base semiconductor foundation, and other semiconductor structures. When reference is made to a semiconductor substrate or wafer in the following description, previous process steps may have been utilized to form regions or junctions in or over the base semiconductor or foundation.

[0027] The term "silver" is intended to include not only elemental silver, but silver with other trace metals or in various alloyed combinations with other metals as known in the semiconductor industry, as long as such silver alloy is

conductive, and as long as the physical and electrical properties of the silver remain unchanged.

[0028] The term "silver-selenide" is intended to include various species of silver-selenide, including some species which have a slight excess or deficit of silver, for instance, Ag_2Se, $Ag_{2+x}Se$, and $Ag_{2-x}Se$.

[0029] The term "semi-volatile memory" is intended to include any memory device or element which is capable of maintaining its memory state after power is removed from the device for a prolonged period of time. Thus, semi-volatile memory devices are capable of retaining stored data after the power source is disconnected or removed. Accordingly, the term "semi-volatile memory" is also intended to include not only semi-volatile memory devices, but also non-volatile memory devices.

[0030] The term "resistance variable material" is intended to include chalcogenide glasses, and chalcogenide glasses comprising a metal, such as silver. For instance the term "resistance variable material" includes silver doped chalcogenide glasses, silver-germanium-selenide glasses, and chalcogenide glass comprising a silver selenide layer.

[0031] The term "resistance variable memory element" is intended to include any memory element, including programmable conductor memory elements, semi-volatile memory elements, and non-volatile memory elements which exhibit a resistance change in response to an applied voltage.

[0032] The term "chalcogenide glass" is intended to include glasses that comprise an element from group VIA (or group 16) of the periodic table. Group VIA elements, also referred to as chalcogens, include sulfur (S), selenium (Se), tellurium (Te), polonium (Po), and oxygen (O).

[0033] The invention will now be explained with reference to FIGS. 1-10, which illustrate exemplary embodiments of a resistance variable memory element

100 in accordance with the invention. FIG. 1 depicts a portion of an insulating layer 12 formed over a semiconductor substrate 10, for example, a silicon substrate. It should be understood that the resistance variable memory element can be formed on a variety of substrate materials and not just semiconductor substrates such as silicon. For example, the insulating layer 12 may be formed on a plastic substrate. The insulating layer 12 may be formed by any known deposition methods, such as sputtering by chemical vapor deposition (CVD), plasma enhanced CVD (PECVD) or physical vapor deposition (PVD). The insulating layer 12 may be formed of a conventional insulating oxide, such as silicon oxide (SiO_2), a silicon nitride (Si_3N_4), or a low dielectric constant material, among many others.

[0034] A first electrode 14 is next formed over the insulating layer 12, as also illustrated in FIG. 1. The first electrode 14 may comprise any conductive material, for example, tungsten, nickel, tantalum, aluminum, platinum, or silver, among many others. A first dielectric layer 15 is next formed over the first electrode 14. The first dielectric layer 15 may comprise the same or different materials as those described above with reference to the insulating layer 12.

[0035] Referring now to FIG. 2, an opening 13 extending to the first electrode 14 is formed in the first dielectric layer 15. The opening 13 may be formed by known methods in the art, for example, by a conventional patterning and etching process. A first chalcogenide glass layer 17 is next formed over the first dielectric layer 15, to fill in the opening 13, as shown in FIG. 3.

[0036] According to a first embodiment of the invention, the first chalcogenide glass layer 17 is a germanium-selenide glass having a Ge_xSe_{100-x} stoichiometry. The preferred stoichiometric range is between about $Ge_{20}Se_{80}$ to about $Ge_{43}Se_{57}$ and is more preferably about $Ge_{40}Se_{60}$. The first chalcogenide glass layer 17 preferably has a thickness from about 100 Å to about 1000 Å and is more preferably 150 Å.

[0037] The first chalcogenide glass layer, acts as a glass backbone for allowing a metal containing layer, such as a silver-selenide layer, to be directly deposited thereon. The use of a metal containing layer, such as a silver-selenide layer, in contact with the chalcogenide glass layer makes it unnecessary to provide a metal (silver) doped chalcogenide glass, which would require photodoping of the substrate with ultraviolet radiation. However, it is possible to also metal (silver) dope the chalcogenide glass layer, which is in contact with the silver-selenide layer, as an optional variant.

[0038] The formation of the first chalcogenide glass layer 17, having a stoichiometric composition in accordance with the invention may be accomplished by any suitable method. For instance, evaporation, co-sputtering germanium and selenium in the appropriate ratios, sputtering using a germanium-selenide target having the desired stoichiometry, or chemical vapor deposition with stoichiometric amounts of GeH_4 and SeH_2 gases (or various compositions of these gases), which result in a germanium-selenide film of the desired stoichiometry are examples of methods which may be used to form the first chalcogenide glass layer 17.

[0039] Referring now to FIG. 4, a first metal containing layer 18, preferably silver-selenide, is deposited over the first chalcogenide glass layer 17. Any suitable metal containing layer may be used. For instance, suitable metal containing layers include silver-chalcogenide layers. Silver sulfide, silver oxide, and silver telluride are all suitable silver-chalcogenides that may be used in combination with any suitable chalcogenide glass layer. A variety of processes can be used to form the silver-selenide layer 18. For instance, physical vapor deposition techniques such as evaporative deposition and sputtering may be used. Other processes such as chemical vapor deposition, co-evaporation or depositing a layer of selenium above a layer of silver to form silver-selenide can also be used.

[0040] The layers may be any suitable thickness. The thickness of the layers depend upon the mechanism for switching. The thickness of the layers is such

that the metal containing layer is thicker than the first chalcogenide glass layer. The metal containing layer is also thicker than a second glass layer, described below. More preferably, the thickness of the layers are such that a ratio of the silver-selenide layer thickness to the first chalcogenide glass layer thickness is between about 5:1 and about 1:1. In other words, the thickness of the silver-selenide layer is between about 1 to about 5 times greater than the thickness of the first chalcogenide glass layer. Even more preferably, the ratio is between about 3.1:1 and about 2:1 silver-selenide layer thickness to first chalcogenide glass layer thickness.

[0041] Referring now to FIG. 5 a second glass layer 20 is formed over the first silver-selenide layer 18. The second glass layer allows deposition of silver above the silver-selenide layer since silver cannot be directly deposited on silver-selenide. Also, it is believed that the second glass layer may prevent or regulate migration of metal, such as silver, from an electrode into the element. Accordingly, although the exact mechanism by which the second glass layer may regulate or prevent metal migration is not clearly understood, the second glass layer may act as a silver diffusion control layer. For use as a diffusion control layer, any suitable glass may be used, including but not limited to chalcogenide glasses. The second chalcogenide glass layer may, but need not, have the same stoichiometric composition as the first chalcogenide glass layer, e.g., GexSe100-x. Thus, the second glass layer 20 may be of a different material, different stoichiometry, and/or more rigid than the first chalcogenide glass layer 17.

[0042] The second glass layer 20, when used as a diffusion control layer may generally comprise any suitable glass material with the exception of SiGe and GaAs. Suitable glass material compositions for the second glass layer 20 include, SiSe (silicon-selenide), AsSe (arsenic-selenide, such as As_3Se_2), GeS (germanium-sulfide), and combinations of Ge, Ag, and Se. Any one of the suitable glass materials may further comprise small concentrations, i.e. less than about 3%, of dopants to include nitrides, metal, and other group 13-16 elements from the periodic table.

[0043] The thickness of the layers are such that the silver-selenide layer thickness is greater than the thickness of the second glass layer. Preferably, a ratio of the silver-selenide layer thickness to the second glass layer thickness is between about 5:1 and about 1:1. More preferably, the ratio of the silver-selenide layer thickness to the thickness of the second glass layer is between about 3.3:1 and about 2:1 silver-selenide layer thickness to second glass layer thickness. The second glass layer 20 preferably has a thickness between about 100 Å to about 1000 Å and is more preferably 150 Å.

[0044] The formation of the second glass layer 20 may be accomplished by any suitable method. For instance, chemical vapor deposition, evaporation, co-sputtering, or sputtering using a target having the desired stoichiometry, may be used.

[0045] Referring now to FIG. 6, a second conductive electrode material 22 is formed over the second glass layer 20. The second conductive electrode material 22 may comprise any electrically conductive material, for example, tungsten, tantalum, titanium, or silver, among many others. Typically, the second conductive electrode material 22 comprises silver. Thus, advantageously, the second glass layer 20 may be chosen to considerably slow or prevent migration of electrically conductive metals, such as silver, through the resistance variable memory element 100.

[0046] Referring now to FIG. 7, one or more additional dielectric layers 30 may be formed over the second electrode 22 and the first dielectric layer 15 to isolate the resistance variable memory element 100 from other structure fabrication over the substrate 10. Conventional processing steps can then be carried out to electrically couple the second electrode 22 to various circuits of memory arrays.

[0047] In accordance with a variation of the first embodiment of the invention, one or more layers of a metal containing material, such as silver-selenide may be deposited on the first chalcogenide glass layer 17. Any number of silver-

selenide layers may be used. As shown in FIG. 8, an optional second silver-selenide layer 19 may be deposited on the first silver-selenide layer 18 subsequent to the processing step shown in FIG. 4.

[0048] The thickness of the layers is such that the total thickness of the combined metal containing layers, e.g. silver-selenide layers, is greater than or equal to the thickness of the first chalcogenide glass layer. The total thickness of the combined metal containing layers is also greater than the thickness of a second glass layer. It is preferred that the total thickness of the combined metal containing layers is between about 1 to about 5 times greater than the thickness of the first chalcogenide glass layer and accordingly between about 1 to about 5 times greater than the thickness of the second glass layer. It is even more preferred that the total thickness of the combined metal containing layers is between about 2 to about 3.3 times greater than the thicknesses of the first chalcogenide glass layer and the second glass layer.

[0049] In accordance, with yet another variation of the invention, the first chalcogenide glass layer may comprise one or more layers of a chalcogenide glass material, such as germanium-selenide. The second glass layer may also comprise one or more layers of a glass material. Any suitable number of layers may be used to comprise the first chalcogenide glass layer and/or the second glass layer. However it is to be understood that the total thickness of the metal containing layer(s) should be thicker than the total thickness of the one or more layers of chalcogenide glass and additionally the total thickness of the metal containing layer(s) should be thicker than the total thickness of the one or more layers of the second glass layer. Preferably a ratio of the total thickness of the metal containing layer(s) to the total thickness of the one or more layers of chalcogenide glass is between about 5:1 and about 1:1. Also, preferably a ratio of the total thickness of the metal containing layer(s) to the total thickness of the one or more layers of the second glass is between about 5:1 and about 1:1. It is even more preferred that the total thickness of the metal containing layer(s) is between about 2 to about 3.3 times greater than

the total thicknesses of the combined one or more layers of chalcogenide glass and the total thickness of the combined one or more layers of the second glass

[0050] In accordance with yet another variant of the invention, one or more of the chalcogenide glass layers and second glass layers may also be doped with a dopant, such as a metal, preferably silver.

[0051] Referring now to FIG. 9, which shows a second embodiment of the invention subsequent to the processing step shown in FIG. 4, the stack of layers formed between the first and second electrodes may include alternating layers of chalcogenide glass and a metal containing layer such as a silver-selenide layer. As shown in FIG. 9, a first chalcogenide glass layer 17 is stacked atop a first electrode 14, a first silver-selenide layer 18 is stacked atop the first chalcogenide glass layer 17, a second chalcogenide glass layer 117 is stacked atop the first silver-selenide layer 18, a second silver-selenide layer 118 is stacked atop the second chalcogenide glass layer 117, a third chalcogenide glass layer 217 is stacked atop the second silver-selenide layer 118, a third silver-selenide layer 218 is stacked atop the third chalcogenide glass layer 217, and a fourth chalcogenide glass layer is stacked atop the third silver-selenide layer 218. The second conductive electrode 22 is formed over the fourth chalcogenide glass layer.

[0052] In accordance with the second embodiment, the stack comprises at least two metal containing layers and at least three chalcogenide glass layers. However, it is to be understood that the stack may comprise numerous alternating layers of chalcogenide glass and silver-selenide, so long as the alternating layers start with a first chalcogenide glass layer and end with a last chalcogenide glass layer, with the first chalcogenide glass layer contacting a first electrode and the last chalcogenide glass layer contacting a second electrode. The thickness and ratios of the alternating layers of silver-selenide and chalcogenide glass are the same as described above, in that the silver-selenide layers are preferably thicker than connecting chalcogenide glass layers, in a ratio of between about 5:1 and about 1:1 silver-selenide layer to

connected chalcogenide glass layer, and more preferably between about 3.3:1 and 2:1 silver-selenide layer to connected chalcogenide glass layer.

[0053] In a variation of the second embodiment, one or more layers of a metal containing material, such as silver-selenide may be deposited between the chalcogenide glass layers. Any number of silver-selenide layers may be used. As shown FIG. 10 at a processing step subsequent to that shown in FIG. 4, an additional silver-selenide layer 418 may be deposited on the first silver-selenide layer 18 and an additional silver-selenide layer 518 may be deposited on the third silver-selenide layer 218 .

[0054] In accordance, with yet another variation of the invention, each of the chalcogenide glass layers may comprise one or more thinner layers of a chalcogenide glass material, such as germanium-selenide. Any suitable number of layers may be used to comprise the chalcogenide glass layers.

[0055] In yet another variation of the second embodiment of the invention, one or more of the chalcogenide glass layers may also be doped with a dopant such as a metal, preferably comprising silver.

[0056] Devices constructed according to the first embodiment of the invention, particularly, those having a silver-selenide layer disposed between two chalcogenide glass layers, show improved memory retention and write/erase performance over conventional memory devices. These devices have also shown low resistance memory retention better than 1200 hours at room temperature. The devices switch at pulse widths less than 2 nanoseconds compared with conventional doped resistance variable memory elements that switch at about 100 nanoseconds.

[0057] Although the embodiments described above refer to the formation of only one resistance variable memory element 100, it must be understood that the invention contemplates the formation of any number of such resistance variable

memory elements, which can be fabricated in a memory array and operated with memory element access circuits.

[0058] FIG. 10 illustrates a typical processor-based system 400 which includes a memory circuit 448, for example a programmable conductor RAM, which employs resistance variable memory elements fabricated in accordance with the invention. A processor system, such as a computer system, generally comprises a central processing unit (CPU) 444, such as a microprocessor, a digital signal processor, or other programmable digital logic devices, which communicates with an input/output (I/O) device 446 over a bus 452. The memory 448 communicates with the system over bus 452 typically through a memory controller.

[0059] In the case of a computer system, the processor system may include peripheral devices such as a floppy disk drive 454 and a compact disc (CD) ROM drive 456, which also communicate with CPU 444 over the bus 452. Memory 448 is preferably constructed as an integrated circuit, which includes one or more resistance variable memory elements 100. If desired, the memory 448 may be combined with the processor, for example CPU 444, in a single integrated circuit.

[0060] The above description and drawings are only to be considered illustrative of exemplary embodiments which achieve the features and advantages of the invention. Modification and substitutions to specific process conditions and structures can be made without departing from the spirit and scope of the invention. Accordingly, the invention is not to be considered as being limited by the foregoing description and drawings, but is only limited by the scope of the appended claims.

CLAIMS

1. A resistance variable memory element comprising:

at least one metal chalcogenide layer represented by M_xC, wherein M is a metal, C is a chalcogenide chemical element, and x is about 2;

at least one chalcogenide glass layer; and

at least one other glass layer, said metal chalcogenide layer being provided between said at least one chalcogenide glass layer and said at least one other glass layer.

2. The memory element of claim 1 wherein said at least one chalcogenide glass layer comprises a plurality of chalcogenide glass layers.

3. The memory element of claim 1 wherein said at least one other glass layer comprises a plurality of glass layers.

4. The memory element of claim 1 wherein said at least one metal chalcogenide layer comprises a silver-chalcogenide.

5. The memory element of claim 1 wherein said at least one metal chalcogenide layer comprises silver-selenide.

6. The memory element of claim 1 wherein said at least one metal chalcogenide layer comprises silver-sulfide.

7. The memory element of claim 1 wherein said at least one metal

chalcogenide layer comprises silver-oxide.

8. The memory element of claim 1 wherein said at least one metal chalcogenide layer comprises silver-telluride.

9. The memory element of claim 4 wherein said at least one chalcogenide glass layer comprises a material having the formula Ge_xSe_{100-x}, wherein x=20 to 43.

10. The memory element of claim 4 wherein said at least one chalcogenide glass layer stoichiometry is about $Ge_{40}Se_{60}$.

11. The memory element of claim 4 wherein said at least one other glass layer comprises a second chalcogenide glass layer.

12. The memory element of claim 4 wherein said at least one other glass layer comprises an SiSe composition.

13. The memory element of claim 4 wherein said at least one other glass layer comprises an AsSe composition.

14. The memory element of claim 4 wherein said at least one other glass layer comprises a GeS composition.

15. The memory element of claim 4 wherein said at least one other glass layer comprises a combination of germanium, silver, and selenium.

16. The memory element of claim 1 wherein said at least one other glass layer has a thickness between about 100 Å and about 1000 Å.

17. The memory element of claim 1 wherein said at least one other glass layer has a thickness of about 150 Å.

18. The memory element of claim 1 wherein said at least one chalcogenide glass layer has a thickness between about 100 Å and about 1000 Å.

19. The memory element of claim 1 wherein said at least one chalcogenide glass layer has a thickness of about 150 Å.

20. The memory element of claim 1 wherein said at least one metal chalcogenide layer has a first thickness and said at least one chalcogenide glass layer has a second thickness whereby a thickness ratio of said first thickness to said second thickness is between about 5:1 to about 1:1.

21. The memory element of claim 1 wherein said at least one metal chalcogenide layer has a first thickness and said at least one chalcogenide glass layer has a second thickness whereby a thickness ratio of said first thickness to said second thickness is between about 3.3:1 to about 2:1.

22. The memory element of claim 1 wherein said at least one metal chalcogenide layer comprises a plurality of stacked metal chalcogenide layers.

23. The memory element of claim 1 wherein said at least one other glass layer comprises at least one second chalcogenide glass layer.

24. The memory element of claim 23 further comprising a second metal chalcogenide layer in contact with said at least one second chalcogenide glass layer and at least one third chalcogenide glass layer in contact with said at least one second metal chalcogenide layer.

25. The memory element of claim 1 wherein one or more of said at least one chalcogenide glass layers contains a metal dopant.

26. The memory element of claim 25 wherein said metal dopant comprises silver.

27. The memory element of claim 1 wherein said at least one metal chalcogenide layer has a first thickness and said at least one other glass layer has a second thickness whereby a thickness ratio of said first thickness to said second thickness is between about 5:1 to about 1:1.

28. The memory element of claim 1 wherein said at least one metal chalcogenide layer has a first thickness and said at least one other glass layer has a second thickness whereby a thickness ratio of said first thickness to said second thickness is between about 3.3:1 to about 2:1.

29. The resistance variable memory element of claim 1 wherein said at least one metal chalcogenide layer has a thickness equal to or greater than a thickness of each of said at least one chalcogenide glass layer and said at least one other glass layer.

30. A resistance variable memory element comprising:

a body, said body comprising a first glass layer in contact with at least one silver-chalcogenide compound layer, said silver-chalcogenide compound layer being in contact with a second glass layer, wherein at least one of said first and second glass layers is a formed of a chalcogenide glass material; and

a first electrode and a second electrode in respective contact with said first and setond glass layers.

31. The memory element of claim 30 wherein said at least one silver-chalcogenide compound layer comprises silver-selenide.

32. The memory element of claim 30 wherein said at least one silver-chalcogenide compound layer compjrises silver-sulfide.

33. The memory element of claim 30 wherein said at least one silver-chalcogenide compound layer compirises silver-oxide.

34. The memory element of claim 30 wherein said at least one silver-chalcogenide compound layer comprises silver-telluride.

35. The memory element of claim 30 wherein said chalcogenide glass material has the formula Ge_xSe_{100-x}, wherein x=20 to 43.

36. The memory element of claim 30 wherein said chalcogenide glass material stoichiometry is about $Ge_{40}Se_{60}$.

37. The memory element of claim 30 wherein both said first glass layer and said second glass layer comprise a chalcogenide glass material.

38. The memory element of claim 30 wherein at least one of said first and second glass layers contains a metal dopant.

39. The memory element of claim 30 wherein said metal dopant comprises silver.

40. The memory element of claim 30 wherein at least one of said first and second glass layers comprises an SiSe composition.

41. The memory element of claim 30 wherein at least the other of said first and second glass layers comprises an AsSe composition.

42. The memory element of claim 30 wherein at least the other of said first and second glass layers comprises a GeS composition.

43. The memory element of claim 30 wherein at least another of said first

and second glass layers comprises a combination of germanium, silver, and selenium.

44. The memory element of claim 30 wherein said silver-chalcogenide compound layer has a first thickness, said second glass layer has a second thickness, and a thickness ratio of said first thickness to said second thickness is between about 5:1 to about 1:1.

45. The memory element of claim 30 wherein said silver-chalcogenide compound layer has a first thickness, said second glass layer has a second thickness, and a thickness ratio of said first thickness to said second thickness is between about 3.3:1 to about 2:1.

46. The memory element of claim 30 wherein said silver-chalcogenide compound layer has a first thickness and said first glass layer has a second thickness and a thickness ratio of said first thickness to said second thickness is between about 5:1 to about 1:1.

47. The memory element of claim 30 wherein said silver-chalcogenide compound layer has a thickness greater than or equal to the thickness of each of said first and second glass layers.

48. A memory element comprising:

a first electrode;

a first glass layer comprising Ge_xSe_{100-x}, wherein x=20 to 43, said first glass layer being in contact with said first electrode;

a first metal chalcogenide layer in contact with said first glass layer, said first metal chalcogenide layer represented by M_xC , wherein M is a metal, C is a chalcogenide chemical element, and x is about 2; a second glass layer in contact with said first metal chalcogenide layer; and a second electrode in contact with said second glass layer.

49. The memory element of claim 48 wherein x is about 40.

50. The memory element of claim 48 wherein said first metal chalcogenide layer comprises a silver-chalcogenide.

51. The memory element of claim 48 wherein said first metal chalcogenide layer comprises silver-selenide.

52. The memory element of claim 48 wherein said first metal chalcogenide layer comprises silver-sulfide.

53. The memory element of claim 48 wherein said first metal chalcogenide layer comprises silver-oxide.

54. The memory element of claim 48 wherein said first metal chalcogenide layer comprises silver-telluride.

55. The memory element of claim 51 wherein said second glass layer acts as a diffusion control layer to control diffusion of components from said

second electrode through said metal chalcogenide layer and said first glass layer.

56. The memory element of claim 55 wherein said second glass layer comprises an SiSe composition.

57. The memory element of claim 55 wherein said second glass layer comprises an AsSe composition.

58. The memory element of claim 55 wherein said second glass layer comprises a GeS composition.

59. The memory element of claim 55 wherein said second glass layer comprises a combination of germanium, silver, and selenium.

60. The memory element of claim 48 wherein said first metal chalcogenide layer comprises a plurality of metal chalcogenide layers in serial contact with each other;.

61. The memory element of claim 48 wherein at least one of said first glass layer and said second glass layer comprises a plurality of glass layers in serial contact with each other.

62. The memory element of claim 48 wherein at least one of said first and second glass layers contains a metal dopant.

63. The memory element of claim 62 wherein said metal dopant comprises silver.

64. A chalcogenide glass stack comprising:

a chalcogenide glass layer, said chalcogenide glass layer being configured for variable resistance memory behavior;

at least one metal chalcogenide layer represented by M_xC, wherein M is a metal, C is a chalcogenide chemical element, and x is about 2, said metal chalcogenide layer being in contact with said chalcogenide glass layer; and

a diffusion control layer in contact with said metal chalcogenide layer for controlling diffusion of elements into said chalcogenide glass layer.

65. The chalcogenide glass stack of claim 64 wherein said diffusion control layer is a second glass layer.

66. The chalcogenide glass staick of claim 64 further comprising a metal containing electrode in contact with said diffusion control layer and wherein said diffusion control layer slows migration of a metal from said electrode into said chalcogenide glass layer.

67. The chalcogenide glass stack of claim 64 wherein said at least one metal chalcogenide layer comprises a silver-chalcogenide.

68. The chalcogenide glass stack of claim 64 wherein said at least one metal chalcogenide layer comprises silver-selenide.

69. The chalcogenide glass stack of claim 64 wherein said at least one metal chalcogenide layer comprises silver-sulfide.

70. The chalcogenide glass stack of claim 64 wherein said at least one metal chalcogenide layer comprises silver-oxide.

71. The chalcogenide glass stack of claim 64 wherein said at least one metal chalcogenide layer comprises silver-telluride.

72. The chalcogenide glass stack of claim 64 wherein at least one or both of said chalcogenide glass layer and said diffusion control layer contains a metal dopant.

73. The chalcogenide glass stack of claim 72 wherein said metal dopant comprises silver.

74. A memory element comprising: a first electrode;

at least one first chalcogenide glass layer in contact with said first electrode;

at least one first metal containing layer in contact with said at least one first chalcogenide glass layer;

at least one second chalcogenide glass layer in contact with said at least one first metal containing layer;

at least one second metal containing layer in contact with said at least one second chalcogenide glass layer;

at least one third chalcogenide glass layer in contact with said at least one second metal containing layer; and

a second electrode in contact with said at least one third chalcogenide glass layer.

75. The memory element of claim 74 wherein said metal containing layers comprise one or more silver-selenide layers.

76. The memory element of claim 74 wherein one or more of said chalcogenide glass layers comprise a plurality of chalcogenide glass layers.

77. The memory element of claim 74 wherein one or more of said metal containing layers comprises a plurality of metal containing layers.

78. The memory element of claim 74 wherein one or more of said chalcogenide glass layers contains a metal dopant.

79. The memory element of claim 78 wherein said metal dopant comprises silver.

80. A method of forming a resistance variable memory element comprising the steps of:

forming a first electrode; forming a first chalcogenide glass layer in contact with said first electrode;

forming a first metal containing layer in contact with said first chalcogenide

glass layer; and

forming a second chalcogenide glass layer in contact with said first metal containing layer;

forming a second metal containing layer in contact with said first chalcogenide glass layer;

forming a third chalcogenide glass layer in contact with said second metal containing layer; and

forming a second electrode in contact with said third chalcogenide glass layer.

81. The method of claim 80 wherein said chalcogenide glass layers comprise a material having the formula Ge_xS_{100-x}, wherein x is between about 20 to about 43.

82. The method of claim 81 wherein said chalcogenide glass layers have a stoichiometry of about $Ge_{40}Se_{60}$.

83. The method of claim 80 wherein said chalcogenide glass layers comprise a plurality of chalcogenide glass layers.

84. The method of claim 80 wherein said metal containing layers comprise a plurality of metal containing layers.

85. The method of claim 80 wherein one or more of said chalcogenide glass layers contain a metal dopant.

86. The method of claim 80 wherein one or more of said metal containing layers comprises silver-selenide.

87. The method of claim 86 wherein said metal dopant comprises silver.

88. The method of claim 80 wherein said metal containing layers have a thickness which is equal to or greater than the thickness of each of said chalcogenide glass layers.

89. The method of claim 80 wherein each of said metal containing layers has a first thickness and each of said chalcogonide glass layers has a second thickness whereby a thickness ratio of said first thickness to said second thickness is between about 5:1 to about 1:1.

91. The method of claim 89 further wherein said thickness ratio of said first thickness to said second thickness is between about 3.3:1 to about 2:1.

92. A method of forming a resistance variable memory element comprising:

forming a first glass layer;

forming a silver-selenide layer in contact with said first glass layer; and

forming a second glass layer in contact with said silver-selenide layer, whereby one of said first and second glass layers is formed of a chalcogenide glass material.

92. The method of claim 91 wherein said chalcogenide glass material has a stoichiometric composition of about $Ge_{40}Se_{60}$.

93. The method of claim 91 wherein at least one of said glass layers contains a metal dopant.

94. The method of claim 93 wherein said metal dopant comprises silver.

95. The method of claim 91 wherein both of said first and second glass layers comprises a chalcogenide glass material.

96. The method of claim 95 further comprising the step of forming alternating layers of said chalcogenide glass material and said silver-selenide layer.

97. The method of claim 91 wherein said layer formed of said chalcogenide glass material further contains a metal dopant.

98. The method of claim 97 wherein said metal dopant comprises silver.

99. The method of claim 91 wherein another of said first and second glass layers controls diffusion of a metal ion from an electrode through said memory element.

100. The method of claim 99 wherein said other glass layer comprises an SiSe composition.

101. The method of claim 99 wherein said other glass layer comprises an AsSe composition.

102. The method of claim 99 wherein said other glass layer comprises a GeS composition.

103. The method of claim 99 wherein said other glass layer comprises a combination of germanium, silver, and selenium.

104. The method of claim 91 wherein said silver-selenide layer has a thickness which is equal to or greater than a thickness of each of said first and second glass layers.

105. The method of claim 91 wherein said metal containing layer comprises a plurality of silver-selenide layers in serial contact with each other.

106. A processor-based system, comprising:

a processor; and

a memory circuit connected to said processor, said memory circuit including a resistance variable memory element comprising at least one metal chalcogenide compound layer, at least one chalcogenide glass layer, at least one other glass layer, said metal chalcogenide compound layer being provided between said at least one

chalcogenide glass layer and said at least one other glass layer.

107. The system of claim 106 wherein said chalcogenide glass layer comprises a material having the formula Ge_xSe_{100-x}, wherein x=20 to 43.

108. The system of claim 106 wherein said chalcogenide glass layer stoichiometry is about $Ge_{40}Se_{60}$.

109. The system of claim 106 wherein at least one of said glass layers contains a metal dopant.

110. The system of claim 109 wherein said metal dopant comprises silver.

111. The system of claim 106 wherein said other glass layer comprises a second chalcogenide glass layer.

112. The system of claim 111 further comprising a second metal chalcogenide layer in contact with said at least one
second chalcogenide glass layer and at least one third chalcogenide glass layer in contact with said at least one second metal chalcogenide layer.

113. The system of claim 111 wherein said chalcogenide glass layer comprises a plurality of stacked chalcogenide glass layers.

114. The system of claim 111 wherein said metal chalcogenide layer

comprises a plurality of stacked metal chalcogenide layers.

115. The system of claim 112 wherein at least one of said chalcogenide glass layers comprises a metal dopant.

116. The system of claim 106 wherein said metal chalcogenide compound layer comprised silver-selenide layer.

117. The system of claim 116 wherein said other glass layer comprises an SiSe composition.

118. The system of claim 116 wherein said other glass layer comprises an AsSe composition.

119. The system of claim 106 wherein said other glass layer comprises a GeS composition.

120. The system of claim 106 wherein said other glass layer comprises a combination of germanium, silver, and selenium.

121. The system of claim 106 wherein said other glass layer is a diffusion control layer for slowing migration of a metal ion from an electrode connected thereto.

122. A processor-based system, comprising:

a processor;

a memory circuit connected to said processor, said memory circuit including a first electrode;

at least one first chalcogenide glass layer in contact with said first electrode;

at least one first metal containing layer in contact with said at least one first chalcogenide glass layer;

at least one second chalcogenide glass layer in contact with said at least one first metal containing layer;

at least one second metal containing layer in contact with said at least one second chalcogenide glass layer;

at least one third chalcogenide glass layer in contact with said at least one second metal containing layer; and

a second electrode in contact with said at least one third chalcogenide glass layer.

123. The system of claim 122 wherein said metal containing layers comprise one or more silver-selenide layers.

124. The system of claim 122 wherein one or more of said chalcogenide glass layers comprise a plurality of chalcogenide glass layers.

125. The system of claim 122 wherein one or more of said metal containing layers comprises a plurality of metal containing layers.

126. The system of claim 122 wherein one or more of said chalcogenide

glass layers contains a metal dopant.

127. The system of claim 126 wherein said metal dopant comprises silver.

128. A memory element comprising:

a first electrode;

a second electrode; and

a plurality of chalcogenide glass layers and a plurality of metal containing layers between said first and second electrodes, whereby said plurality of chalcogenide glass layers alternate with said metal containing layers, with one of said chalcogenide glass layers in contact with said first electrode and another of said chalcogenide glass layers in contact with said second electrode.

129. The memory element of claim 128 wherein said plurality of metal containing layers comprises one or more silver-selenide layers.

130. The memory element of claim 128 wherein one or more of said plurality of chalcogenide glass layers comprises a plurality of chalcogenide glass layers.

131. The memory element of claim 128 wherein one or more of said plurality of metal containing layers comprises a plurality of metal containing layers.

132. The memory element of claim 128 wherein one or more of said plurality of chalcogenide glass layers contains a metal dopant.

133. The memory element of claim 132 wherein said metal dopant comprises silver.

134. A method of forming a resistance variable memory element comprising: forming a first electrode; forming a second electrode; and forming a plurality of chalcogenide glass layers and a plurality of metal containing layers between said first and second electrodes, whereby said plurality of chalcogenide glass layers alternate with said metal containing layers, with one of said chalcogenide glass layers in contact with said first electrode and another of said chalcogenide glass layers in contact with said second electrode.

135. The method of claim 134 wherein said plurality of metal containing layers comprises one or more silver-selenide layers.

136. The method of claim 134 wherein one or more of said plurality of chalcogenide glass layers comprises a plurality of chalcogenide glass layers.

137. The method of claim 134 wherein one or more of said plurality of metal containing layers comprises a plurality of metal containing layers.

138. The method of claim 134 wherein one or more of said plurality of chalcogenide glass layers contains a metal dopant.

139. The method of claim 138 wherein said metal dopant comprises silver.