

PATENT SPECIFICATION

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DRAWINGS ATTACHED

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(54) COMPLEMENTARY INSULATED GATE FIELD EFFECT TRANSISTOR INTEGRATED CIRCUITS

(71) We, RCA CORPORATION a corporation organised under the laws of the State of Delaware, United States of America, of 30 Rockefeller Plaza, City and State of New York, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to integrated circuits of the type which include complementary insulated gate field effect transistors as their active devices. Commonly, these devices are called CMOS integrated circuits. More particularly, the invention relates to CMOS integrated circuits operable at relatively low power supply voltages.

CMOS integrated circuits as they are presently commonly constructed include a body of semiconductive material, usually N type silicon, which provides the substrate for the MOS transistors which have P type channels. Diffused into this body are one or more regions of P type conductivity, called well regions, which act as the substrates for the transistors which have N type channels. Sources and drains of the appropriate types of conductivity are diffused into the well regions of the body and into the body itself outside of the well regions. Gate insulators, contact metallization, and gate metallization are provided to complete the individual transistors. Circuit interconnections are provided to connect the transistors into circuits such as inverter circuits, transmission gates, shift registers, and the like.

The MOS transistors in CMOS integrated circuits are usually of the enhancement type, that is, in each transistor no appreciable current flows in its channel when no voltage difference exists between its gate and its source. For conduction to take place, the potential applied between the gate and the source elec-

trodes of a device must be greater in amplitude than a minimum value called the threshold voltage V_{TP} for P channel devices and V_{TN} for N channel devices.

Above threshold, the conductivity of the devices increases with increasing gate voltage.

In some prior CMOS integrated circuits capable of operation at relatively low supply voltages, the threshold voltages V_{TP} of the P channel devices are distributed statistically from wafer to wafer between about 1.5 and about 3.0 volts, with the peak of the distribution at about 2.2 volts. N channel devices in these integrated circuits have threshold voltages V_{TN} distributed between about 0.8 and about 3.0 volts, with the peak of the distribution at about 1.5 volts. The supply voltage required to operate these circuits must necessarily be greater than the largest threshold voltage, and the extent to which it is larger is highly dependent on the circuit design, that is, it is dictated by the degree of conductivity above mere onset of conduction which is required for a particular circuit function. Heretofore, the lowest supply voltage which would allow reliable operation of a circuit having a maximum threshold voltage of about 1.4 volts (measured at the level where conduction first begins) has been around 3.0 volts. Supply voltages of about 3 to about 15 volts are usually recommended.

There are many applications for CMOS integrated circuits which are capable of operation with supply voltages less than those described above. For example, many devices are presently being designed for operation with small batteries as the power supplies. For these applications, the circuits must be capable of operation at the 1.0 to 3.0 volt level which is available from such batteries.

The speed of operation of CMOS integrated circuits is also a function of the threshold voltages of the devices in the circuit. Many applications can be found for CMOS

integrated circuits which are capable of operation at higher speeds than have been achieved heretofore.

5 Teachings are present in the prior art to the effect that the threshold voltage of an MOS device is dependent on the difference between the work functions of the material of the gate electrode and the material of the semiconductor. See Deal et al. "BARRIER ENERGIES IN METAL-SILICON DIOXIDE-SILICON STRUCTURES" 27 Journal of the Physics and Chemistry of Solids, 1873 et seq. (1966). Moreover, it is known that the threshold voltage is a function of the conductivity type of the semiconductor. See Leuenberger et al. "COMPLEMENTARY-MOS LOW-POWER LOW-VOLTAGE INTEGRATED BINARY COUNTER" 57 Proceedings of the IEEE, 1528 et seq. (1969).

20 The same material has been used heretofore for the gate electrodes of both types of devices in CMOS integrated circuits primarily because those of ordinary skill believed that they should use a single metallization material in order to preserve yields and maintain process economy. The Leuenberger article suggests choosing a material (molybdenum-gold alloy) which provides an optimum threshold voltage for both type of devices, although it is not the best material for either device individually.

30 In commercially available devices, aluminum has usually been used as the material of all the gate electrodes primarily because it is the common metallization material for integrated circuits. Aluminum, however, provides relatively high threshold voltage in P channel devices, as compared to the threshold voltage it provides in N channel devices. Polycrystalline silicon has been used as the gate material in the so-called self-aligned gate structure. In those structures, an N channel transistor has a silicon gate doped with phosphorus and a P channel transistor has a silicon gate doped with boron. Although the dopants are different, these gate electrodes are still predominantly of the same material.

45 According to the invention we provide an integrated circuit device of the type which includes both a P channel insulated gate field effect transistor and an N channel insulated gate field effect transistor, each insulated gate field effect transistor having a gate electrode characterized by the material of the gate electrode of the P channel insulated gate field effect transistor being predominantly one element or alloy and the material of the gate electrode of the N channel insulated gate field effect transistor being predominantly an element or alloy different from that of the P channel insulated gate field effect transistors. In an embodiment of the invention a complementary insulated gate field effect transistor integrated circuit (a CMOS integrated circuit) includes both P channel and N channel

enhancement type insulated gate field effect transistors characterized by extremely low threshold voltages, enabling the circuit to be operated with extremely low power supplies. The P channel transistors have gate electrodes made of boron doped polycrystalline silicon, while the N channel transistors have gate electrodes made of aluminum.

In the accompanying drawing:

FIGURE 1 is a schematic circuit diagram of a CMOS inverter circuit.

FIGURE 2 is a diagram of the combined transfer characteristics of the transistors shown in FIGURE 1.

FIGURES 3 to 5 are partial cross sections of a CMOS wafer at different stages of manufacture of a typical device.

EXAMPLE

FIGURE 1 has been provided in order to explain some of the circuit relationships pertaining to the present invention. The circuit 10 of FIGURE 1 is a complementary inverter circuit which is a basic building block in CMOS circuit.

The circuit 10 includes a P channel MOS transistor 12 and an N channel MOS transistor 14 connected in series between a terminal 16, supplied with a voltage of +V volts, and ground 18. The drains 19 and 20 of transistors 12 and 14 respectively, are connected together and to an output terminal 12. The gates 22 and 24 respectively of the transistors 12 and 14 are connected together and to an input terminal 26.

The transistors 12 and 14 are each of the enhancement type. A voltage difference greater than a value called the threshold value, V_{TP} for P channel devices and V_{TN} for N channel devices, must be applied between the gates and the sources, 27 and 28 respectively, of these devices before appreciable current will flow. The inverter circuit 10 operates in well known manner to provide an output which is inverted with respect to the input.

The diagram of FIGURE 2 illustrates the transfer characteristics of each of the transistors 12 and 14 in a combined graph. FIGURE 2 plots drain current, I_D , against gate-to-source voltage different, $V_{IN}-V_S$. When the gate-to-source voltage, $V_{IN}-V_S$, for the P channel transistor 12 is less than negative than the threshold voltage V_{TP} , the transistor 12 does not conduct appreciable current. Voltages more negative than V_{TP} are required to produce appreciable conduction. For the N channel transistor 14, gate-to-source voltages less than the threshold voltage V_{TN} result in no appreciable current and positive voltages greater than V_{TN} are required.

A typical value of V_{TP} in the prior art is, as indicated above, about 2.2 volts; and a typical value of V_{TN} is about 1.5 volts. The magnitude of +V in FIGURE 1 must be greater than the absolute value of the larger

of the threshold voltages V_{TP} and V_{TN} in order for the circuit 10 to be operative. Moreover, the magnitude of $+V$ must be sufficiently greater than V_{TP} or V_{TN} so that enough conductivity will occur in the transistors 12 and 14 for the circuit 10 to operate efficiently. For prior devices, a minimum power supply voltage of approximately 3.0 volts is usually specified.

The present novel CMOS integrated circuit structure has characteristics which make it operable at power supplies much less than has been required heretofore. The structure of a substantially completed device 30 is illustrated in FIGURE 5. The device 30 in this example includes a body 32 of semiconductive material such as silicon which has a surface 34 adjacent to which the active devices of the circuit are formed. A relatively thick oxide coating 36 covers a part of the surface 34 of the body 32 and has openings 38 adjacent to the transistors 12 and 14. A relatively thin gate insulator 40 is adjacent to the surface 34 in the openings 38 in the thick oxide coating 36. As will appear hereinafter, the coatings 40 are grown by thermal oxidation and consume a portion of the substrate material adjacent to the opening 38, resulting in an indented configuration of the surface 34, as shown. The coatings 36 and 40 are continuously cross hatched since they are of the same material, i.e., silicon dioxide in this example.

The transistor 14 has a substrate region 42 which in this example is a diffused P type region. Within the region 42 are spaced source and drain regions 44 and 46 respectively, which define the ends of a channel region 48 adjacent the surface 34. The P channel transistor 12 utilizes the material of the substrate 32 as its substrate region and has spaced source and drain regions of P+ type conductivity, 50 and 52, defining the ends of a channel region 54 adjacent to the surface 34.

A metal contact and interconnection layer 56 is connected to the source region 44 of the transistor 14. A metal layer 58 interconnects the drain regions 46 and 52 of the two transistors 12 and 14. A metal layer 60 is connected to the source region 50 of the transistor 12. On the gate insulator 40 of the transistor 14 is a gate electrode 62 which, in this example, is made of aluminum. On the gate insulator 40 of the transistor 12 is a gate electrode 64 which, in this example, is made of P+ type polycrystalline silicon. Contact is made to the gate electrode 64 at a location not illustrated in FIGURE 5 to interconnect this electrode with other elements of the circuit.

In a prior art device, the gate electrode 64 of the P channel transistor 12 is made of aluminum. Consequently, the absolute value of the threshold voltage in the transistor 12 is

usually much higher than that of the transistor 14. Typically, the threshold voltage measured at a drain current of $10 \mu A$, for transistors having gate widths (the dimension normal to the plane of the drawings) of 76 microns is about 0.7 volts for N channel transistors and about 1.6 volts for the P channel transistors. The N channel threshold voltage is satisfactorily low. By substituting, in this example, polycrystalline silicon as the gate material in the P channel transistor 12, a threshold voltage for this device of less than or equal to 0.7 volts (at $10 \mu A$ drain current, 76 microns gate width), can be achieved.

The materials mentioned here are those which are preferred in practice, but other materials such as elements like gold, chromium, or titanium or alloys such as molybdenum-gold or chrome-gold, may be selected as the predominant material. The selected materials should be those which provide appropriately low threshold voltages for the kinds of devices to which they are applied, and the preferred materials disclosed here are the best materials known to us for this purpose. The characteristic novelty of the present device is, therefore, that the material of the gate electrodes of the P channel insulated gate field effect transistors is predominantly one element or alloy, and the material of the gate electrodes of the N channel insulated gate field effect transistors is predominantly an element or alloy different from that of the P channel insulated gate field effect transistors.

A preferred method for making the present CMOS integrated circuit device will now be described with reference to FIGURES 3 to 5. The starting material for the present process is a substrate body 32 which may be of N type silicon of (100) orientation, that is, the surface 34 of the substrate body 32 is oriented substantially parallel to the (100) crystallographic planes in the substrate body 32. The resistivity of the substrate 32 is chosen to be about 5 ohms-cm. to about 10 ohms-cm.

The processing steps up to and including the formation of the gate insulators 40 are entirely conventional and are not illustrated in detail. In general, these steps are as follows. First, a source of P type conductivity modifiers is deposited on the surface 34 adjacent to the intended location of the P well region 42. This step is carried out by exposing the body 32 to boron for about 30 minutes at a temperature of from about $800^{\circ}C$ to about $820^{\circ}C$ to form a shallow diffused P type region in the substrate body 32 adjacent to the surface 34. The substrate body 32 is then heated to a temperature of about $1200^{\circ}C$ for a period of a few minutes, i.e., about 15 minutes, in a dry oxidizing ambient. This heat treatment results in a redistribution of the conductivity modifiers from the initial shallow region to form a more deeply diffused P type region. The duration of this heat treatment

step is a variable that effects the final surface concentration of conductivity modifiers in the well region 42. This redistribution step is incomplete, that is, it is carried out for a time less than that which would drive the well region 42 to its final desired depth. The substrate body 32 is then heated in water vapor or steam at a temperature of about 1100°C for about 4 hours. This step results in outdiffusion of conductivity modifiers from the P type region to reduce the surface concentration thereof. The amount of reduction is a variable which is determined by routine experimentation to produce a desired, relatively low surface concentration of less than about 3×10^{18} atoms/cm³. This outdiffusion step is required because it is difficult to achieve a value this low by known direct diffusion techniques.

A second redistribution to complete the well region 42 is then performed. The substrate body 32 is heated to a temperature of about 1200°C, in oxygen, for a period of about 16 hours to accomplish this step. The P+ type regions 50 and 52 of the P channel transistor 12 are next diffused by masking the body 32 and heating it to a temperature of about 1000° C while exposed to a source of boron, for a period of about 30 minutes. The N+ type regions 44 and 46 are then formed by conventionally masking the substrate body 32 and exposing it to a phosphorus oxychloride source at a temperature of about 1050°C.

After the removal of all of the oxides from the surface of the body 32, the relatively thick oxide coating 36 is formed. The coating 36 may be a deposited coating formed by the thermal decomposition of silane (SiH₄) in the presence of oxygen in known manner for a time sufficient to grow a coating of approximately 10,000 Å in thickness. The openings 38 are then formed in the coating 36 by known photolithographic techniques.

The gate insulator layers 40 are next grown. The material of the body 32 adjacent to the portions of the surface 34 which are exposed by the openings 38 is oxidized by heating the body 32 to a temperature of approximately 875°C for a period of about 48 minutes in an atmosphere of an azeotropic mixture of steam and gaseous hydrochloric acid. This results in the formation of oxide coatings of a thickness of about 800 Å. The oxide coatings 40 are then annealed by heat treatment in an inert atmosphere such as forming gas for a period of about 15 minutes at a temperature of about 1100°C.

At this stage, the process diverges from the process used to make the conventional aluminum gate CMOS devices. The next step is to deposit a layer 66 of substantially intrinsic polycrystalline silicon (FIGURE 3) over the entire surface of the body 32. This may be accomplished by the thermal decomposition

of silane diluted with hydrogen, in known manner. The thickness of the layer 66 should be approximately 8000 Å. Next, a layer 68 of silicon dioxide is deposited, e.g., by the thermal decomposition of silane in the presence of oxygen, to form a masking coating over the polycrystalline layer 66. An opening 70 is defined in the coating 68 at the location desired for the gate electrode 64. Boron is then diffused, by conventional processes, into the polycrystalline silicon layer 66 at this location to increase the conductivity of the material. The boron glass resulting from this diffusion step, and the coating 68, are next removed. The entire silicon coating 66 is then exposed to a solvent for silicon, such as an aqueous hydrazine solution, potassium hydroxide-propanol solution, or the like. It has been found unexpectedly that no etch resistant mask is required over the P+ type areas of the coating 66, that is, that the P+ doped material is substantially insoluble in these solvents. The material etches only in its non-diffused portions, resulting in clean well defined edges of the gate electrode 64.

The next step is to open contact holes 72 in the gate insulating coatings 40 wherever contact to the source and drain regions is desired. This is done conventionally. The configuration of the device after the completion of this step is shown in FIGURE 4. Note here that the P+ type gate electrode 64 has been completed. It is not self-aligned with the channel region of the transistor 12 inasmuch as the source and drain regions 50 and 52 were formed previously in an independent step. Nevertheless, lower voltage operation is achieved and yields are improved over conventional aluminum gate and conventional silicon gate devices.

The remainder of the processing is conventional. A coating of aluminum is deposited over the entire wafer and portions of the coating are removed photolithographically to form the interconnection pattern elements 56 and 58 and 60 shown in FIGURE 5, as well as the gates 62 of the N channel transistors. Additional protective coatings may then be applied, and the device further completed in known manner.

Having regard to the provisions of section 9 of the Patents Act, attention is directed to the claims of Application Number 28159/72 (Serial No. 1,332,277).

WHAT WE CLAIM IS:—

1. An improved integrated circuit device of the type which includes both a P channel insulated gate field effect transistor and an N channel insulated gate field effect transistor, each insulated gate field effect transistor having a gate electrode characterized by the material of the gate electrode of the P channel insulated gate field effect transistor being predominantly one element or alloy and the

material of the gate electrode of the N channel insulated gate field effect transistor being predominantly an element or alloy different from that of the P channel insulated gate field effect transistor.

2. A device as in claim 1, wherein said P channel gate electrode material is predominantly polycrystalline silicon, and said N channel gate electrode material is predominantly aluminum.

3. A device as in claim 2, wherein said polycrystalline silicon contains boron.

4. An integrated circuit device substantially as described with reference to the accompanying drawings.

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