

FIGURE 2A

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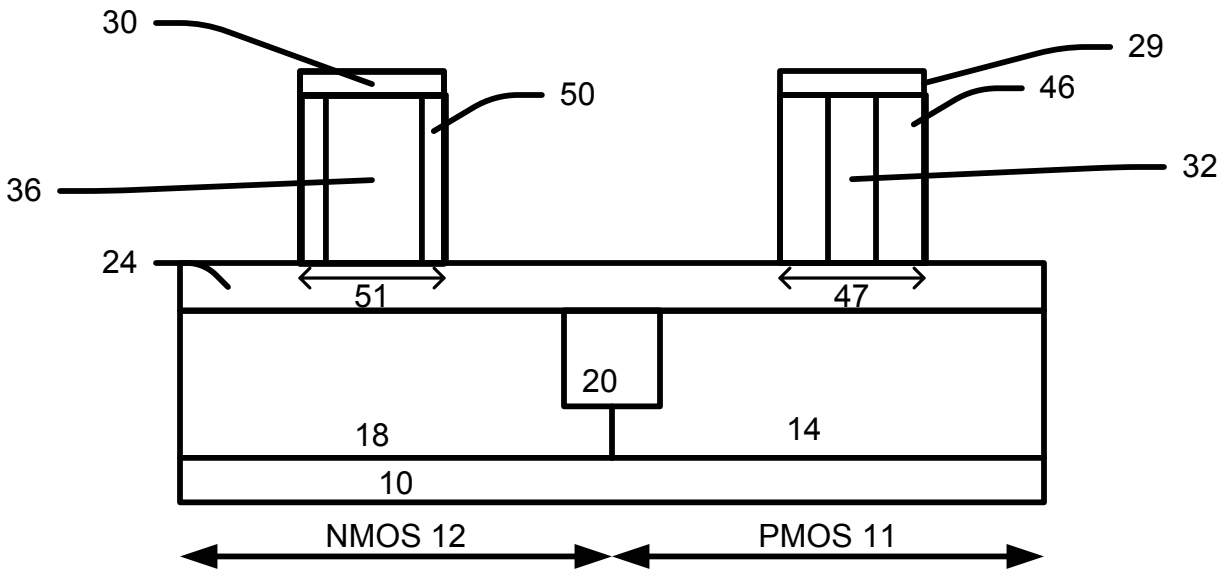


FIGURE 3

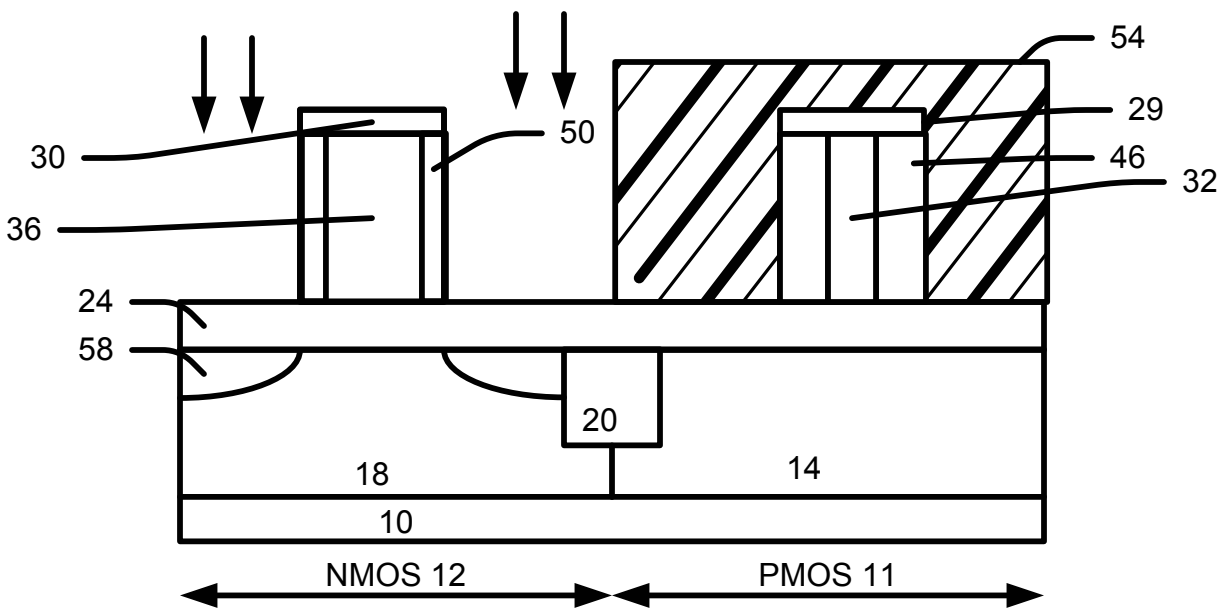


FIGURE 4

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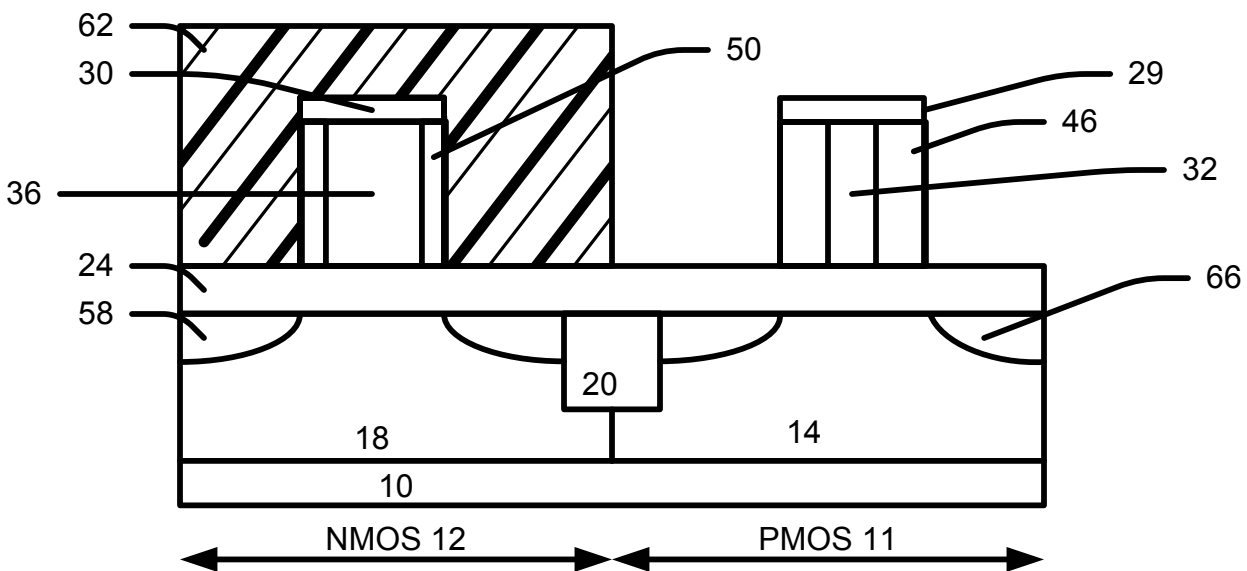


FIGURE 5

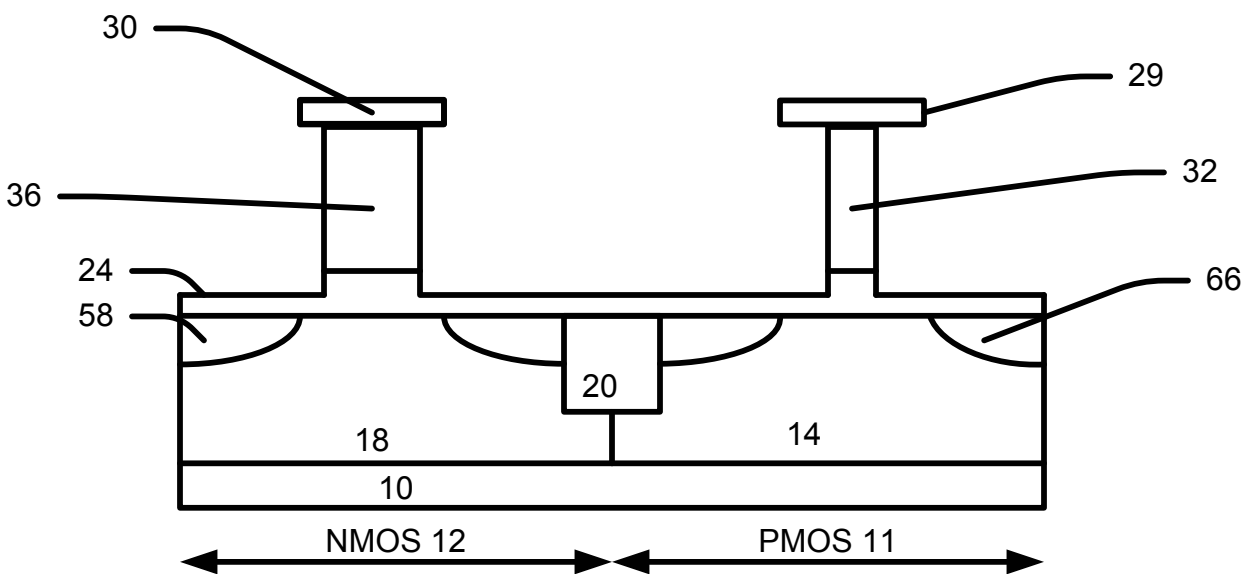


FIGURE 6

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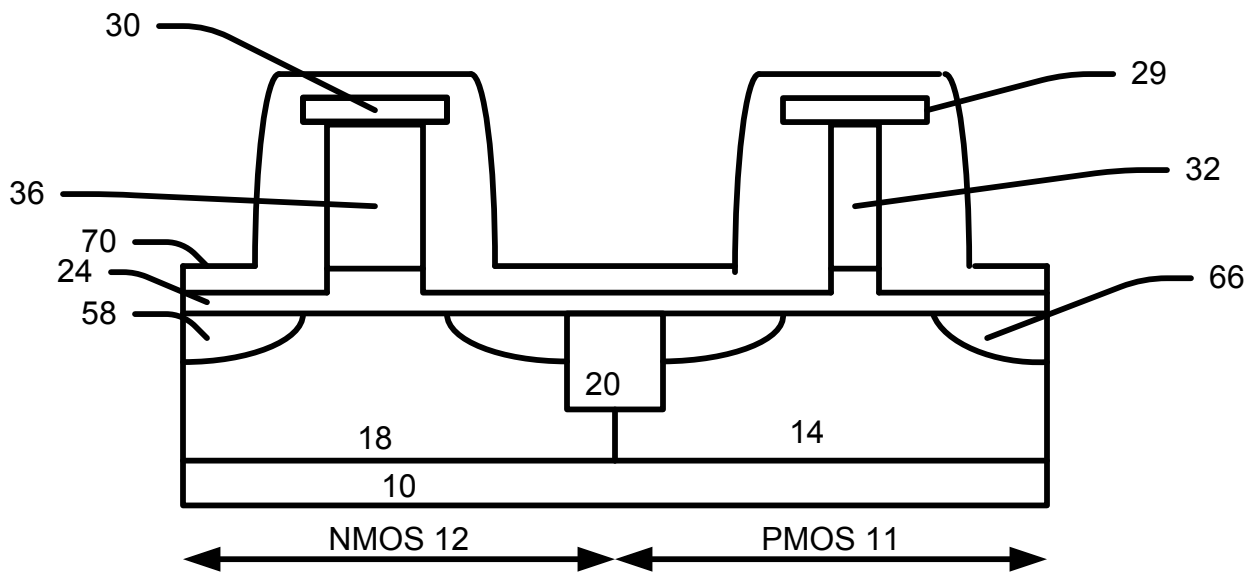


FIGURE 7

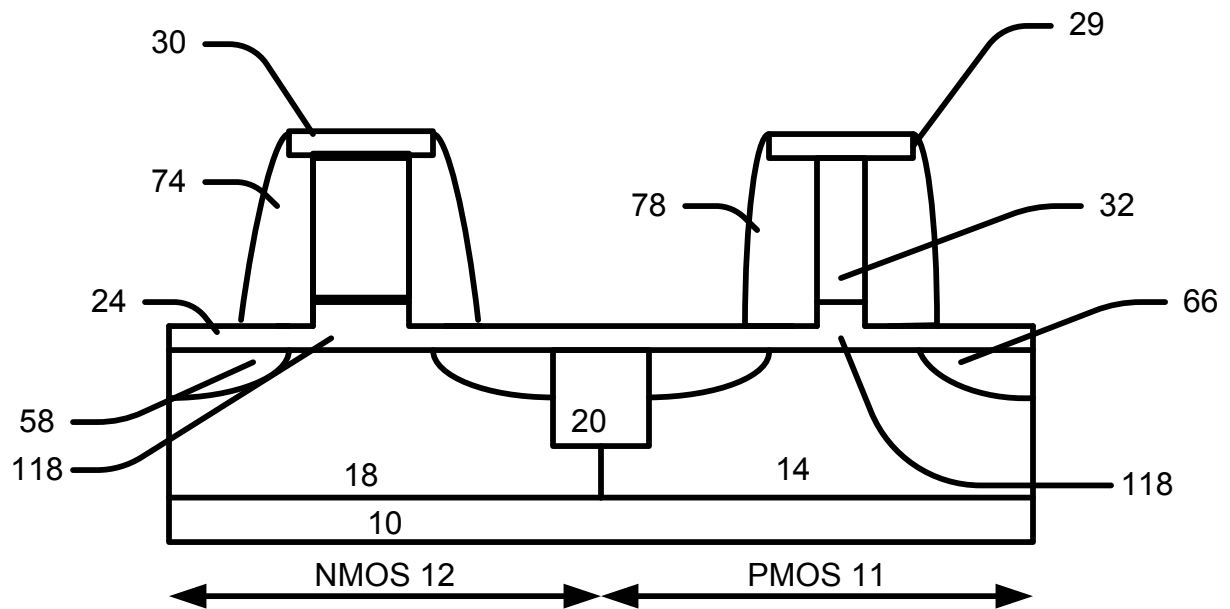


FIGURE 8

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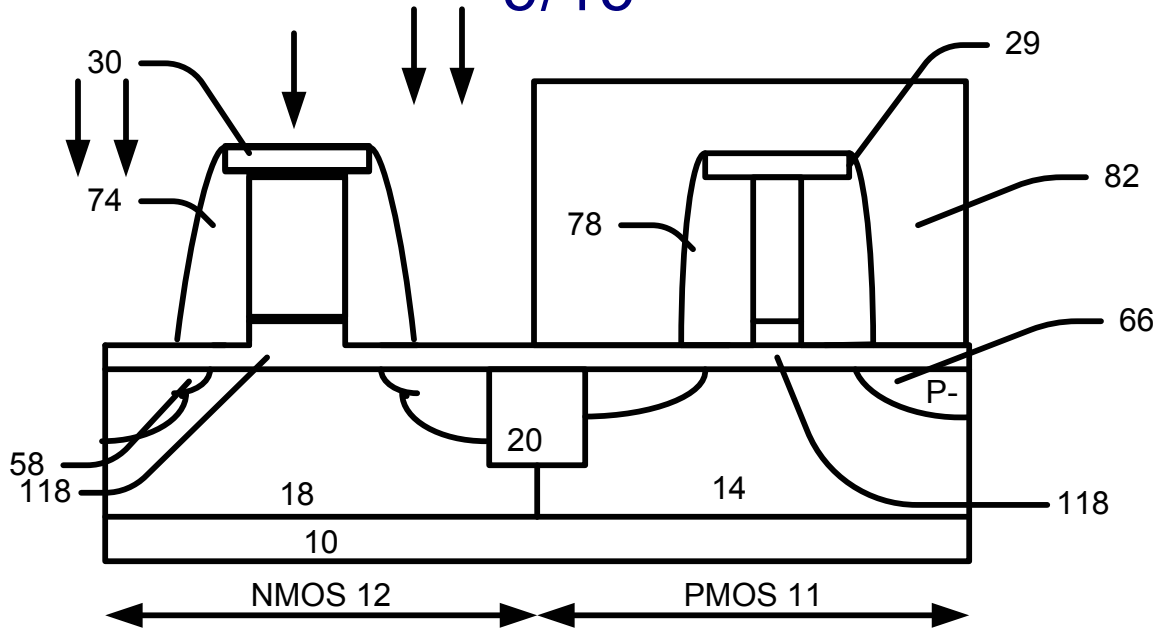


FIGURE 9

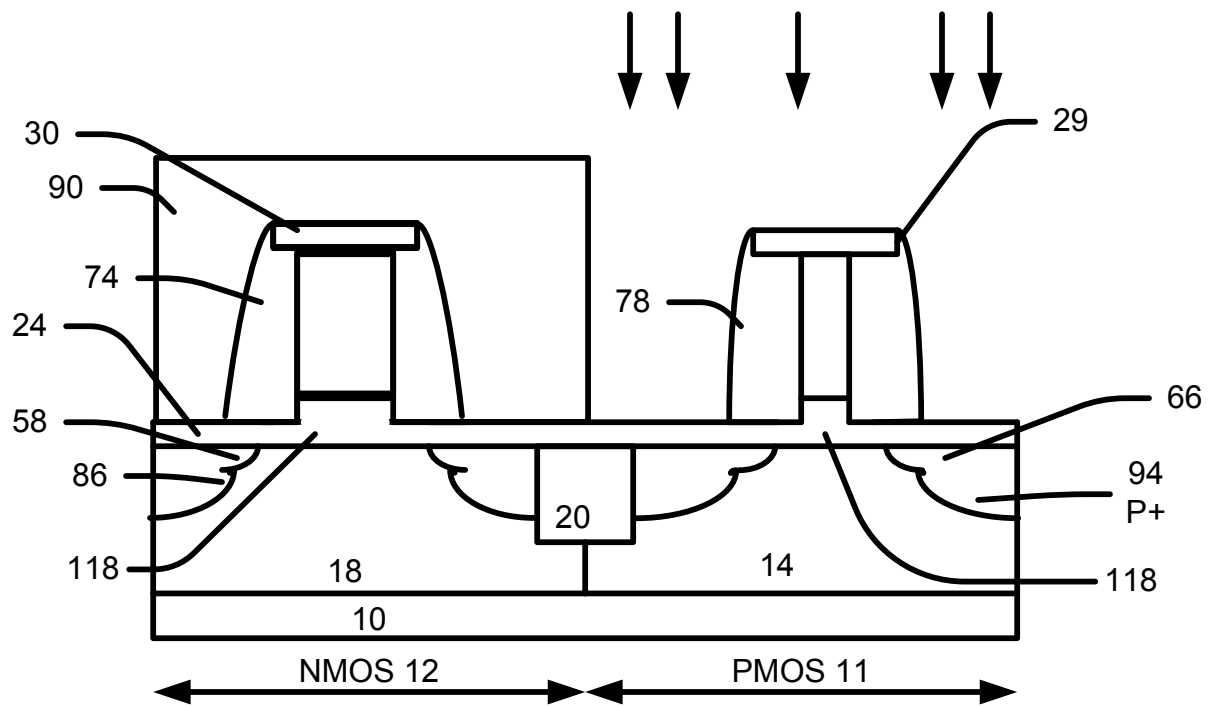


FIGURE 10

30

74

24

98

86

18

10

20

14

29

78

98

94

66

NMOS 12

PMOS 11

FIGURE 12

Diagram illustrating a cross-sectional view of a semiconductor device, showing two transistors (NMOS 12 and PMOS 11) and their associated components. The device is built on a substrate 10. The NMOS 12 and PMOS 11 are formed in the substrate. The gate stack 14 is formed on the substrate. The gate oxide 18 is formed on the substrate. The gate electrode 20 is formed on the gate oxide. The gate oxide 29 is formed on the gate electrode. The gate oxide 30 is formed on the gate oxide. The gate oxide 66 is formed on the gate oxide. The gate oxide 74 is formed on the gate oxide. The gate oxide 78 is formed on the gate oxide. The gate oxide 86 is formed on the gate oxide. The gate oxide 94 is formed on the gate oxide. The gate oxide 98 is formed on the gate oxide. The gate oxide 106 is formed on the gate oxide.

[illegible]

FIGURE 14

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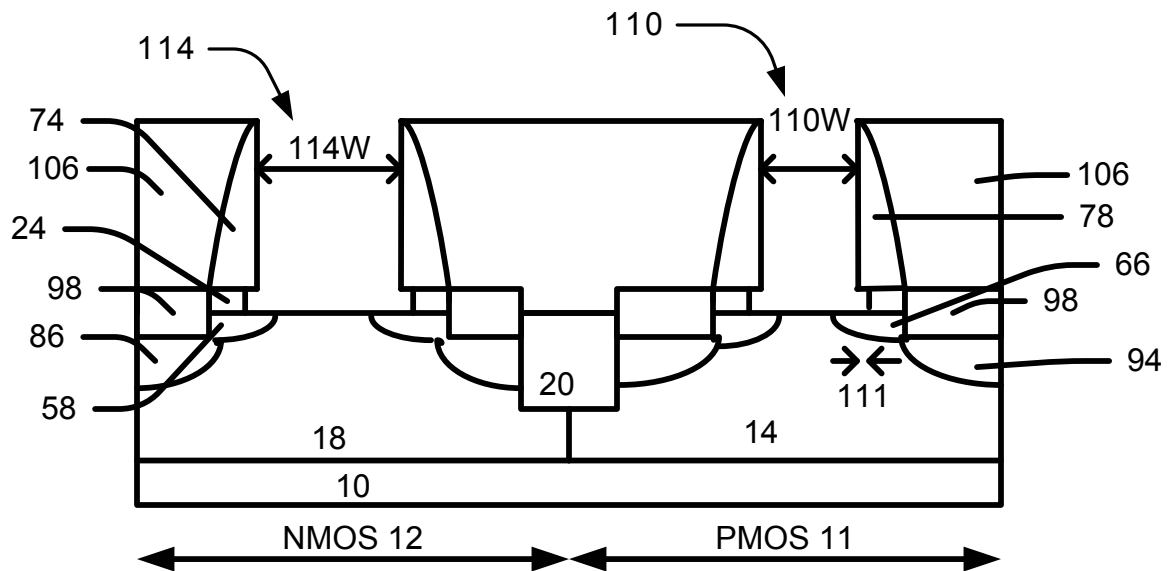


FIGURE 15

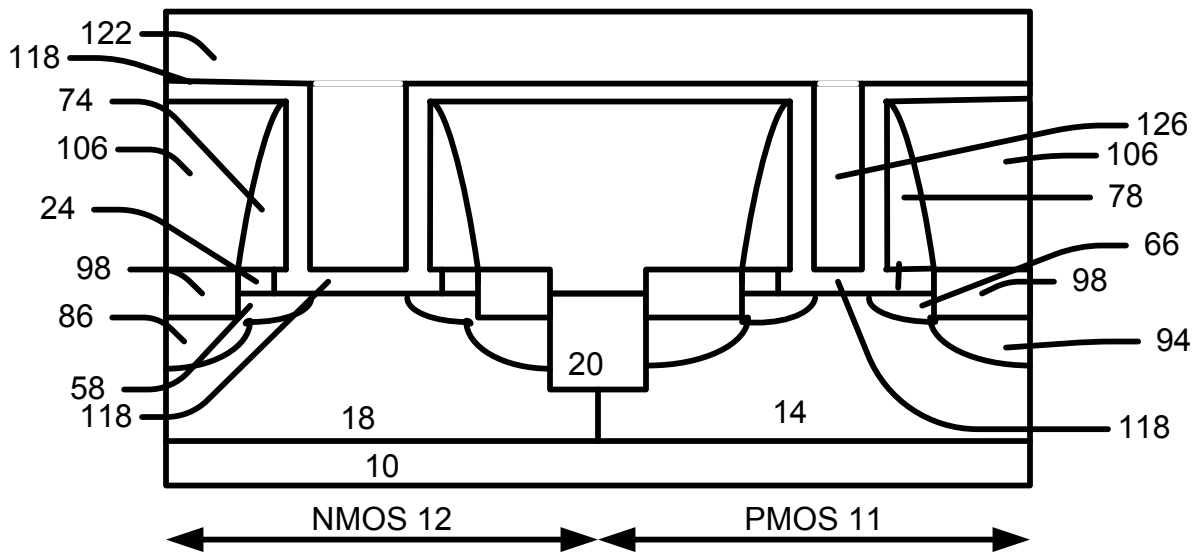


FIGURE 16

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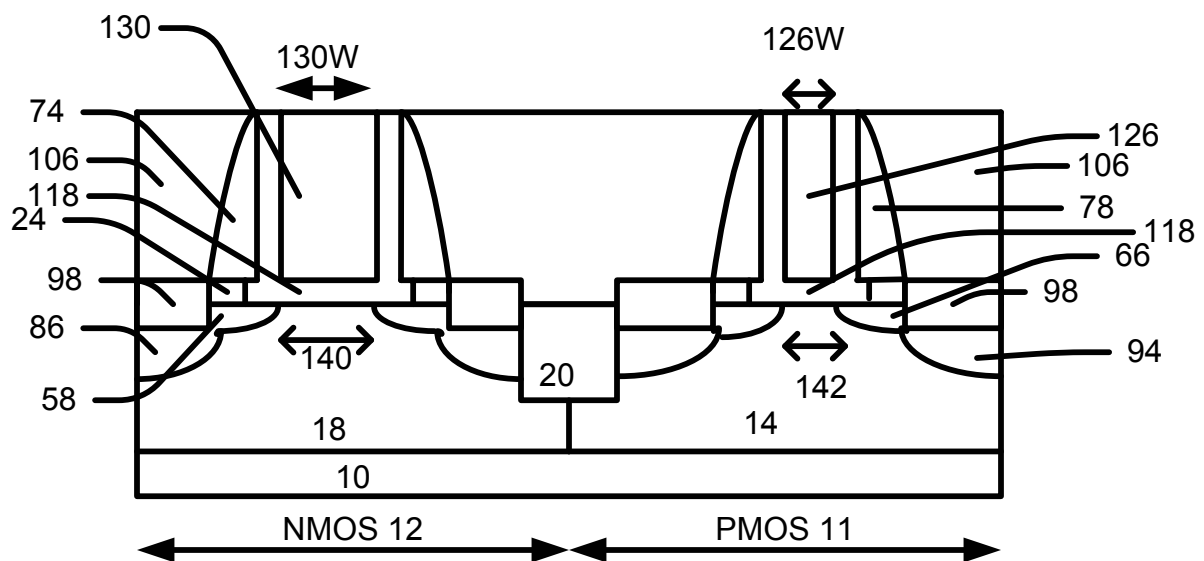
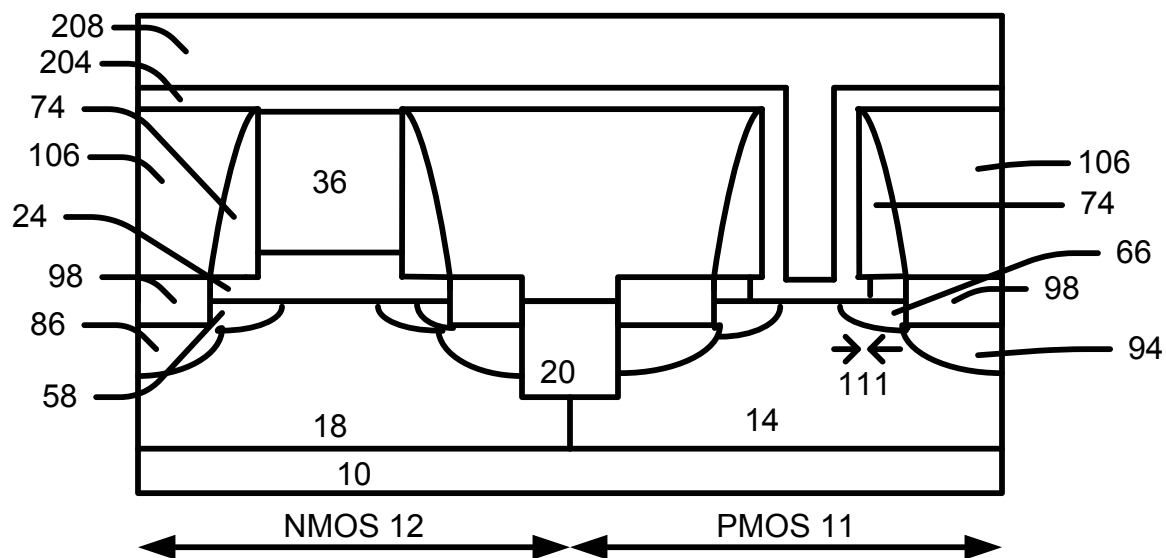


FIGURE 17

A detailed cross-sectional view of a semiconductor device, specifically a CMOS transistor. The device is built on a substrate 10, which is divided into a P-WELL 18 and an N-WELL 14. The P-WELL 18 contains an NMOS 12, and the N-WELL 14 contains a PMOS 11. The NMOS 12 has a gate stack 20, a gate 24, and a channel region 36. The PMOS 11 has a gate stack 20, a gate 24, and a channel region 36. The device is covered by a passivation layer 200. Various other layers and features are labeled, including 106, 74, 98, 86, 58, 66, 94, and 111. The NMOS 12 and PMOS 11 are shown with their respective channel regions 36 and gate stacks 20. The device is shown in a cross-sectional view, with the NMOS 12 on the left and the PMOS 11 on the right. The substrate 10 is the base layer, and the P-WELL 18 and N-WELL 14 are the well regions. The gate stack 20 is the top layer of the transistor, and the gate 24 is the gate electrode. The channel region 36 is the region where the current flows. The passivation layer 200 is the top layer of the device. The other labels (106, 74, 98, 86, 58, 66, 94, 111) point to various other features and layers of the device.

## FIGURE 18



## FIGURE 19

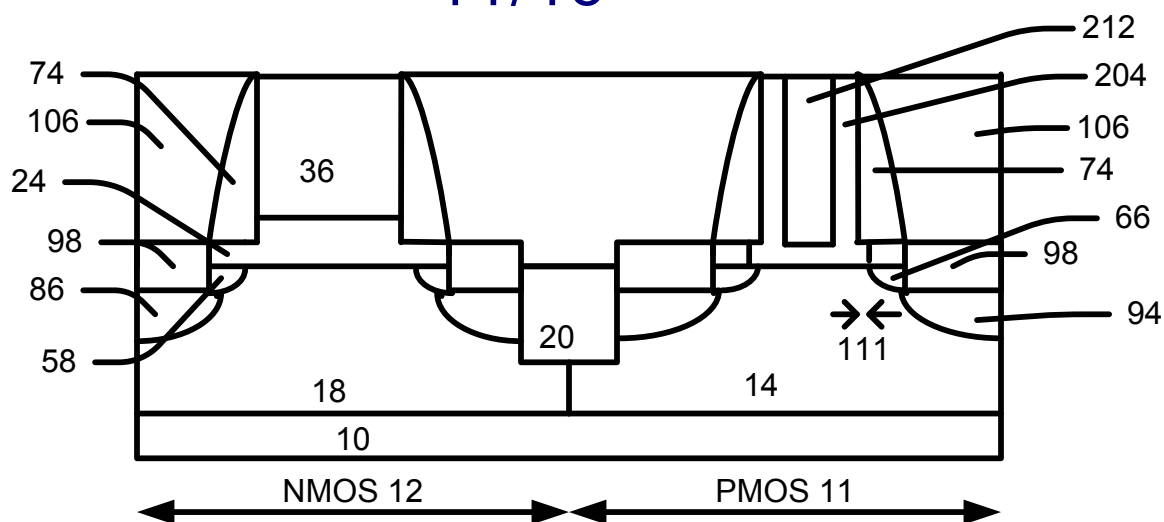


FIGURE 20

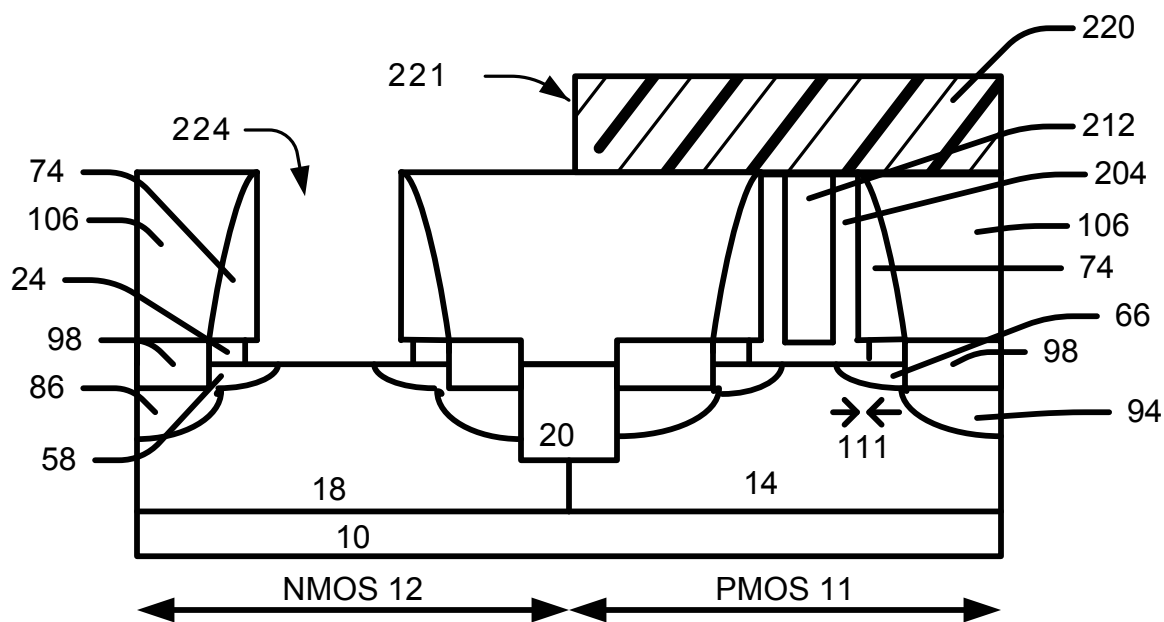


FIGURE 21

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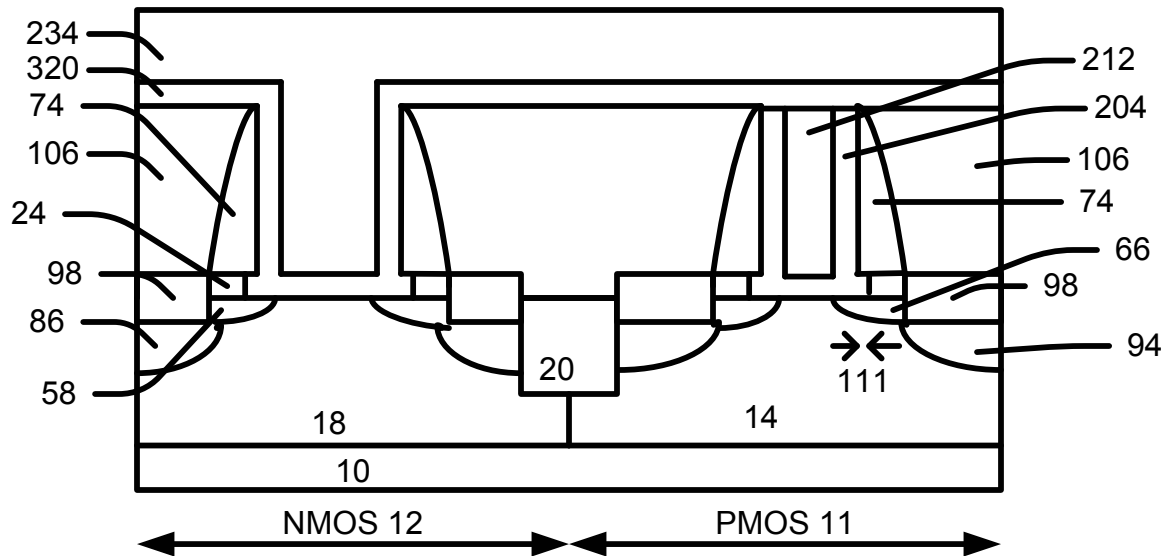


FIGURE 22

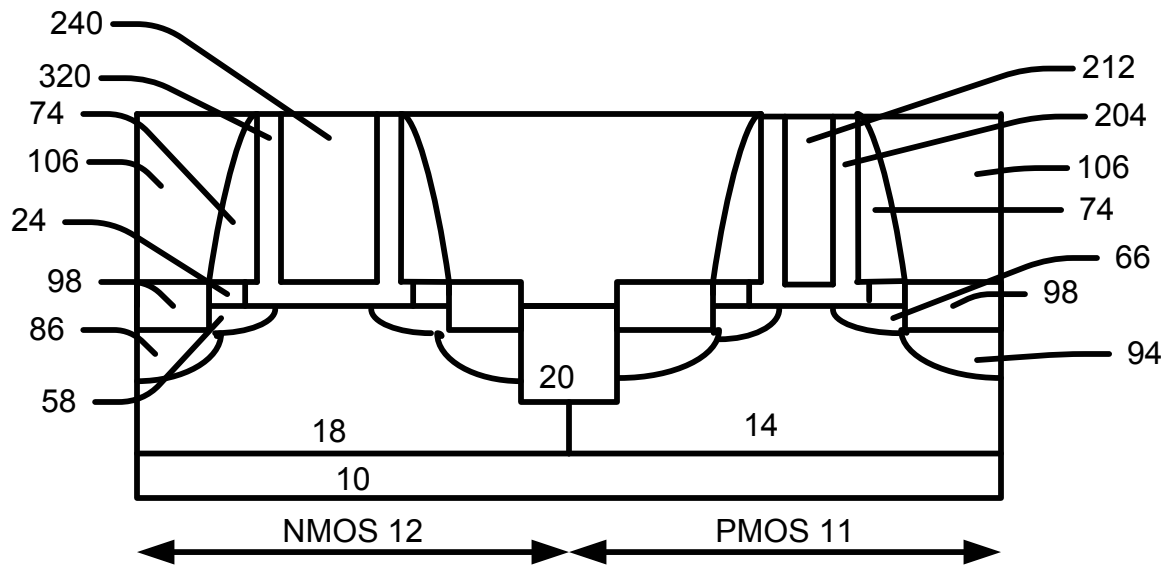


FIGURE 23

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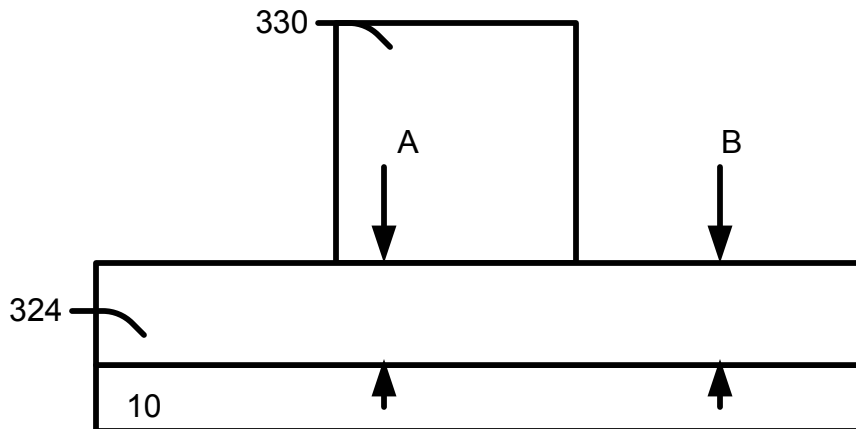


FIGURE 24A

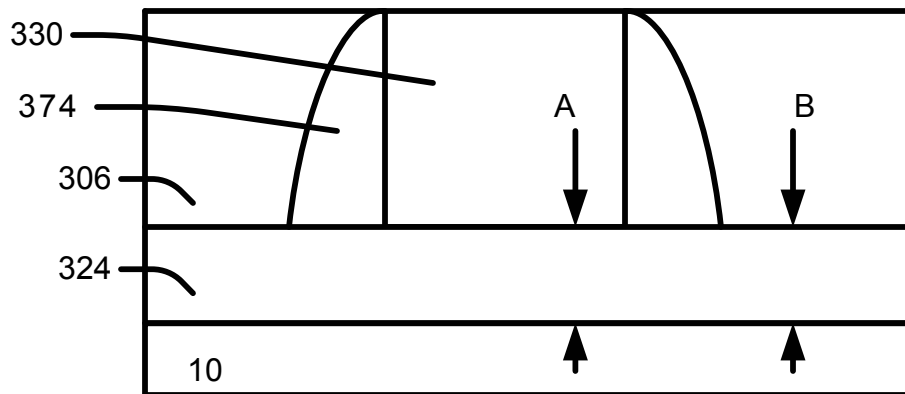


FIGURE 24B

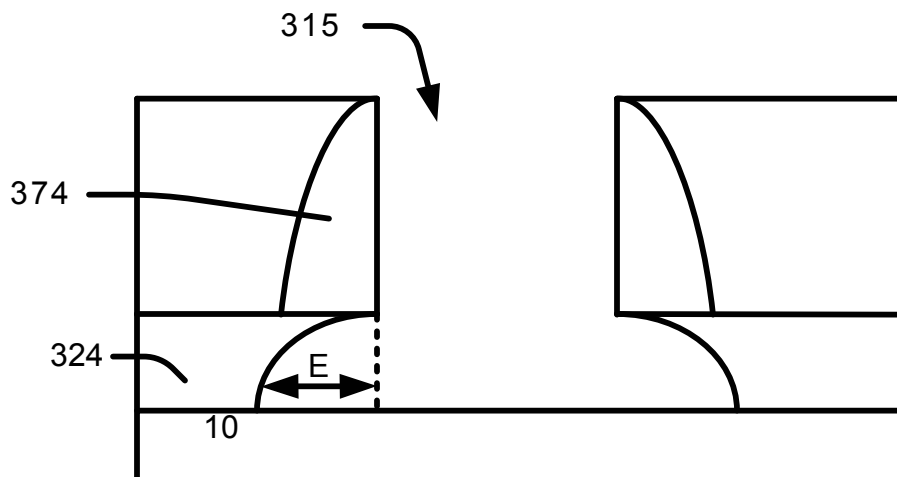


FIGURE 24C

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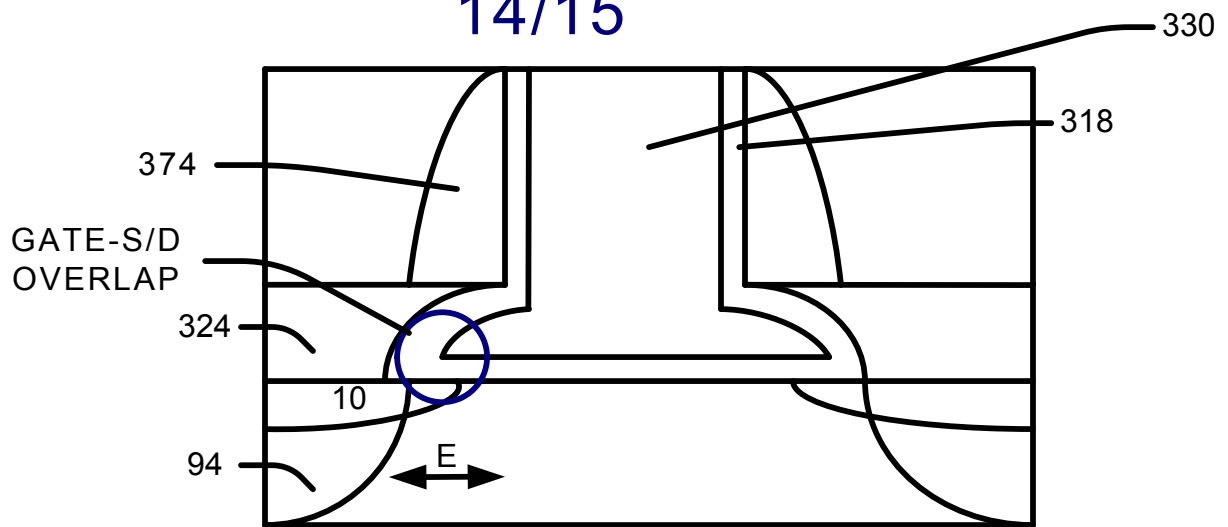


FIGURE 24D

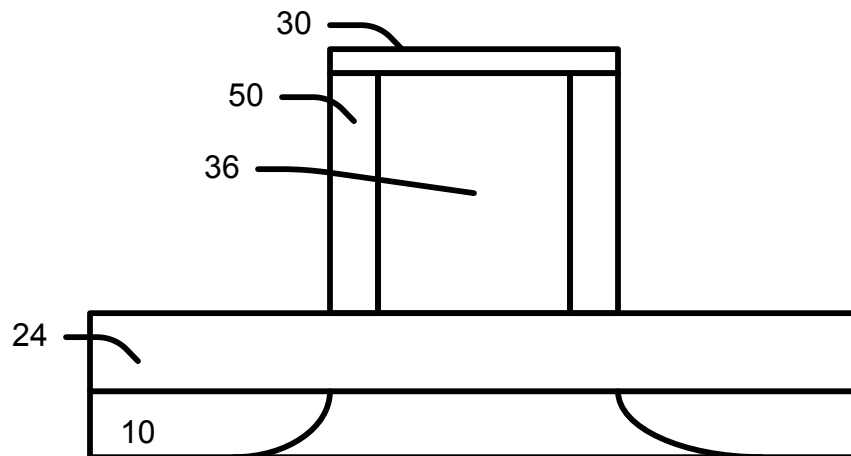


FIGURE 25A-1

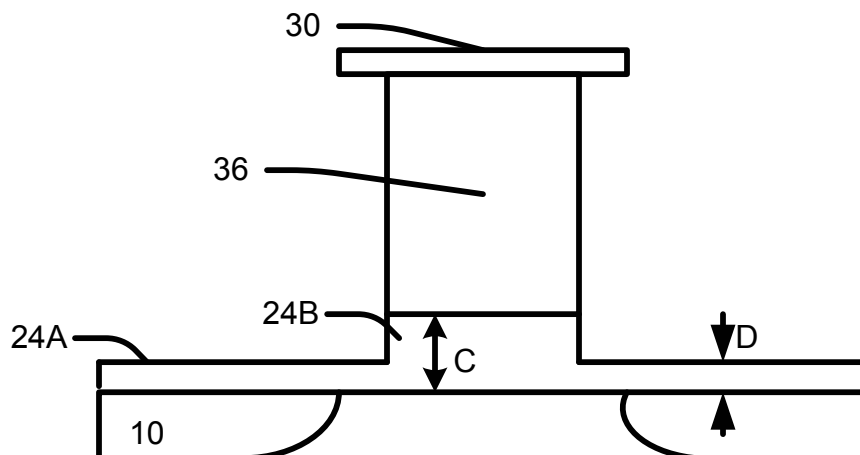


FIGURE 25A-2

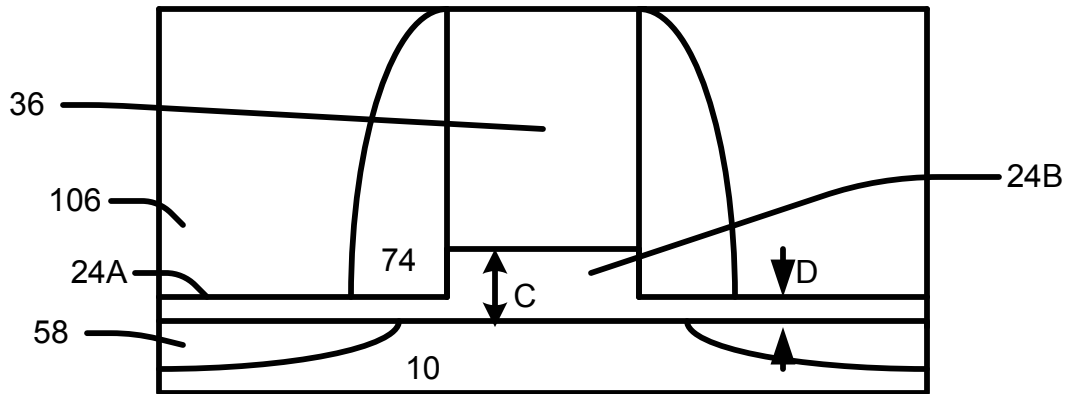


FIGURE 25B

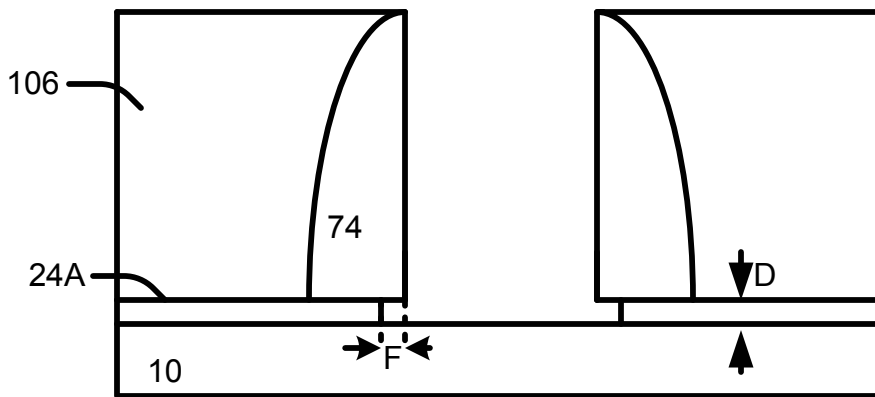


FIGURE 25C

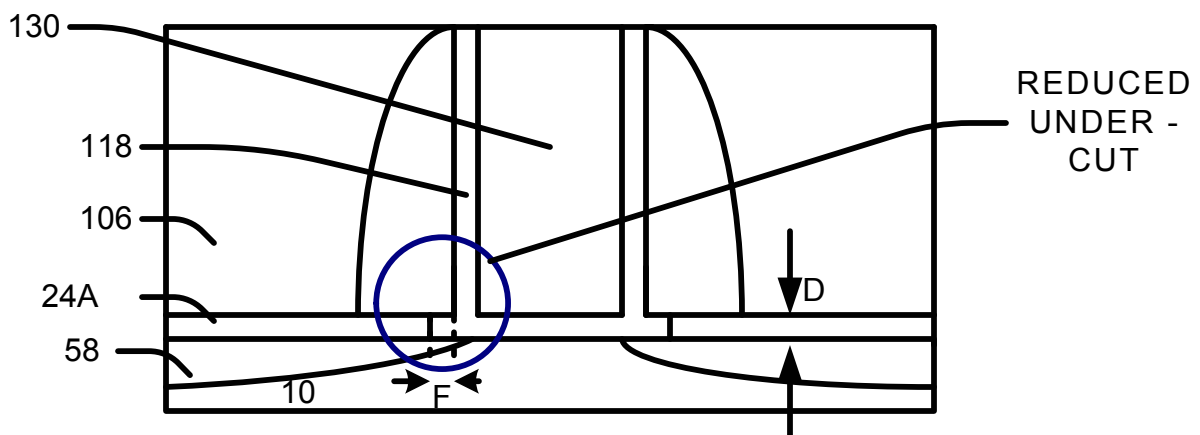


FIGURE 25D