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COMPLETE SPECIFICATION

DRAWINGS ATTACHED

Semiconductor Devices

We, RADIO CORPORATION OF AMERICA, a Corporation organized under the laws of the State of Delaware, United States of America, of 30, Rockefeller Plaza, City and State of New York, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to semiconductive devices, and more particularly, the invention relates to insulated-gate field-effect semiconductor devices and to methods of making them.

The type of semiconductor device in which the conductivity of a portion of a semiconductive wafer may be modulated by an applied electric field is known as a field-effect device. One kind of field-effect device has a dielectric or insulating layer over a portion of the surface of a crystal-line semiconductive wafer, and has a control electrode deposited on this insulating layer. Units of this kind are known as insulated gate field-effect devices, and may comprise a layer or wafer of crystalline semiconductive material, two spaced conductive regions adjacent to one face of said layer, a film of insulating material on said one face between said two spaced regions, two metallic electrodes bonded respectively to said two spaced conductive regions, and a metallic control electrode on said insulating film between said two spaced regions.

One class of insulated gate device is known as the MOS (Metal-Oxide Semiconductor) transistor, and is described by S. R. Hofstein and F. P. Heiman in "The Silicon Insulated Gate Field-Effect Transistor", PROC. IEEE Vol. 51, page 1190, September 1963. In devices of this type, the insulator usually consists of silicon oxide, the metallic con-

trol electrode on the insulating film is also known as the gate electrode, and the two electrodes bonded directly to the semiconductive wafer are known as the source and drain electrodes. It is desirable to improve the stability and uniformity of the electrical characteristics of such MOS devices.

An object of this invention is to provide improved field-effect semiconductor devices having improved stability with respect to their electrical characteristics.

According to one aspect of the present invention, there is provided an insulated gate field-effect semiconductor device comprising: a crystalline semiconductive body of a given conductivity type having at least one major face; first and second spaced low resistivity regions constituting source and drain electrodes in said body immediately adjacent to said one major face; metallic electrode contacts to said regions; a layer of dielectric material on said face covering the gap between said regions, said dielectric layer containing a substance which is a conductivity modifier for said body; and a metallic gate electrode on said dielectric layer over the gap between said regions.

It is another object of this invention to provide improved methods of fabricating improved field-effect semiconductor devices.

According to another aspect of the present invention, there is provided a method of fabricating an insulated gate field-effect semiconductor device which method comprises the steps of: preparing a crystalline semiconductive body with at least one major face; forming two spaced low resistivity regions in said body adjacent to said one major face; depositing a layer of undoped dielectric material on said major body face over the gap between said first and second regions; depositing another layer of dielectric material on said first dielectric layer, said

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other layer containing at least one-half percent by weight of a substance which is a conductivity modifier in said body; depositing a first metallic contact on one said low resistivity region; depositing a second metallic contact on the other said low resistivity region; and depositing a third metallic contact on said other dielectric layer over the gap between said regions.

According to yet another aspect of the present invention, there is provided a method of fabricating an insulated gate field-effect semiconductor device which method comprises the steps of: preparing a crystalline silicon body with at least one major face and a resistivity of at least 1 ohm-cm; forming two spaced low resistivity regions in said body adjacent to said one major face by diffusing a conductivity modifier into portions of said face; depositing a first layer of undoped silicon oxide on said major body face over the gap between said first and second regions; depositing another layer of silicon oxide on said first silicon oxide layer, said other layer containing at least one-half percent by weight of phosphorus; depositing a first metallic contact on one said low resistivity region; depositing a second metallic contact on the other said low resistivity region; and depositing a third metallic contact on said other silicon oxide layer over the gap between said regions.

The invention will now be described in greater detail by examples considered in conjunction with the accompanying drawings, in which:

Figures 1 to 5 are cross-sectional elevational views of a semiconductive body illustrating successive steps in the fabrication of a semiconductive device according to one embodiment of the invention;

Figures 6 to 8 are cross-sectional elevational views of a semiconductive body illustrating successive steps in the fabrication of a semiconductive device according to another embodiment of the invention;

Figure 9 is a schematic diagram of one form of apparatus useful in the practice of the invention; and

Figure 10 is a graph showing the variation of transconductance with time for a field-effect device as described, and for a comparable prior art device.

EXAMPLE I

A crystalline semiconductive body 10 (FIGURE 1) is prepared with at least one major face 11. The exact size, shape and conductivity of semiconductive body 10 is not critical. Conveniently, the semiconductive body or substrate 10 is a die having two opposing major faces 11 and 12. In this example, the semiconductive die 10 is approximately 50 mils square, approximately 6 mils thick, consists of monocrystalline silicon, and is of P-type conductivity.

The resistivity of die 10 is preferably at least 1 ohm-cm, that is, equal to or greater than 1 ohm-cm. Immediately adjacent to one major die face 11 two spaced low resistivity regions 13 and 15 are formed. Formation of low resistivity regions 13 and 15 may be accomplished by techniques known to the art, such as by diffusion of a conductivity modifier through a mask into selected portions of die face 11, and need not be described here. In this example, the two spaced low resistivity regions 13 and 15 are formed by diffusion of a donor such as arsenic, antimony, phosphorus, or the like. To ensure low resistivity in regions 13 and 15, the diffusion is accomplished under such conditions of source concentration and heating profile that the concentration of charge carriers (electrons in this example) at the surface of regions 13 and 15 is at least 10^{19} per cm^3 . This concentration decreases with increasing depth, but regions 13 and 15 are less than 0.5 mil thick. P-N junctions 14 and 16 are formed at the boundaries between the N-type diffused regions 13 and 15 respectively and the P-type bulk of the wafer. The precise size and shape of the two diffused regions is not critical. The two regions 13 and 15 may be of the same size and shape, or may differ in this respect, but preferably the space between the two regions should be less than one mil. In this example, the two donor-diffused low resistivity regions 13 and 15 are 10 mils long, 3 mils wide, and 0.1 mil thick. The two regions 13 and 15 are separated along their 10 mil length by a gap or space of approximately 0.2 mils.

A first layer 20 (FIGURE 2) of substantially pure or undoped silicon oxide is formed on the one major face 11 of die 10. Silicon oxide layer 20 may be formed by thermal decomposition of a siloxane compound, as described below. Alternatively, where the die 10 consists of silicon, the silicon oxide layer 20 may be formed by thermal oxidation of the die. In this example, silicon die 10 is heated in an oxygen ambient for from 7 to 12 minutes at a temperature of approximately 1050°C . The first silicon oxide layer 20 thus formed is from 250 to 300 Angstroms thick, and consists of substantially pure or undoped silicon oxide. The undoped layer 20 acts as a barrier to prevent diffusion into the semiconductive die of conductivity modifiers from the doped silicon oxide layer which is deposited next. Heavily doped silicon oxide does not adhere to a silicon surface as well as pure or undoped silicon oxide. However, heavily doped silicon oxide does adhere well to undoped silicon oxide. Therefore, the undoped silicon oxide layer 20 also serves as a firm base to ensure the adherence of the doped silicon oxide layer which is next deposited.

Referring now to FIGURE 3, a second silicon oxide layer 22 is deposited on the first silicon oxide layer 20. The second silicon oxide layer 22 is formed by the thermal decomposition of a siloxane compound as described below, and contains a substance that is a conductivity modifier in semiconductive body 10. Preferably, the layer 22 contains at least one-half percent by weight of the conductivity modifier. In this example, the conductivity modifier is phosphorus. The silicon oxide layer 22 may contain as much as 10 to 30 percent phosphorus by weight, usually in the form of P_2O_5 . The doped silicon oxide layer 22 is conveniently from 300 to 350 Angstroms thick. In the drawing, the thickness of the silicon oxide layers is not to scale, having been exaggerated for greater clarity.

Two spaced openings or apertures 25 and 27 (FIGURE 4) are now formed in the silicon oxide coatings 20 and 22 by any convenient method. For example, portions of the surface of the silicon oxide layer may be masked by coating with an acid resist. Portions of the silicon oxide layers over the low resistivity regions 13 and 15 are then removed by conventional etching processes well known to the art, leaving openings 25 and 27. One opening 25 is formed entirely within one low resistivity region 13, and the other opening 27 is formed entirely within the other low resistivity wafer region 15. If an acid resist has been utilized, it is removed by means of a suitable solvent prior to the next step.

Referring now to FIGURE 5, a metal such as aluminium, palladium, chromium, or the like is deposited by any convenient method, for example by evaporation through a mask, on the exposed portions of wafer regions 13 and 15, and also on a portion of the uppermost silicon oxide layer 22 over the gap or space between regions 13 and 15. One metallic contact 26 is thus formed to region 13, another metallic contact 28 to region 15, and a third metallic contact 29 on the uppermost silicon oxide layer 22 over the gap between regions 13 and 15. In operation, contacts 26 and 28 serve as the source and drain electrodes, while contact 29 serves as the control or gate electrode of the device. Electrical leads 36, 38 and 39 may be attached to electrodes 26, 28 and 29 respectively. Conveniently, lead wires 36, 38 and 39 are gold wires attached to the electrodes 26, 28 and 29 by thermocompression bonding. In operation, the unit may be biased as shown. The unit may be encapsulated and cased by standard techniques known to the semiconductor art.

The device of this example may be operated as follows. Leads 36 and 38 are utilized as the source and drain leads, respectively, while lead 39 is the control or

gate lead. Die face 12 and source lead 36 are grounded. Drain lead 38 is positively biased by a source of direct current potential such as a battery 50, so that the drain electrode or contact 28 and the drain region 15 of the device are also poled positive with respect to the source region 13 and the source electrode 26. The electrical load, shown as a resistance 52, is connected between the positive pole of battery 50 and the drain lead 38. A signal input on gate lead 39 results in an amplified signal output developed across the load resistor 52.

One method of depositing a dielectric or insulating coating on a semiconductive wafer or die is to treat the wafer in the vapors of an organic siloxane compound at a temperature below the melting point of the wafer, but above the temperature at which the siloxane compound decomposes, so that an adherent insulating coating believed to consist principally of silicon dioxide is formed on the wafer surface. For example, see British Patent No. 946,229.

A method of applying a doped silicon oxide coating to a semiconductive body, and apparatus useful for this purpose, will now be described.

A form of apparatus useful in the practice of the invention is illustrated in FIGURE 9. The apparatus 90 comprises a flow meter 91 for regulating the flow of the carrier gas; a drier or drying column 92 for purification of the carrier gas utilized; and an inlet tube 93 provided with stop-cocks 94 and 94' for bypassing a bubbler 95. The bubbler 95 contains a liquid mixture 96, which consists of an organic siloxane compound and a volatile doping agent or conductivity modifier for the particular semiconductor utilized. The organic siloxane compound may, for example, consist of 10 volumes of ethyl triethoxysilane, and the volatile doping agent may be 1 volume of trimethyl phosphate. The proportions of the conductivity modifier and the siloxane compound may be varied to obtain different concentrations of the doping agent in the silicon oxide layers deposited. Inlet tube 93 is attached to one end of furnace tube 97. The apparatus 90 generally, including inlet tube 93 and furnace tube 97, is suitably made of refractory materials, such as high melting glass, or fused quartz. The furnace tube 97 is surrounded by a furnace 98, which is maintained at approximately 700°C. An inert carrier gas such as nitrogen, argon, helium, and the like, is passed through the apparatus 90 in the direction indicated by the arrows. Since siloxane compounds generally begin to decompose at approximately 600°C, the furnace temperature of 700°C is sufficient to ensure pyrolysis of siloxane vapours introduced into the furnace tube 97 by the flowing carrier gas. The trimethyl

phosphate is also decomposed at this temperature, and is oxidized to phosphorus pentoxide P_2O_5 .

The mixed vapours of the inert carrier gas, the doping agent, and the thermal decomposition products of the siloxane compound, which include silicon dioxide, exit from the other end of furnace tube 97 by way of jet 99, and the jet stream of mixed vapours and carrier gas (not shown) thus formed impinges upon one face 11 of the semiconductive die 10. A coating of phosphorus-doped silicon oxide is thus deposited on face 11 of die 10. The jet stream cools off rapidly as it leaves the jet 99, and hence the temperature of the jet stream at the point where it impinges on the semiconductive wafer can be varied by adjusting the distance between the jet or orifice 99 and the semiconductive die or wafer 10. For a furnace temperature of approximately 700°C , and a separation between jet 99 and semiconductive die 10 of approximately 2 millimeters, the temperature of the jet impinging on the semiconductive die is approximately 150°C . For a more detailed description of this method of depositing a doped silicon oxide coating on a semiconductive wafer, see United States Patent No. 3,114,663. It is thus seen that doped silicon oxide coatings can be deposited by this technique on semiconductive wafers while maintaining the semiconductor at very moderate temperatures. Undoped silicon oxide coatings can be similarly deposited by omitting the doping agent from the liquid 96 in bubbler 95.

EXAMPLE II

It may be desirable to fabricate devices according to the invention utilizing precision photolithographic processes. In these processes a thin layer of a photoresist is deposited on the uppermost oxide coating. The photoresist may, for example, be a bichromated protein such as bichromated gum arabic, bichromated gelatin or bichromated albumin.

The photoresist layer may be deposited directly on an oxide layer containing a conductivity modifier, such as the phosphorus-doped silicon oxide layer 22 of Example I. However, it has been found that the photoresist layer does not adhere to the phosphorus-doped silicon oxide as uniformly as a photoresist layer adheres on pure undoped silicon oxide. Accordingly, when utilizing photolithographic techniques, it has been found advantageous to deposit, as a third layer on the semiconductive die, a thin coating of pure undoped silicon oxide over the doped silicon oxide layer 22. The photoresist layer is then deposited on the surface of this pure silicon oxide layer, and adheres more uniformly thereto.

In this embodiment, a crystalline semiconductive die 10 having a resistivity of at least

1 ohm-cm is prepared with opposing major faces 11 and 12, as in FIGURE 1, and two spaced low-resistivity regions 13 and 15 are formed adjacent to one major face 11 by diffusion of a conductivity modifier into selected portions of die face 11. The low resistivity regions 13 and 15 may be of the same conductivity type as the bulk of the die. For example, the die 10 may be lightly N-type, containing approximately 10^{16} charge carriers (electrons) per cm^3 . The regions 13 and 15 are given a surface concentration of at least 10^{19} charge carriers per cm^3 . The boundaries 14 and 16 may then be described as N- N⁺ junctions. A first layer 20 (FIGURE 2) of pure or undoped silicon oxide is deposited on major die face 11. This first layer serves as a barrier to prevent diffusion of conductivity modifiers from the next silicon oxide layer into the semiconductor die. A second silicon oxide layer 22 (FIGURE 3) is deposited on the first silicon oxide layer 20. The second layer 22 is conveniently formed by the thermal decomposition of a siloxane compound, as described above in connection with FIGURE 9, and is heavily doped with a conductivity modifier, such as phosphorus.

Referring now to FIGURE 6, a third silicon oxide coating 24 of pure or undoped silicon oxide is deposited on the second silicon oxide layer 22. Layer 24 is conveniently formed by thermal decomposition of a siloxane compound, as described above in connection with FIGURE 9. A pure siloxane compound, such as ethyltriethoxy silane, or the like, is utilized as the liquid 96 in the bubbler 95, in order to deposit the pure or undoped silicon oxide layer 24.

A thin coating 30 (FIGURE 6) of a photoresist is deposited on the third silicon oxide layer 24. The photoresist utilized may be one of those previously mentioned, or may be a commercially available photoresist such as Eastman Kodak "KPR" and "KMER", or Clerkin Company "CFC", or Pitman Company "HOT TOP".

Portions of the photoresist layer 30 are illuminated by ultra-violet light, then polymerized, and hardened. The remaining portions of photoresist 30 are removed by a suitable solvent, thus exposing portions of the silicon oxide layer 24. A suitable etchant, such as a hydrofluoric acid solution, is then utilized to remove the exposed portions of silicon oxide layers 24, 22 and 20. Two spaced openings or apertures 25 and 27 (FIGURE 7) are thus formed in the silicon oxide coatings 24, 22 and 20. One opening 25 is formed entirely within one low resistivity region 13, and the other opening 27 is formed entirely within the other low resistivity region 15.

The remaining portions of the photoresist layer 30 are removed by means of a suitable



stripper, such as methylene chloride. A metal such as chromium, palladium, aluminium, and the like, is deposited by any convenient method, such as by evaporation, on the exposed portions of die regions 13 and 15, and also on a portion of the uppermost silicon oxide layer 24 over the gap or space between regions 13 and 15. A first metallic contact 26 (FIGURE 8) is thus formed to die region 13; a second metallic contact 28 is formed to die region 15; and a third metallic contact 29 is formed on the uppermost silicon oxide layer 24 over the gap or spaced between the regions 13 and 15. The subsequent steps of attaching lead 26, 28 and 29 respectively, then encapsulating and casing the device, are accomplished by standard techniques of the semiconductor art. The completed unit is biased and operated in the same manner as described in EXAMPLE I above in connection with FIGURE 5.

In FIGURE 10, Curve A is a plot showing the drain current (in milliamperes) at different values of gate bias (in volts) for a typical insulated gate field-effect device shortly after fabricating. When the gate bias is positive, and is one volt or less, essentially no drain current flows. When such insulated gate field-effect transistors are stored at elevated temperatures with a positive bias on the gate, their electrical characteristics, particularly the transconductance or transfer characteristic, tend to change. Curve B is a plot showing the drain current (in milliamperes) at different values of gate bias (in volts) for an insulated gate field-effect device according to EXAMPLE II after 16 hours storage at 125°C with a positive gate bias of 10 volts applied during the entire storage period. This device included between the gate electrode and the semiconductive die a triple layer of silicon oxide, comprising a central layer heavily doped with phosphorus, between two layers of essentially pure or undoped silicon oxide. In that device according to EXAMPLE II, the graph of which is drawn in FIGURE 10, there is only a small and tolerable change in the transfer characteristic. The positive gate bias at which the drain current becomes essentially zero is now 0.5 volts, and in general, Curve B is shifted by approximately 0.5 volts from the corresponding values of these devices after fabrication and before storage, which were shown in Curve A. For comparison, Curve C shows the drain current (in milliamperes) at different values of gate bias (in volts) after storage for 16 hours at 125°C with 10 volts positive gate bias for a prior art insulated gate field-effect transistor having only pure or undoped silicon oxide between the gate electrode and the semiconductive die. In the prior art device,

some drain current flows even at zero gate bias, and in general, Curve C is shifted by approximately 5 volts from the corresponding values of the device before storage, as shown in Curve A. A change in characteristics of this magnitude is undesirable for many circuit applications. It is thus seen that after storage at elevated temperatures the insulated gate field-effect transistor according to the embodiment of EXAMPLE II is more stable as to transfer characteristic than the corresponding prior art device by a factor of 10.

The exact reasons for the improved stability of insulated gate field-effect semiconductor devices according to the invention are not presently understood. However, the invention may be practiced regardless of whatever theoretical explanation is advanced to explain the results obtained.

The above EXAMPLES are by way of illustration only, and not limitation. Other doping agents such as boron and arsenic may be utilized instead of phosphorus. Other dielectrics or insulators, such as magnesium oxide and the like, may be utilized instead of silicon oxide. The conductivity types of the various regions in the device may be reversed. Other siloxane compounds such as dimethyl diethoxysilane, tetraethoxysilane, amyl triethoxysilane, and vinyl triethoxysilane may be utilized. Other semiconductive materials such as germanium and silicon-germanium alloys may be used instead of silicon.

WHAT WE CLAIM IS:

1. An insulated gate field-effect semiconductor device comprising: a crystalline semiconductive body of a given conductivity type having at least one major face; first and second spaced low resistivity regions constituting source and drain electrodes in said body immediately adjacent to said one major face; metallic electrode contacts to said regions; a layer of dielectric material on said face covering the gap between said regions, said dielectric layer containing a substance which is a conductivity modifier for said body; and a metallic gate electrode on said dielectric layer over the gap between said regions.

2. An insulated gate field-effect semiconductor device according to Claim 1, wherein said dielectric layer contains at least one-half percent by weight of a substance which is a conductivity modifier for said body.

3. An insulated gate field-effect semiconductor device according to Claim 1 or Claim 2, wherein said crystalline semiconductive body is silicon having a resistivity of at least 1 ohm-cm.

4. An insulated gate field-effect semiconductor device according to Claim 1 or Claim 2, wherein said crystalline body is silicon having a resistivity of at least 1 ohm-cm, 130

wires 36, 38 and 39
to the metallic contacts

stripper, such as methylene chloride. A metal such as chromium, palladium, aluminum, and the like, is deposited by any convenient method, such as by evaporation, on the exposed portions of die regions 13 and 15, and also on a portion of the uppermost silicon oxide layer 24 over the gap or space between regions 13 and 15. A first metallic contact 26 (FIGURE 8) is thus formed to die region 13; a second metallic contact 28 is formed to die region 15; and a third metallic contact 29 is formed on the uppermost silicon oxide layer 24 over the gap or spaced between the regions 13 and 15. The subsequent steps of attaching lead 26, 28 and 29 respectively, then encapsulating and casing the device, are accomplished by standard techniques of the semiconductor art. The completed unit is biased and operated in the same manner as described in EXAMPLE I above in connection with FIGURE 5.

In FIGURE 10, Curve A is a plot showing the drain current (in milliamperes) at different values of gate bias (in volts) for a typical insulated gate field-effect device shortly after fabricating. When the gate bias is positive, and is one volt or less, essentially no drain current flows. When such insulated gate field-effect transistors are stored at elevated temperatures with a positive bias on the gate, their electrical characteristics, particularly the transconductance or transfer characteristic, tend to change. Curve B is a plot showing the drain current (in milliamperes) at different values of gate bias (in volts) for an insulated gate field-effect device according to EXAMPLE II after 16 hours storage at 125°C with a positive gate bias of 10 volts applied during the entire storage period. This device included between the gate electrode and the semiconductive die a triple layer of silicon oxide, comprising a central layer heavily doped with phosphorus, between two layers of essentially pure or undoped silicon oxide. In that device according to EXAMPLE II, the graph of which is drawn in FIGURE 10, there is only a small and tolerable change in the transfer characteristic. The positive gate bias at which the drain current becomes essentially zero is now 0.5 volts, and in general, Curve B is shifted by approximately 0.5 volts from the corresponding values of these devices after fabrication and before storage, which were shown in Curve A. For comparison, Curve C shows the drain current (in milliamperes) at different values of gate bias (in volts) after storage for 16 hours at 125°C with 10 volts positive gate bias for a prior art insulated gate field-effect transistor having only pure or undoped silicon oxide between the gate electrode and the semiconductive die. In the prior art device,

some drain current flows even at zero gate bias, and in general, Curve C is shifted by approximately 5 volts from the corresponding values of the device before storage, as shown in Curve A. A change in characteristics of this magnitude is undesirable for many circuit applications. It is thus seen that after storage at elevated temperatures the insulated gate field-effect transistor according to the embodiment of EXAMPLE II is more stable as to transfer characteristic than the corresponding prior art device by a factor of 10.

The exact reasons for the improved stability of insulated gate field-effect semiconductor devices according to the invention are not presently understood. However, the invention may be practiced regardless of whatever theoretical explanation is advanced to explain the results obtained.

The above EXAMPLES are by way of illustration only, and not limitation. Other doping agents such as boron and arsenic may be utilized instead of phosphorus. Other dielectrics or insulators, such as magnesium oxide and the like, may be utilized instead of silicon oxide. The conductivity types of the various regions in the device may be reversed. Other siloxane compounds such as dimethyl diethoxysilane, tetraethoxysilane, amyl triethoxysilane, and vinyl triethoxysilane may be utilized. Other semiconductive materials such as germanium and silicon-germanium alloys may be used instead of silicon.

WHAT WE CLAIM IS:

1. An insulated gate field-effect semiconductor device comprising: a crystalline semiconductive body of a given conductivity type having at least one major face; first and second spaced low resistivity regions constituting source and drain electrodes in said body immediately adjacent to said one major face; metallic electrode contacts to said regions; a layer of dielectric material on said face covering the gap between said regions, said dielectric layer containing a substance which is a conductivity modifier for said body; and a metallic gate electrode on said dielectric layer over the gap between said regions.
2. An insulated gate field-effect semiconductor device according to Claim 1, wherein said dielectric layer contains at least one-half percent by weight of a substance which is a conductivity modifier for said body.
3. An insulated gate field-effect semiconductor device according to Claim 1 or Claim 2, wherein said crystalline semiconductive body is silicon having a resistivity of at least 1 ohm-cm.
4. An insulated gate field-effect semiconductor device according to Claim 1 or Claim 2, wherein said crystalline body is silicon having a resistivity of at least 1 ohm-cm,

wires 36, 38 and 39 to the metallic contacts





and said dielectric layer contains at least one-half percent by weight of phosphorus.

5 An insulated gate field-effect semiconductor device according to any one of the preceding claims, wherein said layer of dielectric material is a layer of silicon oxide on said body face covering the gap between said first and second regions.

6 An insulated gate field-effect semiconductor device according to any one of the preceding claims, wherein a layer of undoped dielectric material on said body face covers the gap between said first and second regions and is positioned between said body face and said first layer of dielectric material which contains the conductivity modifier, said metallic gate electrode being positioned on said first dielectric layer.

7 An insulated gate field-effect semiconductor device according to Claim 6, wherein said crystalline semiconductive body is silicon having a resistivity of at least 1 ohm-cm.

8 An insulated gate field-effect semiconductor device according to Claim 6 or Claim 7, wherein said first dielectric layer contains at least one-half percent by weight of a substance which is a conductivity modifier in silicon.

9 An insulated gate field-effect semiconductor device according to Claim 6 or Claim 7, wherein said first layer of dielectric material contains at least one-half percent by weight phosphorus.

10 An insulated gate field-effect semiconductor device according to claim 7, characterized in that said two layers of dielectric material comprise silicon oxide, and said first layer of silicon oxide contains at least one-half percent by weight phosphorus.

11 An insulated gate field-effect semiconductor device according to any one of Claims 1 to 5, wherein there is a layer of undoped dielectric material on said body face covering the gap between said first and second regions and positioned between said body face and said first layer of dielectric material which contains the conductivity modifier, and a third layer of dielectric material which is undoped and positioned on said first layer, said metallic gate electrode being positioned on said third dielectric layer over the gap between said first and second regions.

12 An insulated gate field-effect semiconductor device according to Claim 11, wherein in all three of said layers of dielectric

material comprise silicon oxide.

13 A method of fabricating an insulated gate field-effect semiconductor device which method comprises the steps of: preparing a crystalline semiconductor body with at least one major face; forming two spaced low resistivity regions in said body adjacent to said one major face; depositing a layer of undoped dielectric material on said major body face over the gap between said first and second regions; depositing another layer of dielectric material on said first dielectric layer, said other layer containing at least one-half percent by weight of a substance which is a conductivity modifier in said body; depositing a first metallic contact on one said low resistivity region; depositing a second metallic contact on the other said low resistivity region; and depositing a third metallic contact on said other dielectric layer over the gap between said regions.

14 A method of fabricating an insulated gate field-effect semiconductor device which method comprises the steps of: preparing a crystalline silicon body with at least one major face and a resistivity of at least 1 ohm-cm; forming two spaced low resistivity regions in said body adjacent to said one major face by diffusing a conductivity modifier into portions of said face; depositing a first layer of undoped silicon oxide on said major body face over the gap between said first and second regions; depositing another layer of silicon oxide on said first silicon oxide layer, said other layer containing at least one-half percent by weight of phosphorus; depositing a first metallic contact on one said low resistivity region; depositing a second metallic contact on the other said low resistivity region; and depositing a third metallic contact on said other silicon oxide layer over the gap between said regions.

15 A method of fabricating an insulated gate field-effect semiconductor device substantially as herein described with reference to Figures 1 to 5 or Figures 6 to 8 of the accompanying drawings.

16 An insulated gate field-effect semiconductor device when fabricated by a method according to any one of Claims 13 to 15.

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