

ABSTRACT
METHOD AND APPARATUS USING NOVEL OPERATIONS
IN A PROCESSOR

A novel processor for manipulating packed data. The packed data includes a first data element D1 and a second data element D2. Each of said data elements has a predetermined number of bits. The processor comprises a decoder, a register, and
5 a circuit. The decoder is for decoding a control signal responsive to receiving the control signal. The register is coupled to the decoder. The register is for storing the packed data. The circuit is coupled to the decoder. The circuit is for generating a first result data element R1 and a second data element R2. The circuit is further for generating R1 to represent a total number bits set in D1, and the circuit is further for
10 generating R2 to represent a total number bits set in D2.

(Figure 9)

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