BINARY-WEIGHTED ATTENUATOR HAVING COMPENSATION CIRCUIT

CROSS-REFERENCE TO RELATED APPLICATION(S)

[0001] This application claims priority to U.S. Provisional Application No. 62/381,376 filed August 30, 2016, entitled BINARY-WEIGHTED ATTENUATOR HAVING COMPENSATION CIRCUIT, the disclosure of which is hereby expressly incorporated by reference herein in its respective entirety.

BACKGROUND

Field

[0002] The present disclosure relates to attenuators for electronic applications.

Description of the Related Art

[0003] In electronic applications such as radio-frequency (RF) applications, it is sometimes desirable to amplify or attenuate a signal. For example, a to-be-transmitted signal can be amplified by a power amplifier, and a received signal can be amplified by a low-noise amplifier. In another example, one or more attenuators can be implemented along either or both of the foregoing transmit and receive paths as needed or desired to attenuate the respective signal(s).

SUMMARY

[0004] In a first aspect, the present disclosure provides a radio-frequency attenuator circuit comprising a plurality of attenuation blocks arranged in series between an input node and an output node, each of the plurality of attenuation blocks including a bypass path; and a phase compensation circuit implemented for each of at least some of the attenuation blocks having the respective bypass paths, the phase compensation circuit configured to compensate for an off-capacitance effect associated with the corresponding bypass path, at least one of the attenuation blocks being without a phase compensation circuit, and the at least one attenuation block without the

phase compensation circuit including an attenuation block having a lowest attenuation value.

[0005] In some embodiments, the attenuation blocks can have binary-weighted attenuation values. The binary-weighted attenuation values can include

N values, with an i-th value being $A2^{i-1}$, where *A* is a step attenuation value and i is a positive integer from 1 to N. The step attenuation value A can be, for example, approximately 1dB. The quantity N can include, for example, 2, 3, 4, 5, 6, 7 or 8.

[0006] In some embodiments, at least one of the attenuation blocks can be without a phase compensation circuit. The at least one attenuation block without the phase compensation circuit can include an attenuation block having a lowest attenuation value.

[0007] In some embodiments, at least one of the attenuation blocks can be configured as a pi-attenuator. The at least one attenuation block having the pi-attenuator can include an attenuation block having a highest attenuation value.

[0008] In some embodiments, the bypass path of the attenuation block having the pi-attenuator can include a bypass switching transistor configured to be on when the attenuation block is in a bypass mode and off when in an attenuation mode, such that the bypass switching transistor provides an off-capacitance when in the attenuation mode. The phase compensation circuit of the attenuation block having the pi-attenuator can include a phase compensation circuit configured to compensate for the off-capacitance when the attenuator block is in the attenuation mode. The pi-attenuator can include a resistance, a first shunt path implemented between one end of the resistance and a ground, and a second shunt path implemented between the other end of the resistance and the ground. Each of the first and second shunt paths can include a shunt resistance.

[0009] In some embodiments, the phase compensation circuit associated with the pi-attenuator can include a first compensation capacitance arranged to be electrically parallel with the first shunt resistance, and a second compensation capacitance arranged to be electrically parallel with the second shunt resistance. The off-capacitance of the bypass switching transistor can result in a phase lead change, and the phase compensation circuit can be configured to provide a phase lag change to compensate for the phase lead change. The first and second shunt resistances can have substantially the same value, and the first and second compensation capacitances have substantially the same value.

[0010] In some embodiments, the phase lead change can be by an amount calculated as $\phi = \tan^{-1}(\omega R_1 C_{off}) - \tan^{-1}\left(\omega \frac{R_1 R_L}{R_1+R_L} C_{off}\right)$, and the phase lag change can be by an amount calculated as $\phi = -\tan^{-1}\left(\frac{\omega R_1 R_2' C_C}{R_1+R_2'}\right)$, where ω is 2π times frequency, R_L is load impedance, R_1 is the resistance, C_C is the first local compensation capacitance, and R_2' is an equivalent resistance of a parallel arrangement of the first shunt resistance and the load impedance. The value of the first compensation capacitance can be selected such that magnitude of the phase lag change is substantially the same as magnitude of the phase lead change. The value of the compensation capacitance can be selected such that a gain of the attenuation block is approximately flat over a selected frequency range.

[0011] In some embodiments, at least one of the attenuation blocks can be configured as a bridge-T-attenuator. The bypass path of the attenuation block having the bridge-T-attenuator can include a bypass switching transistor configured to be on when the attenuation block is in a bypass mode and off when in an attenuation mode, such that the bypass switching transistor provides an off-capacitance when in the attenuation mode. The phase compensation circuit of the attenuation block having the bridge-T-attenuator can include a phase compensation circuit configured to compensate for the off-capacitance when the attenuator block is in the attenuation mode.

[0012] In some embodiments, the bridge-T-attenuator can include two first resistances connected in series, a second resistance electrically parallel with the series combination of the two first resistances, and a shunt path implemented between a ground and a node between the two first resistances, the shunt path including a shunt resistance. The phase compensation circuit associated with the bridge-T-attenuator can include a compensation capacitance arranged to be electrically parallel with the shunt resistance.

[0013] In some embodiments, the off-capacitance of the bypass switching transistor can result in a phase lead change, and the phase compensation circuit can be configured to provide a phase lag change to compensate for the phase lead change. The phase lead change can be by an amount calculated as $\phi = \tan^{-1}(\omega R_2 C_{off}) - \tan^{-1}\left(\frac{\omega R_2 C_{off}}{1+\frac{R_2}{R_L}}\right)$, and the phase lag

change can be by an amount calculated as $\phi = -\tan^{-1}\left(\frac{\omega R_1 R_3' C_C}{R_1 + R_3'}\right)$, where ω is 2π times frequency, R_L is load impedance, R_1 is the first resistance, R_2 is the second resistance, C_C is the compensation capacitance, and R_3' is an equivalent resistance of a parallel arrangement of the shunt resistance and a series-combination of the first resistance and the load impedance. The value of the compensation capacitance can be selected such that magnitude of the phase lag change is substantially the same as magnitude of the phase lead change. The value of the compensation capacitance can be selected such that a gain of the attenuation block is approximately flat over a selected frequency range.

[0014] In some embodiments, the attenuator circuit can further include a global bypass path that includes a global bypass switching transistor configured to be on when in a global bypass mode and off when in a global attenuation mode, such that the global bypass switching transistor provides a global off-capacitance when in the global attenuation mode. In some embodiments, the attenuator circuit can further include a global phase compensation circuit configured to compensate for the global off-capacitance when the attenuator circuit is in the global attenuation mode. The global phase compensation circuit can include a first global compensation resistance and a second global compensation resistance arranged in series between the input node and the output node. The global phase compensation circuit can further include a global compensation capacitance implemented between a ground and a node between the first and second global compensation resistances. The global off-capacitance of the global bypass switching transistor can result in a phase lead change, and the global phase compensation circuit can be configured to provide a phase lag change to compensate for the phase lead change. The first and second global compensation resistances can have substantially the same value.

[0015] In some embodiments, the phase lead change can be by an amount calculated as $\phi = \tan^{-1}(2\omega R_{G1} C_{off}) - \tan^{-1}\left(\frac{2}{3}\omega R_{G1} C_{off}\right)$, and the phase lag change can be by an amount calculated as $\phi = -\tan^{-1}\left(\frac{2}{3}\omega R_{G1} C_G\right)$, where ω is 2π times frequency, R_L is load impedance, R_{G1} is the first global compensation resistance, and C_G is the global compensation capacitance. The values of the first global compensation resistance and the global compensation

capacitance can be selected such that magnitude of the phase lag change is substantially the same as magnitude of the phase lead change. The value of the global compensation capacitance can be selected such that a global gain of the attenuator circuit is approximately flat over a selected frequency range.

[0016] In a second aspect, the present disclosure provides a semiconductor die having a radio-frequency circuit, the semiconductor die comprising: a semiconductor substrate; and an attenuator circuit implemented on the semiconductor substrate, the attenuator circuit including a plurality of attenuation blocks arranged in series between an input node and an output node, each of the plurality of attenuation blocks including a bypass path, the attenuator circuit further including a phase compensation circuit implemented for each of at least some of the attenuation blocks having the respective bypass paths, the phase compensation circuit configured to compensate for an off-capacitance effect associated with the corresponding bypass path, at least one of the attenuation blocks being without a phase compensation circuit and the at least one attenuation block without the phase compensation circuit including an attenuation block having a lowest attenuation value.

[0017] In a third aspect, the present disclosure provides a radio-frequency module comprising: a packaging substrate configured to receive a plurality of components; and a radio-frequency attenuator circuit implemented on the packaging substrate, the attenuator circuit including a plurality of attenuation blocks arranged in series between an input node and an output node, each of the plurality of attenuation blocks including a bypass path the attenuator circuit further including a phase compensation circuit implemented for each of at least some of the attenuation blocks having the respective bypass paths, the phase compensation circuit configured to compensate for an off-capacitance effect associated with the corresponding bypass path, at least one of the attenuation blocks being without a phase compensation circuit, and the at least one attenuation block without the phase compensation circuit including an attenuation block having a lowest attenuation value.

[0018] In some embodiments, some or all of the radio-frequency attenuator circuit can be implemented on a semiconductor die. In some

embodiments, substantially all of the radio-frequency attenuator circuit can be implemented on the semiconductor die.

[0019] In some embodiments, the radio-frequency module can be configured to process a received radio-frequency signal. The radio-frequency module can be, for example, a diversity receive module.

[0020] In some embodiments, the radio-frequency module can further include a controller in communication with the radio-frequency attenuator circuit and configured to provide a control signal for operation of the radio-frequency

attenuator circuit. The controller can be configured to provide, for example, a Mobile Industry Processor Interface control signal.

[0021] In a fourth aspect, the present disclosure provides a wireless device comprising: an antenna configured to receive a radio-frequency signal; a transceiver in communication with the antenna; and a signal path between the antenna and the transceiver; and a radio-frequency attenuator circuit implemented along the signal path, the attenuator circuit including a plurality of attenuation blocks arranged in series between an input node and an output node, each of the plurality of attenuation blocks including a bypass path, the attenuator circuit further including a phase compensation circuit implemented for each of at least some of the attenuation blocks having the respective bypass paths, the phase compensation circuit is configured to compensate for an off-capacitance effect associated with the corresponding bypass path, at least one of the attenuation blocks being without a phase compensation circuit and the at least one attenuation block without the phase compensation circuit including an attenuation block having a lowest attenuation value.

[0022] In some embodiments, the wireless device can further include a controller in communication with the radio-frequency attenuator circuit and configured to provide a control signal for operation of the radio-frequency attenuator circuit. The controller can be configured to provide, for example, a Mobile Industry Processor Interface control signal.

[0023] In some implementations, the present disclosure relates to a signal attenuator circuit that includes a plurality of local binary-weighted attenuation blocks arranged in series between an input node and an output node, with each attenuation block including a local bypass path. The signal attenuator circuit can further include a global bypass path implemented between the input node and the output node, and a local phase compensation circuit associated with at least one of the one or more local attenuation blocks. The local phase compensation circuit is configured to compensate for an off-capacitance effect associated with the respective local bypass path.

[0023a] In a fifth aspect, the present disclosure provides a signal attenuator circuit comprising: A signal attenuator circuit comprising: a plurality of attenuation blocks arranged in series between an input node and an output node, each attenuation block including a local bypass path; a global bypass path implemented between the input node and the output node; and a local phase compensation circuit associated with at least one of the plurality of attenuation blocks, the local phase compensation circuit configured to compensate for an off-capacitance effect associated with the respective local bypass path, at least one of the attenuation blocks being without a phase compensation circuit and the at least one attenuation block without the phase compensation circuit including an attenuation block having a lowest attenuation value.

[0024] In some embodiments, the signal attenuator circuit can further include a global phase compensation circuit configured to compensate for an off-capacitance effect associated with the global bypass path.

[0025] In some implementations, the present disclosure relates to a semiconductor die that includes a semiconductor substrate, and a signal attenuator circuit implemented on the semiconductor substrate. The signal

attenuator circuit includes a plurality of local binary-weighted attenuation blocks arranged in series between an input node and an output node, with each attenuation block including a local bypass path. The signal attenuator circuit further includes a global bypass path implemented between the input node and the output node, and a local phase compensation circuit associated with at least one of the one or more local attenuation blocks. The local phase compensation circuit is configured to compensate for an off-capacitance effect associated with the respective local bypass path.

[0025a] In a sixth aspect, the present disclosure provides a semiconductor die comprising: a semiconductor substrate; and a signal attenuator circuit implemented on the semiconductor substrate, and including a plurality of attenuation blocks arranged in series between an input node and an output node, each attenuation block including a local bypass path, the signal attenuator circuit further including a global bypass path implemented between the input node and the output node, and a local phase compensation circuit associated with at least one of the plurality of attenuation blocks, the local phase compensation circuit configured to compensate for an off-capacitance effect associated with the respective local bypass path, at least one of the attenuation blocks being without a phase compensation circuit and the at least one attenuation block without the phase compensation circuit including an attenuation block having a lowest attenuation value.

[0026] In some implementations, the present disclosure relates to a radio-frequency module that includes a packaging substrate configured to receive a plurality of components, and a signal attenuator circuit implemented on the packaging substrate. The signal attenuator circuit further includes a plurality of local binary-weighted attenuation blocks arranged in series between an input node and an output node, with each attenuation block including a local bypass path. The signal attenuator circuit further includes a global bypass path implemented between the input node and the output node, and a local phase compensation circuit associated at least one of the one or more local attenuation blocks. The local phase compensation circuit is configured to compensate for an off-capacitance effect associated with the respective local bypass path.

[0026a] In a seventh aspect, the present disclosure provides a radio-frequency module comprising: a packaging substrate configured to receive a plurality of components; and a signal attenuator circuit implemented on the packaging substrate, and including a plurality of attenuation blocks arranged in series between an input node and an output node, each attenuation block including a local bypass path, the signal attenuator circuit further including a global bypass path implemented between the input node and the output node, and a local phase compensation circuit associated with at least one of the plurality of attenuation blocks, the local phase compensation circuit configured to compensate for an off-capacitance effect associated with the respective local bypass path, at least one of the attenuation blocks being without a phase compensation circuit and the at least one attenuation block without the phase compensation circuit including an attenuation block having a lowest attenuation value.

[0027] In some implementations, the present disclosure relates to a wireless device that includes an antenna configured to receive a radio-frequency signal, a transceiver in communication with the antenna, and a signal path between the antenna and the transceiver. The wireless device further includes a signal attenuator circuit implemented along the signal path, and includes a plurality of local binary-weighted attenuation blocks arranged in series between an input node and an output node, with each attenuation block including a local bypass path. The signal attenuator circuit further includes a global bypass path implemented between the input node and the output node, and a local phase compensation circuit associated with at least one of the one or more local attenuation blocks. The local phase compensation circuit is configured to compensate for an off-capacitance effect associated with the respective local bypass path.

[0027a] In an eighth aspect, the present disclosure provides a wireless device comprising: an antenna configured to receive a radio-frequency signal; a transceiver in communication with the antenna; a signal path between the antenna and the transceiver; and a signal attenuator circuit implemented along the signal path, and including a plurality of attenuation blocks arranged in series between an input node and an output node, each attenuation block including a

local bypass path, the signal attenuator circuit further including a global bypass path implemented between the input node and the output node, and a local phase compensation circuit associated with at least one of the plurality of local attenuation blocks, the local phase compensation circuit configured to compensate for an off-capacitance effect associated with the respective local bypass path, at least one of the attenuation blocks being without a phase compensation circuit and the at least one attenuation block without the phase compensation circuit including an attenuation block having a lowest attenuation value.

[0028] For purposes of summarizing the disclosure, certain aspects, advantages and novel features of the inventions have been described herein. It

is to be understood that not necessarily all such advantages may be achieved in accordance with any particular embodiment of the invention. Thus, the invention may be embodied or carried out in a manner that achieves or optimizes one advantage or group of advantages as taught herein without necessarily achieving other advantages as may be taught or suggested herein.

BRIEF DESCRIPTION OF THE DRAWINGS

[0029] Figure 1 depicts an attenuator circuit configured to receive a signal at an input node and generate an attenuated signal at an output node.

[0030] Figure 2 shows a block diagram of an attenuation circuit having a plurality of attenuation blocks implemented in a binary-weighted configuration.

[0031] Figure 3 shows an attenuation circuit that can be a more specific example of the attenuation circuit of Figure 2.

[0032] Figure 4 shows the fourth attenuation block of Figure 3 by itself.

[0033] Figure 5 shows a circuit representation of the example attenuation block of Figure 4, in which the various switching transistors are represented as either off-capacitance(s) or on-resistance(s).

[0034] Figure 6 shows an individual attenuation block that can represent each of the second and third attenuation blocks of Figure 3.

[0035] Figure 7 shows a circuit representation of the example attenuation block of Figure 6, in which the various switching transistors are represented as either off-capacitance(s) or on-resistance(s).

[0036] Figure 8A shows an operating mode for the attenuation circuit of Figure 3, in which each attenuation block is being bypassed, to provide a total attenuation of approximately 0dB.

[0037] Figure 8B shows an operating mode for the attenuation circuit of Figure 3, in which attenuation is being provided by the first attenuation block, and each of the second to fourth attenuation blocks is being bypassed, to provide a total attenuation of approximately 1dB.

[0038] Figure 8C shows an operating mode for the attenuation circuit of Figure 3, in which attenuation is being provided by the second attenuation block, and each of the first, third and fourth attenuation blocks is being bypassed, to provide a total attenuation of approximately 2dB.

[0039] Figure 8D shows an operating mode for the attenuation circuit of Figure 3, in which attenuation is being provided by each of the first and second attenuation blocks, and each of the third and fourth attenuation blocks is being bypassed, to provide a total attenuation of approximately 3dB.

[0040] Figure 8E shows an operating mode for the attenuation circuit of Figure 3, in which attenuation is being provided by each of the second to fourth attenuation blocks, and the first attenuation block is being bypassed, to provide a total attenuation of approximately 14dB.

[0041] Figure 8F shows an operating mode for the attenuation circuit of Figure 3, in which attenuation is being provided by each of the four attenuation blocks, to provide a total attenuation of approximately 15dB.

[0042] Figure 9A shows a compensation path that includes a local compensation capacitance.

[0043] Figure 9B shows that in some embodiments, the capacitance of Figure 9A can be implemented as a transistor device configured to provide a desired capacitance value.

[0044] Figure 10 shows that in some embodiments, an attenuation circuit having one or more features as described herein can be controlled by a controller.

[0045] Figure 11 shows that in some embodiments, some or all of an attenuation circuit having one or more features as described herein can be implemented on a semiconductor die.

[0046] Figure 12 shows an example where some or all of an attenuation circuit having one or more features as described herein can be implemented on a packaged module, and such a packaged module can include a semiconductor die similar to the example of Figure 11.

[0047] Figure 13 shows another example where some or all of an attenuation circuit having one or more features as described herein can be implemented on a packaged module, and such a packaged module can include a plurality of semiconductor die.

[0048] Figure 14 shows non-limiting examples of how an attenuator having one or more features as described herein can be implemented in a radio-frequency system.

[0049] Figure 15 shows an example of a diversity receive module that includes an attenuator having one or more features as described herein.

[0050] Figure 16 depicts an example wireless device having one or more advantageous features described herein.

DETAILED DESCRIPTION OF SOME EMBODIMENTS

[0051] The headings provided herein, if any, are for convenience only and do not necessarily affect the scope or meaning of the claimed invention.

[0052] Disclosed herein are various examples of circuits, devices and methods related to attenuators that can be utilized in, for example, radio-frequency (RF) applications. Although various examples are described herein in the context of RF applications, it will be understood that such circuits, devices and methods related to attenuators can be utilized in other electronic applications.

[0053] Figure 1 depicts an attenuator circuit 100 configured to receive an RF signal at an input node (IN) and generate an attenuated RF signal at an output node (OUT). Such an attenuator circuit can include one or more features as described herein so as to provide desirable functionalities such as phase shift compensation, gain compensation, and/or low loss bypass capability. As described herein, such phase compensation can provide, for example, an approximately zero phase shift resulting from an attenuation block and/or the attenuator circuit itself. As also described herein, such gain compensation can provide, for example, an approximately flat gain over a frequency range.

[0054] It is noted that phase variation and gain slope are generally not desired when an input signal passes through an attenuator, since such effects can cause performance degradation in a communication link. In some embodiments, the attenuation circuit 100 of Figure 1 can include a local compensation scheme to address the phase variation problem. In some embodiments, such an attenuation circuit can also include a global compensation scheme to address the phase variation problem. As described herein, such compensation schemes can be configured to address sources of such phase variations. As also described herein, such compensation schemes can also provide an approximately flat gain over a relatively wide frequency range. As

also described herein, such compensation schemes can also provide a bypass path having relatively low loss which is desirable for keeping signal attenuation to a minimum under some situations (e.g., when an attenuation path is not being used).

[0055] For the purpose of description, an attenuation circuit can also be referred to as an attenuator assembly or simply an attenuator. Description of such an attenuation circuit, attenuator assembly, attenuator, etc. can apply to one or more attenuation blocks (also referred to herein as local attenuation), overall attenuation circuit (also referred to herein as global attenuation), or any combination thereof.

[0056] Figure 2 shows a block diagram of an attenuation circuit 100 configured to receive an RF signal at its input node (IN) and provide an output RF signal at its output node (OUT). Such an output RF signal can be attenuated by one or more attenuation values, or be substantially the same as the input RF signal (e.g., through bypass functionality) when attenuation is not desired. Examples of how such attenuation values and bypass functionality can be implemented are described herein in greater detail. Also described herein are examples of how phase compensation can be implemented at a local attenuation level, at a global level, or any combination thereof.

[0057] In the example of Figure 2, a plurality of attenuation blocks are shown to be implemented in a binary-weighted configuration. For example, four attenuation blocks (102a, 102b, 102c, 102d) are shown to be arranged in series between the input (IN) and output (OUT) nodes, and are shown to provide 1dB, 2dB, 4dB, 8dB attenuations, respectively. By different combinations of such attenuations (and/or bypasses), the attenuation circuit 100 can provide a total attenuation of 0dB to 15dB in 1dB increments. Examples related to how such different total attenuations can be obtained are described herein in greater detail.

[0058] In the example of Figure 2, as well as in other examples based on Figure 2, four binary-weighted attenuation blocks are utilized. However, it will be understood that one or more features of the present disclosure can also be implemented in attenuation circuits having more or less numbers of attenuation blocks. For example, three attenuation blocks can be utilized to provide 0dB to 7dB attenuation values in 1dB increments. In another example, five attenuation

blocks can be utilized to provide 0dB to 31dB attenuation values in 1dB increments.

[0059] In the various examples described herein, a step attenuation value is assumed to be 1dB. However, it will be understood that such a step attenuation value can have a value other than 1dB. Accordingly, it will be understood that one or more features of the present disclosure can be implemented in an attenuation circuit having a plurality of attenuation blocks capable of providing attenuation values based on a binary-weighted scheme where an i-th attenuation block is capable of providing an attenuation of $A2^{i-1}$, where *A* is a step attenuation value (e.g., 0.5dB, 1dB, 2dB, etc.). For example, in the example of Figure 2, A = 1dB, such that the first attenuation block (i = 1) provides an attenuation of 1dB x 2^0 = 1dB; the second attenuation block (i = 2) provides an attenuation of 1dB x 2^1 = 2dB; and so on.

[0060] In another example, suppose that a finer granularity (e.g., 0.5dB) in attenuation is desired for a similar range of attenuation as in the example of Figure 2 (e.g. 0 to 15.5dB). In such an example, a first attenuation block (i = 1) can provide an attenuation of 0.5dB x 2^0 = 0.5dB, a second attenuation block (i = 2) can provide an attenuation of 0.5dB x 2^1 = 1.0dB, a third attenuation block (i = 3) can provide an attenuation of 0.5dB x 2^2 = 2.0dB, a fourth attenuation block (i = 4) can provide an attenuation of 0.5dB x 2^3 = 4.0dB, and a fifth attenuation block (i = 5) can provide an attenuation of 0.5dB x 2^4 = 8.0dB. With such five binary-weighted attenuation blocks, attenuations values can be provided from 0dB to 15.5dB in 0.5dB increments.

[0061] In the example of Figure 2, each of the attenuation blocks 102a, 102b, 102c, 102d is shown to include a respective phase compensation circuit (104a, 104b, 104c, 104d). Examples related to such phase compensation circuits are described herein in greater detail. In the example of Figure 2, all of the attenuation blocks are shown to have respective phase compensation circuits. However, it will be understood that in some embodiments, one or more attenuation blocks may or may not have such phase compensation circuit(s).

[0062] In the example of Figure 2, it will be understood that the attenuation blocks 102a, 102b, 102c, 102d may or may not have similar attenuation configurations. For example, one or more of the attenuation blocks can have a T-attenuation configuration, and one or more of the attenuation blocks

can have a pi-attenuation configuration. Thus, it will be understood that the attenuation circuit 100 of Figure 2 can include one or more types of attenuation configurations among the attenuation blocks. It will also be understood that other types of attenuation configurations can be implemented in one or more attenuation blocks.

[0063] Figure 3 shows an attenuation circuit 100 that can be a more specific example of the attenuation circuit 100 of Figure 2. In the example of Figure 3, each of three attenuation blocks 102a, 102b, 102c is shown to include a bridge-T-attenuator configuration and a corresponding bypass path (105a, 105b or 105c). For example, the first attenuation block 102a is shown to include resistances $R1_A$, $R1'_A$, $R2_A$, $R3_A$ arranged in a bridge-T-configuration. The resistances $R1_A$ and $R1'_A$ are shown to be in series and implemented between input and output nodes of the first attenuation block 102a. The resistance $R2_A$ is shown to be implemented between the input node and the output node so as to be electrically parallel with the series combination of $R1_A$ and $R1'_A$. The resistance $R3_A$ is shown to be implemented between ground and a node between $R1_A$ and $R1'_A$ (also referred to herein as a T-node).

[0064] Similarly, the second attenuation block 102b is shown to include resistances $R1_B$, $R1'_B$, $R2_B$, $R3_B$ arranged in a bridge-T-configuration. The resistances $R1_B$ and $R1'_B$ are shown to be in series and implemented between input and output nodes of the first attenuation block 102b. The resistance $R2_B$ is shown to be implemented between the input node and the output node so as to be electrically parallel with the series combination of $R1_B$ and $R1'_B$. The resistance $R3_B$ is shown to be implemented between ground and a node between $R1_B$ and $R1'_B$ (also referred to herein as a T-node).

[0065] Similarly, the third attenuation block 102c is shown to include resistances $R1_C$, $R1'_C$, $R2_C$, $R3_C$ arranged in a bridge-T-configuration. The resistances $R1_C$ and $R1'_C$ are shown to be in series and implemented between input and output nodes of the first attenuation block 102c. The resistance $R2_C$ is shown to be implemented between the input node and the output node so as to be electrically parallel with the series combination of $R1_C$ and $R1'_C$. The resistance $R3_C$ is shown to be implemented between ground and a node between $R1_C$ and $R1'_C$ (also referred to herein as a T-node).

[0066] In the example of Figure 3, the fourth attenuation block 102d is shown to include resistances $R1_D$, $R2_D$, $R3_D$ arranged in a pi-configuration. The resistance $R1_D$ is shown to be implemented between input and output nodes of the fourth attenuation block 102d. The resistance $R2_D$ is shown to be implemented between the input node and ground; similarly, the resistance $R3_D$ is shown to be implemented between the output node and ground.

[0067] In the bridge-T-configuration of each of the three attenuation blocks 102a, 102b, 102c of Figure 3, a switching FET ($M2_A$, $M2_B$ or $M2_C$) can be provided between the corresponding T-node and one end of the shunt resistance ($R3_A$, $R3_B$ or $R3_C$), with the other end of the shunt resistance being coupled to ground. Such a switching FET ($M2_A$, $M2_B$ or $M2_C$) can be turned ON when attenuation is enabled for the corresponding attenuation block, and be turned OFF when attenuation is bypassed through the corresponding bypass path (105a, 105b or 105c). Such a bypass path can include, for example, a corresponding switching FET ($M1_A$, $M1_B$ or $M1_C$) which can be turned OFF when attenuation is enabled for the corresponding attenuation block, and be turned ON when attenuation is bypassed through the bypass path.

[0068] In the pi-configuration of the fourth attenuation block 102d of Figure 3, a switching FET $M2_D$ can be provided between the input node and one end of the resistance $R2_D$, with the other end of the resistance $R2_D$ being coupled to ground. Similarly, a switching FET $M3_D$ can be provided between the output node and one end of the resistance $R3_D$, with the other end of the resistance $R3_D$ being coupled to ground. Such switching FETs ($M2_D$ and $M3_D$) can be turned ON when attenuation is enabled for the fourth attenuation block 102d, and be turned OFF when attenuation is bypassed through the bypass path 105d. Such a bypass path (105d) can include, for example, a switching FET $M1_D$ which can be turned OFF when attenuation is enabled for the fourth attenuation block 102d, and be turned ON when attenuation is bypassed through the bypass path 105d.

[0069] In the bridge-T-configuration of the second attenuation block 102b of Figure 3, a capacitance C2 can be provided so as to be electrically parallel with the resistance $R3_B$. As described herein, such a capacitance can be selected to compensate for phase-shifting that occurs when an RF signal is passed through the attenuation block. As also described herein, such a

capacitance can also allow the attenuation block to provide a desirably flat gain profile over a relatively wide frequency range.

[0070] Similarly, in the bridge-T-configuration of the third attenuation block 102c of Figure 3, a capacitance C4 can be provided so as to be electrically parallel with the resistance $R3_C$. As described herein, such a capacitance can be selected to compensate for phase-shifting that occurs when an RF signal is passed through the attenuation block. As also described herein, such a capacitance can also allow the attenuation block to provide a desirably flat gain profile over a relatively wide frequency range.

[0071] In the pi-configuration of the fourth attenuation block 102d of Figure 3, a capacitance C8 can be provided so as to be electrically parallel with the resistance $R2_D$. Similarly, a capacitance C8' can be provided so as to be electrically parallel with the resistance $R3_D$. As described herein, such capacitances can be selected to compensate for phase-shifting that occurs when an RF signal is passed through the attenuation block. As also described herein, such capacitances can also allow the attenuation block to provide a desirably flat gain profile over a relatively wide frequency range.

[0072] In the example of Figure 3, it is noted that the first attenuation block 102a does not include a compensation capacitance. In some embodiments, an attenuation block having a lower attenuation value may not result in a significant amount of phase shift; accordingly, a compensation circuit (e.g., a compensation capacitance) may or may not provide significant compensation benefit.

[0073] In the attenuation block 102b, the presence of the capacitance C2 in parallel with the resistance $R3_B$ allows phase compensation to be implemented as described herein. As also described herein, such phase compensation can also depend on the values of one or more resistances associated with the attenuation block 102b, as well as on-resistance value (Ron) of the switching transistor $M2_B$. Accordingly, it will be understood that a box indicated as 104b can include some or all of circuit elements of a respective phase compensation circuit, or includes some or all of circuit elements that can influence such phase compensation.

[0074] Similarly, in the attenuation block 102c, the presence of the capacitance C4 in parallel with the resistance $R3_C$ allows phase compensation to

be implemented as described herein. As also described herein, such phase compensation can also depend on the values of one or more resistances associated with the attenuation block 102c, as well as on-resistance value (Ron) of the switching transistor $M2_C$. Accordingly, it will be understood that a box indicated as 104c can include some or all of circuit elements of a respective phase compensation circuit, or includes some or all of circuit elements that can influence such phase compensation.

[0075] In the attenuation block 102d, the presence of the capacitances C8 and C8' in parallel with their respective resistances $R2_D$ and $R3_D$ allows phase compensation as described herein. As also described herein, such phase compensation can also depend on values of the resistances $R2_D$ and $R3_D$, as well as on-resistance values (Ron) of the switching transistors $M2_D$ and $M3_D$. Accordingly, it will be understood that a box indicated as 104d includes some or all of circuit elements of a phase compensation circuit, or includes some or all of circuit elements that can influence such phase compensation.

[0076] In the example of Figure 3, some or all of the various switching FETs can be implemented as, for example, silicon-on-insulator (SOI) devices. It will be understood that while such various switching FETs are depicted as being NFETs, one or more features of the present disclosure can also be implemented utilizing other types of FETs. It will also be understood that the various switches in the example of Figure 3 can also be implemented as other types of transistors, including non-FET transistors.

[0077] Figures 4 and 5 show an example of how phase compensation can be implemented for the attenuation block 102d of the example of Figure 3. Figures 6 and 7 show an example of how phase compensation can be implemented for each of the attenuation blocks 102b, 102c of the example of Figure 3.

[0078] Figure 4 shows the attenuation block 102d by itself, and such an attenuation block can represent the fourth attenuation block 102d of Figure 3. In the example of Figure 4, the attenuation block 102d is in its attenuation mode, such that an RF signal received at the local input node (IN) is attenuated and provided at the local output node (OUT). Accordingly, the bypass switching FET $M1_D$ of the bypass path 105d is OFF, and each of the switching FETs $M2_D$ and $M3_D$ of the circuit 104d is ON.

[0079] Figure 5 shows a circuit representation 120 of the example attenuation block 102d of Figure 4, in which the various switching FETs are represented as either off-capacitance(s) or on-resistance(s). For example, the OFF state of $M1_D$ is represented as an off-capacitance Coff, and the ON state of each of $M2_D$ and $M3_D$ is represented as an on-resistance Ron. For the purpose of description, it is assumed that the pi-attenuator configuration of Figure 4 is generally symmetric. Accordingly, $M2_D$ can be similar to $M3_D$, such that Ron of $M2_D$ is approximately the same as Ron of $M3_D$; hence, Figure 5 depicts each of $M2_D$ and $M3_D$ as Ron. Similarly, the resistances $R2_D$ and $R3_D$ in Figure 4 are assumed to be approximately the same; hence, Figure 5 depicts each of $R2_D$ and $R3_D$ as having a resistance R2. Similarly, the capacitances C8 and C8' in Figure 4 are assumed to be approximately the same; hence, Figure 5 depicts each of C8 and C8' as having a compensation capacitance of Cc.

[0080] In Figure 5, the circuit representation 120 is shown to have a source impedance Rs at the local input (IN), and a load impedance RL at the local output (OUT). Such impedance values may or may not be the same. For the purpose of description, however, values of Rs and RL are assumed to be the same at a characteristic impedance Z0 (e.g., at 50Ω).

[0081] With the foregoing assumption, values of R1 and R2 in the example of Figure 5 can be obtained as follows:

$$R_1 = \frac{Z_0}{2} \cdot \frac{K-1}{K+1} \qquad (1)$$

$$R_2 = Z_0 \cdot \frac{K+1}{K-1}. \qquad (2)$$

In Equations 1 and 2, the parameter K represents the attenuation value of the attenuation block 120. It is noted that as attenuation becomes larger, R1 generally increases, and R2 generally decreases.

[0082] Referring to Figure 5, and assuming that the on-resistance Ron of each of $M2_D$ and $M3_D$ is approximately zero, a portion of the attenuation block 120, indicated as Network 1, can contribute to forward gain and phase shift (e.g., phase lead) of the attenuation block 120 as:

$$\frac{V_{out}}{V_{in}} = \frac{R_L(1+sR_1C_{off})}{(R_L+R_1)+sR_LR_1C_{off}} \quad (3)$$

$$\phi = \tan^{-1}(\omega R_1 C_{off}) - \tan^{-1}\left(\omega \frac{R_1 R_L}{R_1+R_L} C_{off}\right). \quad (4)$$

[0083] In Figure 5, a portion of the attenuation block 120, indicated as Network 2, can contribute to forward gain and phase shift (e.g., phase lag) of the attenuation block 120 as:

$$\frac{V_{out}}{V_{in}} = \frac{R_2'}{(R_2'+R_1)+sR_2'R_1C_c} \quad (5)$$

$$\phi = -\tan^{-1}\left(\frac{\omega R_1 R_2' C_c}{R_1+R_2'}\right). \quad (6)$$

In Equations 3-6, $\omega = 2\pi f$, where *f* is frequency, and R_2' is a resistance value of parallel arrangement of R_2 and R_L.

[0084] Referring to Figures 4 and 5, and Equations 4 and 6, it is noted that the parameters $\omega, R_L, C_{off}, R_1 \; and \; R_2$ are typically set for a given frequency, characteristic impedance, switching FET configuration, and attenuation value. However, in some embodiments, the value of the compensation capacitance Cc can be adjusted such that the phase lag of Equation 6 compensates for the phase lead of Equation 4. Such phase compensation can allow the phase associated with the attenuation block 102d/120 of Figures 4 and 5 to be at or near a desired value. For example, the compensated phase associated with the attenuation block 102d/120 can have substantially the same phase variation as in a reference mode.

[0085] Referring to Figures 4 and 5, it is noted that since Coff is in parallel arrangement with R1, its impedance $1/(j\omega C_{off})$ will make an equivalent series impedance between the input and output nodes become smaller as frequency increases, resulting in less attenuation at a higher frequency. Inversely, higher attenuation can result at a lower frequency.

[0086] It is further noted that the compensation capacitance Cc is arranged parallel to the corresponding shunt resistance R2. Thus, the

impedance $(1/(j\omega C_c))$ of the compensation capacitance Cc will make an equivalent impedance of the shunt arm become less, resulting in more attenuation for the attenuation block. Thus, in some embodiments, the compensation capacitance Cc can be selected to compensate for the impact of Coff on gain, and thereby achieve a desired gain profile (e.g., approximately flat profile) for the attenuation block over a wide frequency range. In some embodiments, the compensation capacitance Cc can be selected to provide at least some phase compensation described herein, as well as to provide at least some gain compensation as described herein, for the attenuation block.

[0087] Figures 6 and 7 show an example of how phase compensation can be implemented for each of the attenuation blocks 102b, 102c of the example of Figure 3. Figure 6 shows an individual attenuation block 102, and such an attenuation block can represent each of the two example attenuation blocks 102b, 102c of Figure 3. Accordingly, reference numerals of the various elements of the attenuation block 102 are shown without subscripts.

[0088] In the example of Figure 6, the attenuation block 102 is in its attenuation mode, such that an RF signal received at the local input node (IN) is attenuated and provided at the local output node (OUT). Accordingly, the bypass switching FET M1 of the bypass path 105 is OFF, and the switching FET M2 of the circuit 104 is ON.

[0089] Figure 7 shows a circuit representation 130 of the example attenuation block 102 of Figure 6, in which the various switching FETs are represented as either off-capacitance(s) or on-resistance(s). For example, the OFF state of M1 is represented as an off-capacitance Coff, and the ON state of M2 is represented as an on-resistance Ron. For the purpose of description, it is assumed that the bridge-T-attenuator configuration of Figure 6 is generally symmetric. Accordingly, the resistances R1 and R1' in Figure 6 are assumed to be approximately the same; hence, Figure 7 depicts each of R1 and R1' as having a resistance R1. In Figure 7 the capacitance C2 of Figure 6 is assumed as having a compensation capacitance of Cc.

[0090] In Figure 7, the circuit representation 130 is shown to have a source impedance Rs at the local input (IN), and a load impedance RL at the local output (OUT). Such impedance values may or may not be the same. For the purpose of description, however, values of Rs and RL are assumed to be the

same at a characteristic impedance Z0 (e.g., at 50Ω). Further, the resistance R1 can be assumed to have the same characteristic impedance Z0 (e.g., at 50Ω).

[0091] With the foregoing assumption, values of R2 and R3 in the example of Figure 7 can be obtained as follows:

$$R_2 = R_1 \cdot (K - 1) \quad (7)$$

$$R_3 = \frac{R_1}{K-1}. \quad (8)$$

In Equations 7 and 8, the parameter K represents the attenuation value of the attenuation block 130. It is noted that as attenuation becomes larger, R2 generally increases, and R3 generally decreases.

[0092] Referring to Figure 7, and assuming that the on-resistance Ron of M2 is approximately zero, a portion of the attenuation block 130, indicated as Network 1, can contribute to forward gain and phase shift (e.g., phase lead) of the attenuation block 130 as:

$$\frac{V_{out}}{V_{in}} = \frac{1+sR_2C_{off}}{\left(1+\frac{R_2}{R_L}\right)+sR_2C_{off}} \quad (9)$$

$$\phi = \tan^{-1}(\omega R_2 C_{off}) - \tan^{-1}\left(\frac{\omega R_2 C_{off}}{1+\frac{R_2}{R_L}}\right). \quad (10)$$

[0093] In Figure 7, a portion of the attenuation block 130, indicated as Network 2, can contribute to forward gain and phase shift (e.g., phase lag) of the attenuation block 130 as:

$$\frac{V_{out}}{V_{in}} = \frac{0.5 \cdot R_3'}{(R_3'+R_1)+sR_3'R_1C_c} \quad (11)$$

$$\phi = -\tan^{-1}\left(\frac{\omega R_1 R_3' C_c}{R_1+R_3'}\right). \quad (12)$$

In Equations 9-12, $\omega = 2\pi f$, where *f* is frequency, and R_3' is a resistance value of parallel arrangement of R_3 and (R_1+R_L).

[0094] Referring to Figures 6 and 7, and Equations 10 and 12, it is noted that the parameters $\omega, R_L, C_{off}, R_1, R_2 \; and \; R_3$ are typically set for a given frequency, characteristic impedance, switching FET configuration, and attenuation value. However, in some embodiments, the value of the compensation capacitance Cc can be adjusted such that the phase lag of Equation 12 compensates for the phase lead of Equation 12. Such phase compensation can allow the phase associated with the attenuation block 102/130 of Figures 6 and 7 to be at or near a desired value. For example, the compensated phase associated with the attenuation block 102/130 can have substantially the same phase variation as in a reference mode.

[0095] Referring to Figures 6 and 7, it is noted that since Coff is in parallel arrangement with R2, its impedance $1/(j\omega C_{off})$ will make an equivalent series impedance between the input and output nodes become smaller as frequency increases, resulting in less attenuation at a higher frequency. Inversely, higher attenuation can result at a lower frequency.

[0096] It is further noted that the compensation capacitance Cc is arranged parallel to the corresponding shunt resistance R3. Thus, the impedance $(1/(j\omega C_c))$ of the compensation capacitance Cc will make an equivalent impedance of the shunt arm become less, resulting in more attenuation for the attenuation block. Thus, in some embodiments, the compensation capacitance Cc can be selected to compensate for the impact of Coff on gain, and thereby achieve a desired gain profile (e.g., approximately flat profile) for the attenuation block over a wide frequency range. In some embodiments, the compensation capacitance Cc can be selected to provide at least some phase compensation described herein, as well as to provide at least some gain compensation as described herein, for the attenuation block.

[0097] Figures 8A-8F show examples of different operating modes that can be implemented for the attenuation circuit 100 of Figure 3. In Figure 8A, the attenuation circuit 100 is shown to be in an overall bypass mode, such that the attenuation circuit 100 provides a total of approximately 0dB attenuation. In such a mode, each of the bypass switches $M1_A$, $M1_B$, $M1_C$, $M1_D$ is ON, and each of the

shunt switches $M2_A$, $M2_B$, $M2_C$, $M2_D$ (assuming $M2_D$ is substantially the same as $M3_D$ in Figure 3) is OFF. Accordingly, an RF signal is shown to be routed as indicated by path 140. In such a mode, the RF signal is generally not subjected to a Coff capacitance; thus, undesirable phase shifting generally does not occur.

[0098] In Figure 8B, the attenuation circuit 100 is shown to be in a mode to provide a total of approximately 1dB attenuation. In such a mode, the bypass switch $M1_A$ is OFF, and each of the remaining bypass switches $M1_B$, $M1_C$, $M1_D$ is ON. Further, the shunt switch $M2_A$ is ON, and each of the remaining shunt switches $M2_B$, $M2_C$, $M2_D$ is OFF. Accordingly, an RF signal is shown to be routed as indicated by path 142. In such a mode, the RF signal is generally subjected to only a Coff capacitance of the bypass switch $M1_A$; and as described herein, such a mode may or may not need phase compensation.

[0099] In Figure 8C, the attenuation circuit 100 is shown to be in a mode to provide a total of approximately 2dB attenuation. In such a mode, the bypass switch $M1_B$ is OFF, and each of the remaining bypass switches $M1_A$, $M1_C$, $M1_D$ is ON. Further, the shunt switch $M2_B$ is ON, and each of the remaining shunt switches $M2_A$, $M2_C$, $M2_D$ is OFF. Accordingly, an RF signal is shown to be routed as indicated by path 144. In such a mode, the RF signal is generally subjected to a Coff capacitance of the bypass switch $M1_B$; and as described herein, phase compensation can be implemented by providing an appropriate value for the capacitance C2.

[0100] In Figure 8D, the attenuation circuit 100 is shown to be in a mode to provide a total of approximately 3dB attenuation. In such a mode, each of the bypass switches $M1_A$, $M1_B$ is OFF, and each of the remaining bypass switches $M1_C$, $M1_D$ is ON. Further, each of the shunt switches $M2_A$, $M2_B$ is ON, and each of the remaining shunt switches $M2_C$, $M2_D$ is OFF. Accordingly, an RF signal is shown to be routed as indicated by path 146. In such a mode, the RF signal is generally subjected to a Coff capacitance of each of the bypass switches $M1_A$, $M1_B$; and as described herein, phase compensation can be implemented by providing an appropriate value for the capacitance C2.

[0101] Higher attenuation values can be provided in similar manners by incrementing in 1dB steps by different combinations of the binary-weighted attenuation blocks. Continuing such increase in attenuation, a total attenuation of approximately 14dB can be provided by the attenuation circuit 100, as shown in

Figure 8E. In such a mode, each of the bypass switches $M1_B$, $M1_C$, $M1_D$ is OFF, and the remaining bypass switch $M1_A$ is ON. Further, each of the shunt switches $M2_B$, $M2_C$, $M2_D$ is ON, and the remaining shunt switch $M2_A$ is OFF. Accordingly, an RF signal is shown to be routed as indicated by path 148. In such a mode, the RF signal is generally subjected to a Coff capacitance of each of the bypass switches $M1_B$, $M1_C$, $M1_D$; and as described herein, phase compensation can be implemented by providing appropriate values for the capacitances C2, C4, C8.

[0102] As shown in Figure 8F, a total attenuation of approximately 15dB can be provided by the attenuation circuit 100. In such a mode, each of the bypass switches $M1_A$, $M1_B$, $M1_C$, $M1_D$ is OFF, and each of the shunt switches $M2_A$, $M2_B$, $M2_C$, $M2_D$ is ON. Accordingly, an RF signal is shown to be routed as indicated by path 150. In such a mode, the RF signal is generally subjected to a Coff capacitance of each of the bypass switches $M1_A$, $M1_B$, $M1_C$, $M1_D$; and as described herein, phase compensation can be implemented by providing appropriate values for the capacitances C2, C4, C8.

[0103] As described herein, a compensation circuit (e.g., 104b, 104c, 104c in Figure 3) can include a compensation capacitance (e.g., C2, C4, C8 in Figure 3, and Cc in Figures 5 and 7). Figure 9A shows a compensation path 170 that includes such a local compensation capacitance (indicated as C). Such a compensation path is also shown to have a resistance R in parallel with C.

[0104] Figure 9B shows that in some embodiments, the capacitance C of Figure 9A can be implemented as a FET device 172 (e.g., as a MOSFET device) configured to provide a desired capacitance value of C. For example, source and drain of the FET device 172 can be connected to the two ends of the resistance R, and a gate of the FET device 172 can be grounded without a gate bias, such that the FET device 172 acts as a capacitance similar to that of C of Figure 9A.

[0105] When the compensation capacitance is implemented as in the example of Figure 9B, a number of desirable features can be achieved. For example, the compensation capacitance elements can be fabricated essentially together with the various FETs (e.g., bypass FETs $M1_B$, $M1_C$, $M1_D$ in Figure 3). In another example, and assuming the foregoing fabrication process commonality, the FET devices 172 acting as capacitances are affected by essentially the same process variations that affect the other FETS (including the

local bypass FETs $M1_B$, $M1_C$, $M1_D$). Accordingly, process independence can be achieved among, for example, the FET devices 172 and the other FETs.

[0106] Figure 10 shows that in some embodiments, an attenuation circuit 100 having one or more features as described herein can further include a global bypass path 106 and a global phase compensation circuit 108. Such a global bypass path can be activated by allowing an RF signal received at the input node (IN) to be routed to the output node (OUT) through the global bypass path 106. In such a global bypass mode, each of a first switch S1 between the input node and a first node 110 and a second switch S2 between a second node and the output node can be opened to generally isolate the binary weighted attenuation blocks (collectively indicated as 102) and one or more local phase compensation circuits therein (collectively indicated as 104).

[0107] When the attenuation circuit 100 is in an attenuation mode, the binary-weighted attenuation blocks 102 and their local phase compensation circuit(s) 104 therein can be operated as described herein, and the global bypass path 106 can be disabled. Thus, an RF signal received at the input node (IN) can be routed to the output node (OUT) through the closed first switch S1, the binary-weighted attenuation blocks 102, and the closed second switch S2. In such an attenuation mode, some or all of phase shift (e.g., phase lead) associated with the disabled global bypass path 106 can be compensated by the global phase compensation circuit 108. Additional details concerning such global bypass path and global phase compensation are described in U.S. Patent Application No. 15/687,475, entitled ATTENUATORS HAVING PHASE SHIFT AND GAIN COMPENSATION CIRCUITS, the disclosure of which is filed on even date herewith and hereby incorporated by reference herein in its entirety and to be considered part of the specification of the present application.

[0108] Figure 10 further shows that in some embodiments, an attenuation circuit 100 having one or more features as described herein can be controlled by a controller 180. Such a controller can provide various control signals to, for example, operate the various switches to achieve various attenuation modes (e.g., as in Figures 8A-8F). In some embodiments, the controller 180 can be configured to include MIPI (Mobile Industry Processor Interface) functionality.

[0109] Figure 11 shows that in some embodiments, some or all of an attenuation circuit 100 having one or more features as described herein can be implemented on a semiconductor die 200. Such a die can include a substrate 202, and at least some of a phase/gain compensation circuit 204 (e.g., phase compensation circuits 104a, 104b, 104c, 104d of Figure 3) can be implemented on the substrate 202. For example, some or all of compensation capacitances C2, C4, C8, C8' can be implemented as on-die capacitors.

[0110] Figures 12 and 13 show that in some embodiments, some or all of an attenuation circuit 100 having one or more features as described herein can be implemented on a packaged module 300. Such a module can include a packaging substrate 302 configured to receive a plurality of components such as one or more die and one or more passive components.

[0111] Figure 12 shows that in some embodiments, the packaged module 300 can include a semiconductor die 200 that is similar to the example of Figure 11. Accordingly, such a die can include some or all of the attenuation circuit 100, with at least some of a phase/gain compensation circuit 204 (e.g., phase compensation circuits 104a, 104b, 104c, 104d of Figure 3) being implemented on the die 200.

[0112] Figure 13 shows that in some embodiments, the packaged module 300 can include a first semiconductor die 210 having some of the attenuation circuit 100, while the rest of the attenuation circuit 100 is implemented on another die 212, outside of a die (e.g., on the packaging substrate 302), or any combination thereof. In such a configuration, some of a phase/gain compensation circuit 204 (e.g., phase compensation circuits 104a, 104b, 104c, 104d of Figure 3) can be implemented on the first die 210, and the rest of the phase/gain compensation circuit 204 can be implemented on another die 212, outside of a die (e.g., on the packaging substrate 302), or any combination thereof.

[0113] Figure 14 shows non-limiting examples of how an attenuator having one or more features as described herein can be implemented in an RF system 400. Such an RF system can include an antenna 402 configured to facilitate reception and/or transmission of RF signals. In the context of reception, an RF signal received by the antenna 402 can be filtered (e.g., by a band-pass filter 410) and passed through an attenuator 100 before being amplified by a low-

noise amplifier (LNA) 412. Such an LNA-amplified RF signal can be filtered (e.g., by a band-pass filter 414), passed through an attenuator 100, and routed to a mixer 440. The mixer 440 can operate with an oscillator (not shown) to yield an intermediate-frequency (IF) signal. Such an IF signal can be filtered (e.g., by a band-pass filter 442) and passed through an attenuator 100 before being routed to an intermediate-frequency (IF) amplifier 416. Some or all of the foregoing attenuators 100 along the receive path can include one or more features as described herein.

[0114] In the context of transmission, an IF signal can be provided to an IF amplifier 420. An output of the IF amplifier 420 can be filtered (e.g., by a band-pass filter 444) and passed through an attenuator 100 before being routed to a mixer 446. The mixer 446 can operate with an oscillator (not shown) to yield an RF signal. Such an RF signal can be filtered (e.g., by a band-pass filter 422) and passed through an attenuator 100 before being routed to a power amplifier (PA) 424. The PA-amplified RF signal can be routed to the antenna 402 through an attenuator 100 and a filter (e.g., a band-pass filter 426) for transmission. Some or all of the foregoing attenuators 100 along the transmit path can include one or more features as described herein.

[0115] In some embodiments, various operations associated with the RF system 400 can be controlled and/or facilitated by a system controller 430. Such a system controller can include, for example, a processor 432 and a storage medium such as a non-transient computer-readable medium (CRM) 434. In some embodiments, at least some control functionalities associated with the operation of one or more attenuators 100 in the RF system 400 can be performed by the system controller 430.

[0116] In some embodiments, an attenuation circuit having one or more features as described herein can be implemented along a receive (Rx) chain. For example, a diversity receive (DRx) module can be implemented such that processing of a received signal can be achieved close to a diversity antenna. Figure 15 shows an example of such a DRx module.

[0117] In Figure 15, a diversity receiver module 300 can be an example of the modules 300 of Figures 12 and 13. In some embodiments, such a DRx module can be coupled to an off-module filter 513. The DRx module 300 can include a packaging substrate 501 configured to receive a plurality of

components and a receiving system implemented on the packaging substrate 501. The DRx module 300 can include one or more signal paths that are routed off the DRx module 300 and made available to a system integrator, designer, or manufacturer to support a filter for any desired band.

[0118] The DRx module 300 of Figure 15 is shown to include a number of paths between the input and the output of the DRx module 300. The DRx module 300 is also shown to include a bypass path between the input and the output activated by a bypass switch 519 controlled by the DRx controller 502. Although Figure 15 depicts a single bypass switch 519, in some implementations, the bypass switch 519 may include multiple switches (e.g., a first switch disposed physically close to the input and a second switch disposed physically close to the output. As shown in Figure 15, the bypass path does not include a filter or an amplifier.

[0119] The DRx module 300 is shown to include a number of multiplexer paths including a first multiplexer 511 and a second multiplexer 512. The multiplexer paths include a number of on-module paths that include the first multiplexer 511, a bandpass filter 613a-613d implemented on the packaging substrate 501, an amplifier 614a-614d implemented on the packaging substrate 501, and the second multiplexer 512. The multiplexer paths include one or more off-module paths that include the first multiplexer 511, a bandpass filter 513 implemented off the packaging substrate 501, an amplifier 514, and the second multiplexer 512. The amplifier 514 may be a wide-band amplifier implemented on the packaging substrate 501 or may also be implemented off the packaging substrate 501. In some embodiments, the amplifiers 614a-614d, 514 may be variable-gain amplifiers and/or variable-current amplifiers.

[0120] A DRx controller 502 can be configured to selectively activate one or more of the plurality of paths between the input and the output. In some implementations, the DRx controller 502 can be configured to selectively activate one or more of the plurality of paths based on a band select signal received by the DRx controller 502 (e.g., from a communications controller). The DRx controller 502 may selectively activate the paths by, for example, opening or closing the bypass switch 519, enabling or disabling the amplifiers 614a-614d, 514, controlling the multiplexers 511, 512, or through other mechanisms. For example, the DRx controller 502 may open or close switches along the paths

(e.g., between the filters 613a-613d, 513 and the amplifiers 614a-614d, 514) or by setting the gain of the amplifiers 614a-614d, 514 to substantially zero.

[0121] In the example DRx module 300 of Figure 15, some or all of the amplifiers 614a-614d, 514 can be provided with an attenuation circuit 100 having one or more features as described herein. For example, each of such amplifiers is shown to have an attenuation circuit 100 implemented on its input side. In some embodiments, a given amplifier can have an attenuation circuit on its input side and/or on its output side.

[0122] In some implementations, an architecture, device and/or circuit having one or more features described herein can be included in an RF device such as a wireless device. Such an architecture, device and/or circuit can be implemented directly in the wireless device, in one or more modular forms as described herein, or in some combination thereof. In some embodiments, such a wireless device can include, for example, a cellular phone, a smart-phone, a hand-held wireless device with or without phone functionality, a wireless tablet, a wireless router, a wireless access point, a wireless base station, etc. Although described in the context of wireless devices, it will be understood that one or more features of the present disclosure can also be implemented in other RF systems such as base stations.

[0123] Figure 16 depicts an example wireless device 700 having one or more advantageous features described herein. As described in reference to Figures 14 and 15, one or more attenuators having one or more features as described herein can be implemented in a number of places in such a wireless device. For example, in some embodiments, such advantageous features can be implemented in a module such as a diversity receive (DRx) module 300 having one or more low-noise amplifiers (LNAs). Such a DRx module can be configured as described herein in reference to Figures 12, 13 and 15. In some embodiments, an attenuator having one or more features as described herein can be implemented along an RF signal path before and/or after an LNA.

[0124] In the example of Figure 16, power amplifiers (PAs) in a PA module 712 can receive their respective RF signals from a transceiver 710 that can be configured and operated to generate RF signals to be amplified and transmitted, and to process received signals. The transceiver 710 is shown to interact with a baseband sub-system 708 that is configured to provide conversion

between data and/or voice signals suitable for a user and RF signals suitable for the transceiver 710. The transceiver 710 is also shown to be connected to a power management component 706 that is configured to manage power for the operation of the wireless device 700. Such power management can also control operations of the baseband sub-system 708 and other components of the wireless device 700.

[0125] The baseband sub-system 708 is shown to be connected to a user interface 702 to facilitate various input and output of voice and/or data provided to and received from the user. The baseband sub-system 708 can also be connected to a memory 704 that is configured to store data and/or instructions to facilitate the operation of the wireless device, and/or to provide storage of information for the user.

[0126] In the example of Figure 16, the DRx module 300 can be implemented between one or more diversity antennas (e.g., diversity antenna 730) and the ASM 714. Such a configuration can allow an RF signal received through the diversity antenna 730 to be processed (in some embodiments, including amplification by an LNA) with little or no loss of and/or little or no addition of noise to the RF signal from the diversity antenna 730. Such processed signal from the DRx module 300 can then be routed to the ASM through one or more signal paths.

[0127] In the example of Figure 16, a main antenna 720 can be configured to, for example, facilitate transmission of RF signals from the PA module 712. In some embodiments, receive operations can also be achieved through the main antenna.

[0128] A number of other wireless device configurations can utilize one or more features described herein. For example, a wireless device does not need to be a multi-band device. In another example, a wireless device can include additional antennas such as diversity antenna, and additional connectivity features such as Wi-Fi, Bluetooth, and GPS.

[0129] Unless the context clearly requires otherwise, throughout the description and the claims, the words “comprise,” “comprising,” and the like are to be construed in an inclusive sense, as opposed to an exclusive or exhaustive sense; that is to say, in the sense of “including, but not limited to.” The word

"coupled", as generally used herein, refers to two or more elements that may be either directly connected, or connected by way of one or more intermediate elements. Additionally, the words "herein," "above," "below," and words of similar import, when used in this application, shall refer to this application as a whole and not to any particular portions of this application. Where the context permits, words in the above Detailed Description using the singular or plural number may also include the plural or singular number respectively. The word "or" in reference to a list of two or more items, that word covers all of the following interpretations of the word: any of the items in the list, all of the items in the list, and any combination of the items in the list.

[0130] The above detailed description of embodiments of the invention is not intended to be exhaustive or to limit the invention to the precise form disclosed above. While specific embodiments of, and examples for, the invention are described above for illustrative purposes, various equivalent modifications are possible within the scope of the invention, as those skilled in the relevant art will recognize. For example, while processes or blocks are presented in a given order, alternative embodiments may perform routines having steps, or employ systems having blocks, in a different order, and some processes or blocks may be deleted, moved, added, subdivided, combined, and/or modified. Each of these processes or blocks may be implemented in a variety of different ways. Also, while processes or blocks are at times shown as being performed in series, these processes or blocks may instead be performed in parallel, or may be performed at different times.

[0131] The teachings of the invention provided herein can be applied to other systems, not necessarily the system described above. The elements and acts of the various embodiments described above can be combined to provide further embodiments.

[0132] While some embodiments of the inventions have been described, these embodiments have been presented by way of example only, and are not intended to limit the scope of the disclosure. Indeed, the novel methods and systems described herein may be embodied in a variety of other forms; furthermore, various omissions, substitutions and changes in the form of the methods and systems described herein may be made without departing from the spirit of the disclosure. The accompanying claims and their equivalents are

intended to cover such forms or modifications as would fall within the scope and spirit of the disclosure.

WHAT IS CLAIMED IS:

1. A radio-frequency attenuator circuit comprising:

a plurality of attenuation blocks arranged in series between an input node and an output node, each of the plurality of attenuation blocks including a bypass path; and

a phase compensation circuit implemented for each of at least some of the attenuation blocks having the respective bypass paths, the phase compensation circuit configured to compensate for an off-capacitance effect associated with the corresponding bypass path, at least one of the attenuation blocks being without a phase compensation circuit, and the at least one attenuation block without the phase compensation circuit including an attenuation block having a lowest attenuation value.

2. The attenuator circuit of claim 1 wherein the attenuation blocks have binary-weighted attenuation values.

3. The attenuator circuit of claim 2 wherein the binary-weighted attenuation values include N values, with an i-th value being $A2^{i-1}$, where *A* is a step attenuation value and i is a positive integer from 1 to N.

4. The attenuator circuit of claim 3 wherein the step attenuation value A is approximately 1dB.

5. The attenuator circuit of claim 3 wherein the quantity N includes 2, 3, 4, 5, 6, 7 or 8.

6. The attenuator circuit of claim 1 wherein at least one of the attenuation blocks is configured as a pi-attenuator.

7. The attenuator circuit of claim 6 wherein the at least one attenuation block having the pi-attenuator includes an attenuation block having a highest attenuation value.

8. The attenuator circuit of claim 6 wherein the bypass path of the attenuation block having the pi-attenuator includes a bypass switching transistor configured to be on when the attenuation block is in a bypass mode and off when in an attenuation mode, such that the bypass switching transistor provides an off-capacitance when in the attenuation mode.

9. The attenuator circuit of claim 8 wherein the phase compensation circuit of the attenuation block having the pi-attenuator includes a phase compensation circuit configured to compensate for the off-capacitance when the attenuator block is in the attenuation mode.

10. The attenuator circuit of claim 9 wherein the pi-attenuator includes a resistance, a first shunt path implemented between one end of the resistance and a ground, a second shunt path implemented between the other end of the resistance and the ground, each of the first and second shunt paths including a shunt resistance.

11. The attenuator circuit of claim 10 wherein the phase compensation circuit associated with the pi-attenuator includes a first compensation capacitance arranged to be electrically parallel with the first shunt resistance, and a second compensation capacitance arranged to be electrically parallel with the second shunt resistance.

12. The attenuator circuit of claim 11 wherein the off-capacitance of the bypass switching transistor results in a phase lead change, and the phase compensation circuit is configured to provide a phase lag change to compensate for the phase lead change.

13. The attenuator circuit of claim 12 wherein the first and second shunt resistances have substantially the same value, and the first and second compensation capacitances have substantially the same value.

14. The attenuator circuit of claim 13 wherein the phase lead change is by an amount calculated as $\phi = \tan^{-1}(\omega R_1 C_{off}) - \tan^{-1}\left(\omega \frac{R_1 R_L}{R_1 + R_L} C_{off}\right)$, and the phase lag change is by an amount calculated as $\phi = -\tan^{-1}\left(\frac{\omega R_1 R_2' C_c}{R_1 + R_2'}\right)$, where ω is 2π times frequency, R_L is load impedance, R_1 is the resistance, C_C is the first local compensation capacitance, , C_{off} is the off capacitance of the local bypass switching transistor of the pi-attenuator and R_2' is an equivalent resistance of a parallel arrangement of the first shunt resistance and the load impedance.

15. The attenuator circuit of claim 14 wherein the value of the first compensation capacitance is selected such that magnitude of the phase lag change is substantially the same as magnitude of the phase lead change.

16. The attenuator circuit of claim 14 wherein the value of the compensation capacitance is selected such that a gain of the attenuation block is approximately flat over a selected frequency range.

17. The attenuator circuit of claim 1 wherein at least one of the attenuation blocks is configured as a bridge-T-attenuator.

18. The attenuator circuit of claim 17 wherein the bypass path of the attenuation block having the bridge-T-attenuator includes a bypass switching transistor configured to be on when the attenuation block is in a bypass mode and off when in an attenuation mode, such that the bypass switching transistor provides an off-capacitance when in the attenuation mode.

19. The attenuator circuit of claim 18 wherein the phase compensation circuit of the attenuation block having the bridge-T-attenuator includes a phase compensation circuit configured to compensate for the off-capacitance when the attenuator block is in the attenuation mode.

20. The attenuator circuit of claim 19 wherein the bridge-T-attenuator includes two first resistances connected in series, a second resistance electrically parallel with the series combination of the two first resistances, and a shunt path implemented between a ground and a node between the two first resistances, the shunt path including a shunt resistance.

21. The attenuator circuit of claim 20 wherein the phase compensation circuit associated with the bridge-T-attenuator includes a compensation capacitance arranged to be electrically parallel with the shunt resistance.

22. The attenuator circuit of claim 21 wherein the off-capacitance of the bypass switching transistor results in a phase lead change, and the phase compensation circuit is configured to provide a phase lag change to compensate for the phase lead change.

23. The attenuator circuit of claim 22 wherein the phase lead change is by an amount calculated as $\phi = \tan^{-1}(\omega R_2 C_{off}) - \tan^{-1}\left(\frac{\omega R_2 C_{off}}{1+\frac{R_2}{R_L}}\right)$, and the phase lag change is by an amount calculated as $\phi = -\tan^{-1}\left(\frac{\omega R_1 R_3' C_c}{R_1+R_3'}\right)$, where ω is 2π times frequency, R_L is load impedance, R_1 is the first resistance, R_2 is the second resistance, C_C is the compensation capacitance, C_{off} is the off capacitance of the local bypass switching transistor of the bridge T-attenuator and R_3' is an equivalent resistance of a parallel arrangement of the shunt resistance and a series-combination of the first resistance and the load impedance.

24. The attenuator circuit of claim 23 wherein the value of the compensation capacitance is selected such that magnitude of the phase lag change is substantially the same as magnitude of the phase lead change.

25. The attenuator circuit of claim 23 wherein the value of the compensation capacitance is selected such that a gain of the attenuation block is approximately flat over a selected frequency range.

26. The attenuator circuit of claim 1 further comprising a global bypass path that includes a global bypass switching transistor configured to be on when in a global bypass mode and off when in a global attenuation mode, such that the global bypass switching transistor provides a global off-capacitance when in the global attenuation mode.

27. The attenuator circuit of claim 26 further comprising a global phase compensation circuit configured to compensate for the global off-capacitance when the attenuator circuit is in the global attenuation mode.

28. The attenuator circuit of claim 27 wherein the global phase compensation circuit includes a first global compensation resistance and a second global compensation resistance arranged in series between the input node and the output node, the global phase compensation circuit further including a global compensation capacitance implemented between a ground and a node between the first and second global compensation resistances.

29. The attenuator circuit of claim 28 wherein the global off-capacitance of the global bypass switching transistor results in a phase lead change, and the global phase compensation circuit is configured to provide a phase lag change to compensate for the phase lead change.

30. The attenuator circuit of claim 29 wherein the first and second global compensation resistances have substantially the same value.

31. A semiconductor die having a radio-frequency circuit, the semiconductor die comprising:

a semiconductor substrate; and

an attenuator circuit implemented on the semiconductor substrate, the attenuator circuit including a plurality of attenuation blocks arranged in series between an input node and an output node, each of the plurality of attenuation blocks including a bypass path, the attenuator circuit further including a phase compensation circuit implemented for each of at least some of the attenuation blocks having the respective bypass paths, the phase compensation circuit configured to compensate for an off-capacitance effect associated with the corresponding bypass path, at least one of the attenuation blocks being without a phase compensation circuit, and the at least one attenuation block without the phase compensation circuit including an attenuation block having a lowest attenuation value.

32. A radio-frequency module comprising:

a packaging substrate configured to receive a plurality of components; and

a radio-frequency attenuator circuit implemented on the packaging substrate, the attenuator circuit including a plurality of attenuation blocks arranged in series between an input node and an output node, each of the plurality of attenuation blocks including a bypass path, the attenuator circuit further including a phase compensation circuit implemented for each of at least some of the attenuation blocks having the respective bypass paths, the phase compensation circuit configured to compensate for an off-capacitance effect associated with the corresponding bypass path, at least one of the attenuation blocks being without a phase compensation circuit and the at least one attenuation block without the phase compensation circuit including an attenuation block having a lowest attenuation value.

33. The radio-frequency module of claim 32 wherein some or all of the radio-frequency attenuator circuit is implemented on a semiconductor die.

34. The radio-frequency module of claim 33 wherein substantially all of the radio-frequency attenuator circuit is implemented on the semiconductor die.

35. The radio-frequency module of claim 32 wherein the radio-frequency module is configured to process a received radio-frequency signal.

36. The radio-frequency module of claim 35 wherein the radio-frequency module is a diversity receive module.

37. The radio-frequency module of claim 32 further comprising a controller in communication with the radio-frequency attenuator circuit and configured to provide a control signal for operation of the radio-frequency attenuator circuit.

38. The radio-frequency module of claim 37 wherein the controller is configured to provide a Mobile Industry Processor Interface control signal.

39. A wireless device comprising:

an antenna configured to receive a radio-frequency signal;

a transceiver in communication with the antenna;

a signal path between the antenna and the transceiver; and

a radio-frequency attenuator circuit implemented along the signal path, the attenuator circuit including a plurality of attenuation blocks arranged in series between an input node and an output node, each of the plurality of attenuation blocks including a bypass path, the attenuator circuit further including a phase compensation circuit implemented for each of at least some of the attenuation blocks having the respective bypass paths, the phase compensation circuit configured to compensate for an off-capacitance effect associated with the corresponding bypass path, at least one of the attenuation blocks being without a phase compensation circuit and the at least one attenuation block without the phase compensation circuit including an attenuation block having a lowest attenuation value.

40. The wireless device of claim 39 further comprising a controller in communication with the radio-frequency attenuator circuit and configured to provide a control signal for operation of the radio-frequency attenuator circuit.

41. The wireless device of claim 40 wherein the controller is configured to provide a Mobile Industry Processor Interface control signal.

42. A signal attenuator circuit comprising:

a plurality of attenuation blocks arranged in series between an input node and an output node, each attenuation block including a local bypass path;

a global bypass path implemented between the input node and the output node; and

a local phase compensation circuit associated with at least one of the plurality of attenuation blocks, the local phase compensation circuit configured to compensate for an off-capacitance effect associated with the respective local bypass path, at least one of the attenuation blocks being without a phase compensation circuit and the at least one attenuation block without the phase compensation circuit including an attenuation block having a lowest attenuation value.

43. The signal attenuator circuit of claim 42 further comprising a global phase compensation circuit configured to compensate for an off-capacitance effect associated with the global bypass path.

44. A semiconductor die comprising:

a semiconductor substrate; and

a signal attenuator circuit implemented on the semiconductor substrate, and including a plurality of attenuation blocks arranged in series between an input node and an output node, each attenuation block including a local bypass path, the signal attenuator circuit further including a global bypass path implemented between the input node and the output node, and a local phase compensation circuit associated with at least one of the plurality of attenuation blocks, the local phase compensation circuit configured to compensate for an off-capacitance effect associated with the respective local bypass path, at least one of the attenuation blocks being without a phase compensation circuit and the at least one attenuation

block without the phase compensation circuit including an attenuation block having a lowest attenuation value.

45. A radio-frequency module comprising:

a packaging substrate configured to receive a plurality of components; and

a signal attenuator circuit implemented on the packaging substrate, and including a plurality of attenuation blocks arranged in series between an input node and an output node, each attenuation block including a local bypass path, the signal attenuator circuit further including a global bypass path implemented between the input node and the output node, and a local phase compensation circuit associated with at least one of the plurality of attenuation blocks, the local phase compensation circuit configured to compensate for an off-capacitance effect associated with the respective local bypass path, at least one of the attenuation blocks being without a phase compensation circuit and the at least one attenuation block without the phase compensation circuit including an attenuation block having a lowest attenuation value.

46. A wireless device comprising:

an antenna configured to receive a radio-frequency signal;

a transceiver in communication with the antenna;

a signal path between the antenna and the transceiver; and

a signal attenuator circuit implemented along the signal path, and including a plurality of attenuation blocks arranged in series between an input node and an output node, each attenuation block including a local bypass path, the signal attenuator circuit further including a global bypass path implemented between the input node and the output node, and a local phase compensation circuit associated with at least one of the plurality of local attenuation blocks, the local phase compensation circuit configured to compensate for an off-capacitance effect associated with the respective local bypass path, at least one of the attenuation blocks being without a phase compensation circuit and the at least one attenuation

block without the phase compensation circuit including an attenuation block having a lowest attenuation value.