DESCRIPTION

Title of Invention

CROSS-CURRENT SUPPRESSION CONTROL DEVICE FOR POWER CONVERSION CIRCUIT

Technical field

[0001]

The present invention relates to a cross current suppression control device for equalizing current duty of each inverter unit in a power conversion circuit in which the inverter units are connected in parallel to each other.

Background Art

In a power conversion device, a method may be used in which a plurality of inverter units are connected in parallel to each other in order to obtain large capacity. If such a method is used, it is not necessary to design an inverter unit which is only used in a large-capacity device. In contrast, a cross current is generated between respective inverter units and thus the current duty tends to vary. Consequently, the lifetime of a specific inverter unit is shortened, and, in the worst case, a switching element may be thermally damaged due to overcurrent or overheating.

[0002]

As a countermeasure therefor, a method is used in which

a cross current suppression reactor is connected to each inverter unit in the related art, but causes new problems such as increases in cost, a weight, and a loss. In order to solve the problems, a method of suppressing a cross current through control has been examined (for example, PTLs 1 to 4).

[0003]

Paragraphs [0011] to [0015] of PTL 1 disclose that a cross current is detected, and output current unbalance is suppressed by adjusting an ON-pulse width.

[0004]

Paragraphs [0009] and [0010] of PTL 2 disclose that, by magnetically coupling gate lines, operation timings of switching elements can be aligned with each other even in a case where there are differences between timings of gate signals.

[0005]

Paragraph [0020] of PTL 3 discloses a method in which a cross current is detected on the basis of a difference between a mean output current and each inverter unit output current, and an output voltage command value is corrected.

[0006]

Paragraph [0026] of PTL 4 discloses a method in which a variation in gate signals between the inverter units is corrected by delaying the gate signal, and thus output currents are equalized. In addition, paragraph [0052] thereof

discloses a method in which a cross current is detected, and when the cross current increases, abnormality is determined, and the inverter unit is stopped.

Citation List

Patent Literature

[0007]

[PTL 1] JP-A-10-94259

[PTL 2] JP-A-2009-148001

[PTL 3] JP-A-2000-060137

[PTL 4] JP-A-10-04673

[PTL 5] JP-A-2008-048569

[PTL 6] JP-A-2-7714

[PTL 7] JP-A-2006-288148

Summary of Invention

[0008]

The method disclosed in PTL 1 is a method of adjusting a pulse width by detecting a cross current. The pulse width is reduced by delaying rising of a pulse and by advancing falling thereof. However, this method cannot handle a case where, for example, rising and falling are required to be advanced without changing a pulse width since there is delay disturbance of a gate signal due to a physical configuration of a gate circuit or a characteristic error of a switching element, for example, a transmission path of the gate signal for driving inverter units on one side is long among the

inverter units which are connected in parallel to each other, or gate capacitance of the switching element is large, and thus there is a problem in which a cross current increases.

[0009]

The method disclosed in PTL 2 is a method in which the switching elements corresponding to the same arm of each of the parallel-connected inverter units are magnetically coupled to each other. In this method, timings of accumulating or releasing electric charge of the gate signals can be aligned between the magnetically coupled switching elements. However, in a case where gate capacitances are different from each other due to an individual difference of the switching elements, or gate voltage threshold values for turning on the switching elements are different from each other, there is a problem in that operation timings of the switching elements cannot be aligned with each other, and thus a cross current is generated.

[0010]

The method disclosed in PTL 3 is a method of correcting a voltage command value by detecting a cross current. Since this method is based on the use of a PWM type, if the voltage command value is corrected to a positive side, a pulse width of a gate signal can be increased, and if the voltage command value is corrected to a negative side, the pulse width can be reduced. However, in the same manner as in PTL 1, also in this method, it is difficult to advance or delay rising and falling

without changing a pulse width.

[0011]

The method disclosed in PTL 4 is a method in which rising and falling of the gate signal is separately adjusted. However, since a delay amount is not adjusted through detection of a cross current, the delay amount is required to be manually adjusted before an operation, and is thus required to be manually readjusted in a case where characteristics of the switching element vary due to a temperature change, deterioration over time, or the like.

[0012]

In addition, none of the above-described methods have a function of correcting deviations of voltage drop (a saturation voltage between a collector and an emitter) Vce(sat) or forward voltage drop Vf occurring when a current passes through the switching element, a deviation of a parasitic inductance component of the wiring, and the like. In a case where there is such disturbance, a cross current is generated and increases even if timings of gate signals can be perfectly adjusted between the inverter units. For this reason, it is necessary to select a rated switching element which withstands the occurrence of a cross current or to provide a rated cross current suppression reactor which withstands the occurrence of a cross current. Further, it is necessary to increase inductance of a reactor in order to suppress a cross current.

[0013]

As described above, in the power conversion device in which inverter units are connected in parallel to each other, an object of the invention is to suppress not only a cross current caused by a timing of a gate signal but also a cross current caused by delay disturbance of a gate signal, which is associated with a characteristic error of an individual switching element or a physical configuration such as a distance or a shape of a transmission circuit.

[0014]

The present invention is made by considering the problems of the related art, and according to an aspect of the invention, there is provided a cross current suppression control device which suppresses a cross current in a power conversion circuit in which inverter units are connected in parallel to a direct current voltage source including a switching element, the cross current suppression control device including: a gate delay command value calculation section that operates once at a half switching cycle so as to calculate a rising gate delay command value and a falling gate delay command value; a rising delay adding section that adds the rising gate delay command value to a gate command value or a voltage command value; and a falling delay adding section that adds the falling gate delay command value to the gate command value or the voltage command value, in which the rising delay adding section and the falling delay

adding section are provided for each phase of each inverter unit, in which the gate delay command value calculation block includes a proportional amplifier that multiplies a deviation between an inverter unit output current command value and an inverter unit output current detection value by a gain, the deviation being obtained as a cross current; an integral amplifier to which the cross current is input by a first switch which is turned on whenever each switching element is turned on or off and when a logical result of a sign of the inverter unit output current detection value and a sign of the gate command value is true; and a second switch that receives a signal from the integral amplifier and is turned on by the sign of the inverter unit output current detection value, and in which outputs from the proportional amplifier and the second switch are added together, and thus the rising gate delay command value and the falling gate delay command value are output.

[0015]

According to another aspect of the invention, there is provided a cross current suppression control device which suppresses a cross current in a power conversion circuit in which inverter units are connected in parallel to a direct current voltage source, the cross current suppression control device including: a gate delay command value calculation section that operates once at a half switching cycle so as to

calculate a rising gate delay command value and a falling gate delay command value; a rising delay adding section that adds the rising gate delay command value to a gate command value or a voltage command value; and a falling delay adding section that adds the falling gate delay command value to the gate command value or the voltage command value, in which the rising delay adding section and the falling delay adding section are provided for each phase of each inverter unit, in which the gate delay command value calculation block includes a proportional amplifier that multiplies a deviation between an inverter unit output current command value and an inverter unit output current detection value by a gain, the deviation being obtained as a cross current; an integral amplifier that is provided so as to correspond to each switching element and to which the cross current is input by a first switch which is operated by the sign of the inverter unit output current detection value; and a second switch that receives a signal from the integral amplifier and is operated by the sign of the inverter unit output current detection value, and in which outputs from the proportional amplifier and the integral amplifier are added together, and thus the rising gate delay command value and the falling gate delay command value are output.

[0016]

In addition, as an aspect, when an absolute value of the

cross current is equal to or smaller than a set value, the proportional amplifier outputs zero, and the integral amplifier stops being updated, and when the absolute value of the cross current is equal to or greater than the set value, a value obtained by subtracting the set value from the absolute value is input to the proportional amplifier and the integral amplifier.

[0017]

Further, as an aspect, the inverter unit output current command value is a value obtained by dividing an inverter output current detection value by the number of inverter units.

[0018]

Further, as another aspect, the inverter unit output current command value is an output current detection value of another certain inverter unit.

[0019]

Further, as another aspect, when the inverter unit output current detection value is equal to or smaller than a set value, the proportional amplifier outputs zero, and the integral amplifier stops being updated, when an absolute value of the inverter output current detection value is equal to or greater than the set value, a value obtained by subtracting the set value from the absolute value is input to the proportional amplifier and the integral amplifier, and proportional integral calculation is performed so that the deviation between

the inverter unit output current command value and the inverter unit output current detection value becomes zero, and a value obtained by adding a proportional integral calculation result and outputs from the proportional amplifier and the integral amplifier together is used as the gate delay command value.

[0020]

Further, as an aspect, effective values of the inverter unit output current command value and the inverter unit output current detection value are used for the proportional integral calculation.

[0021]

Further, as an aspect, absolute current mean values per cycle of a fundamental wave of the inverter unit output current command value and the inverter unit output current detection value are used for the proportional integral calculation.

[0022]

Further, as an aspect, when an absolute value of the inverter output current is smaller than a threshold value, the integral amplifier stops being updated.

[0023]

Further, as an aspect, the gate delay command value calculation block is operated at a peak of a carrier triangular wave.

[0024]

Further, as an aspect, the gate delay command value

calculation block is operated when the gate command value changes.

[0025]

Further, each of the inverter units is a multi-level inverter.

[0026]

Further, as an aspect, the integral amplifier stops being updated in a case where the number of times of switching is not one during a half cycle of the carrier triangular wave.

[0027]

In addition, a gate command is output without adding delay thereto when an initial value of the integral amplifier starts to be set during a test operation of the power conversion circuit, during the test operation of the power conversion circuit, in a state in which a switching element of an inverter unit which is out of a delay time measurement target is turned on, a pulse-ON command is output to a switching element of a delay time measurement target inverter unit, a closed circuit is formed of the two switching elements and a cross current suppression reactor, time after a gate signal is set to an ON state until a differentiation result of the inverter unit current detection value exceeds a threshold value and time after the gate signal is set to an OFF state until the differentiation result of the inverter unit current detection value is equal to or smaller than the threshold value are

measured in the delay time measurement target inverter unit, and the measured times are used as initial values of the integral amplifier, and when an operation state of the power conversion circuit is changed from the test operation to a normal operation, a value of the integral amplifier is reset, and the initial value is input to the integral amplifier.

[0028]

Further, during the test operation of the power conversion circuit, as a current detector used to detect an inverter unit current detection value, a current detector of a specific inverter unit is used in all inverter units.

[0029]

Further, during the test operation of the power conversion circuit, a direct current voltage of the inverter unit is set to be lower than during a normal operation when a delay time is measured.

[0030]

Further, during the test operation of the power conversion circuit, among switching elements other than the turned-on switching element of the delay time measurement target inverter unit, a positive side voltage of a gate driving circuit for a switching element of an inverter unit is lowered, and voltage drop of the switching element is set higher than during the normal operation.

[0031]

Further, a PWM carrier frequency is increased in a specific period after the power conversion circuit starts to operate or a total output current of the inverter units exceeds a current threshold value.

[0032]

According to the present invention, it is possible to suppress not only a cross current caused by a timing of a gate signal but also a cross current caused by delay disturbance of a gate signal, which is associated with a characteristic difference of an individual switching element or a physical configuration such as a distance or a shape of a transmission circuit, in a power conversion circuit in which inverter units are connected in parallel.

Brief Description of Drawings

[0033]

Fig. 1 is a circuit configuration diagram for each phase of a power conversion circuit in Embodiment 1.

Fig. 2 is a block diagram illustrating a cross current suppression control block in Embodiment 1.

Fig. 3 is a time chart illustrating each waveform in Embodiment 1.

Fig. 4 is a block diagram illustrating a cross current suppression control block in Embodiment 2.

Fig. 5 is a block diagram illustrating a cross current suppression control block in Embodiment 3.

Fig. 6 is a block diagram illustrating a cross current suppression control block in Embodiment 4.

Fig. 7 is a block diagram illustrating a cross current suppression control block in Embodiment 5.

Fig. 8 is a block diagram illustrating a cross current suppression control block in Embodiment 6.

Fig. 9 is a block diagram illustrating a cross current suppression control block in Embodiment 7.

Fig. 10 is a block diagram illustrating a cross current suppression control block in Embodiment 8.

Fig. 11 is a circuit configuration diagram for each phase of a power conversion circuit in Embodiment 9.

Fig. 12 is a block diagram illustrating a cross current suppression control block in Embodiment 9.

Fig. 13 is a time chart illustrating a carrier triangular wave and a voltage command value of a level inverter.

Fig. 14 is a circuit configuration diagram for each phase of a power conversion circuit in Embodiment 10.

Fig. 15 is a block diagram illustrating a cross current suppression control block in Embodiment 10.

Fig. 16 is a block diagram illustrating an initial value determination block in Embodiment 10.

Fig. 17 is a waveform diagram illustrating each signal used to obtain an initial value of an integral amplifier in Embodiment 10.

Fig. 18 is a waveform diagram illustrating each signal used to obtain an initial value of the integral amplifier in Embodiment 10.

Fig. 19 is a block diagram illustrating an initial value determination block in Embodiment 11.

Fig. 20 is a waveform diagram illustrating each signal used to obtain an initial value of the integral amplifier in Embodiment 11.

Fig. 21 is a circuit configuration diagram for each phase of a power conversion circuit in Embodiment 12.

Fig. 22 is a block diagram illustrating a precharge circuit control block in Embodiment 12.

Fig. 23 is a circuit configuration diagram illustrating a gate drive circuit in Embodiment 13.

Fig. 24 is a block diagram illustrating an initial value determination block in Embodiment 13.

Fig. 25 is a waveform diagram of each signal used to obtain an initial value of an integral amplifier in Embodiment 13.

Fig. 26 is a block diagram illustrating a frequency determination block of a carrier triangular wave in Embodiment 14.

Description of Embodiments

[0034]

[Embodiment 1]

Fig. 1 is a configuration diagram illustrating a main

circuit of a power conversion circuit in which inverter units are connected in parallel.

[0035]

As illustrated in Fig. 1, an inverter unit 1 in which a switching element Tu1 and a switching element Tx1 are connected in series to each other is connected to both terminals of a direct current voltage source Vdc. In addition, inverter units 2 to N are connected to the direct current voltage source Vdc in parallel to the inverter unit 1.

[0036]

In the respective inverter units 1 to N, first ends of cross current suppression reactors L1 to LN are respectively connected to common connection points between the switching elements Tu1 to TuN and the switching elements Tx1 to TxN. In addition, second ends of the cross current suppression reactors L1 to LN are connected to each other, and a common connection point therebetween is connected to one of a reactor L11.

[0037]

Further, current detectors CTU1 to CTUN are respectively provided on output sides of the cross current suppression reactors L1 to LN, and detect output currents IinvU1 to IinvUN from the respective inverter units 1 to N as detection signals IinvU1det to IinvUNdet. Still further, a current detector CTU is provided on an output side of the reactor L11, and detects a total output current IinvU of the inverter units as a

detection signal IinvUdet.

[0038]

In Fig. 1, inverter units 1 to N related to only a U phase is illustrated, but, for example, in a case of a three-phase power conversion circuit, configurations related to a V phase and a W phase are the same as the configuration illustrated in Fig. 1.

[0039]

Fig. 2 illustrates a cross current suppression control block for each phase of the inverter unit in Embodiment 1. Herein, it is assumed that there are N inverter units, and the N-th inverter unit N is a control target in the cross current suppression control block.

[0040]

In Embodiment 1, a cross current is detected, and the cross current is suppressed by adjusting a timing of a gate signal.

[0041]

A PWM modulator 21 receives an output voltage command value Vuref, and compares the amplitude thereof with the amplitude of a carrier triangular wave Vcarry so as to generate a gate command value Gref. The output voltage command value Vuref may be provided through feed-forwarding, and may be output from a voltage control section (not illustrated) or a current control section (not illustrated) of the inverter unit.

In addition, the carrier triangular wave Vcarry is output from a control section (not illustrated) of the inverter unit.

[0042]

The gate command value Gref of 1 causes a gate signal GuN applied to the switching element TuN of the upper arm to enter an ON state and causes a gate signal GxN applied to the switching element TxN of the lower arm to enter an OFF state, and the gate command value Gref of 0 causes the gate signal GuN applied to the switching element TuN of the upper arm to enter an OFF state and causes the gate signal GxN applied to the switching element TxN of the lower arm to enter an ON state.

[0043]

A delay adder DelayU delays a timing at which the gate command value Gref rises from 0 to 1 on the basis of a rising gate delay command value DelayrefU which is output from a gate delay command value calculation block 23.

[0044]

A delay adder DelayD delays a timing at which the gate command value Gref falls from 1 to 0 on the basis of a falling gate delay command value DelayrefD which is output from the gate delay command value calculation block 23.

[0045]

A dead time processor 24 adds a dead time to a gate command value GrefN having undergone the delay process so as to output the gate signal GuN for the switching element TuN of the upper

arm and the gate signal GxN for the switching element TxN of the lower arm.

[0046]

A peak detector 22 operates once at a half of a switching cycle (hereinafter, referred to as a half switching cycle) of each of the above-described switching elements, and detects upper and lower peaks of the carrier triangular wave Vcarry. When the peaks are generated in the carrier triangular wave, the gate delay command value calculation block 23 operates on the basis of an output signal from the peak detector 22.

[0047]

Next, the gate delay command value calculation block 23 will be described.

[0048]

A divider div divides the inverter output current detection value IinvUdet by the number N of inverter units so as to calculate a mean value for each inverter unit, and sets the mean value as each inverter output current command value IinvUdet/N.

[0049]

A subtractor sub obtains a deviation (cross current) between the inverter unit output current command value IinvUdet/N and the inverter unit output current detection value IinvUNdet. A proportional amplifier P multiplies the deviation by any gain.

[0050]

A sign detector 25 outputs "1" if the inverter unit output current detection value IinvUNdet is positive, and outputs "0" if negative (in a case where an input value of the sign detector 25 is "0", the sign detector 25 may output any value).

[0051]

NOT elements NOT1 and NOT2 invert an output from the sign detector 25 (input and output signals of the two elements are the same as each other in Fig. 2 for simplification of illustration). An AND element AND1 outputs a logical product between the gate command value Gref and the sign of the inverter unit output current detection value IinvUNdet. An AND element AND2 outputs a logical product between the gate command value Gref and an inversion signal of the sign of the inverter unit output current detection value IinvUNdet. An AND element AND3 outputs a logical product between an inversion signal of the gate command value Gref and the sign of the inverter unit output current detection value IinvUNdet. An AND element AND4 outputs a logical product between the inversion signal of the gate command value Gref and the inversion signal of the sign of the inverter unit output current detection value IinvUNdet.

[0052]

An input switch SW11 is turned on if the inverter unit output current detection value IinvUNdet > 0, and the gate command value Gref = "1". An input switch SW21 is turned on

if the inverter unit output current detection value IinvUNdet < 0, and the gate command value Gref = "1". An input switch SW31 is turned on if the inverter unit output current detection value IinvUNdet > 0, and the gate command value Gref = "0". An input switch SW41 is turned on if the inverter unit output current detection value IinvUNdet < 0, and the gate command value Gref = "0".

[0053]

Integral amplifiers I1 to I4 perform an integral process on outputs from the input switches SW11 to SW14.

[0054]

An output switch SW12 is turned on if the inverter unit output current detection value IinvUNdet > 0, and outputs an output from the integral amplifier I1 to a subsequent stage. An output switch SW22 is turned on if the inverter unit output current detection value IinvUNdet < 0, and outputs an output from the integral amplifier I2 to the subsequent stage. An output switch SW32 is turned on if the inverter unit output current detection value IinvUNdet > 0, and outputs an output from the integral amplifier I3 to the subsequent stage. An output switch SW42 is turned on if the inverter unit output current detection value IinvUNdet < 0, and outputs an output from the integral amplifier I4 to the subsequent stage.

[0055]

An adder add1 adds the outputs from the proportional

amplifier P, the output switch SW12, and the output switch SW22 together. An output from the adder add1 is multiplied by -1 in a multiplier mul so that a sign thereof is inverted. An output from the multiplier mul corresponds to the gate delay command value DelayrefU at a timing at which the gate command value Gref rises from "0" to "1". An adder add2 adds the outputs from the proportional amplifier P, the output switch SW32, and the output switch SW42 together. An output from the adder add2 corresponds to the gate delay command value DelayrefD at a timing at which the gate command value Gref falls from "1" to "0".

[0056]

[Gate Delay Command Value using Proportional amplifier P]

The cross current (deviation) IinvUdet/N-IinvUNdet is input to the proportional amplifier P, a value obtained by multiplying the difference by any gain is output to the adders add1 and add2, and the gate delay command values DelayrefU and DelayrefD are output from the adders add1 and add2. If the cross current increases, the proportional amplifier P outputs greater gate delay command values DelayrefU and DelayrefD in proportion to the increase, and thus causes the values to be immediately reflected in a switching operation after the cross current is detected.

[0057]

In a case where the cross current (deviation) is positive, this indicates that the inverter unit output current detection value IinvUNdet of the inverter unit is smaller than the mean value (the inverter unit output current command value IinvUdet/N). In this case, the rising gate delay command value DelayrefU is a negative value, and advancing correction is performed on rising of the gate command value Gref. In addition, the falling gate delay command value DelayrefD is a positive value, and delaying correction is performed on the gate command value Gref. Consequently, a pulse width of the gate signal GuN increases, a pulse width of the gate signal GxN decreases, and thus an operation is performed so as to increase an output current.

[0058]

[Gate Delay Command Value using Integral Amplifiers I1 to I4]

Each of the integral amplifiers I1 to I4 stores a value which was output right before. In addition, a cross current is detected through the present switching operation and is input to the integral amplifiers I1 to I4, and a value obtained by multiplying the cross current by a gain and the value stored in each of the integral amplifiers are added together so as to be output as a new value of the integral amplifier. This operation is the same as an operation of a general integral amplifier. Consequently, several switching operations are

performed, and thus a delay difference caused by disturbance such as a difference in a distance to the switching element, a gate control board, or a transmission path is learnt so that a deviation of a timing of the gate signal can be completely corrected.

[0059]

However, each inverter unit includes two switching elements for each phase, and four integral amplifiers are required for each phase when taking into consideration differences in rising and falling characteristics. For this reason, in Fig. 2, the integral amplifiers I1 to I4 are provided for each phase. In addition, the gate delay command value is required to be reflected only in a corresponding switching element. For this reason, the switches S11, S12, S21, S22, S31, S32, S41 and S42 are provided on the input and output sides of the four integral amplifiers I1 to I4, and an operation and a non-operation of each of the integral amplifiers I1 to I4 are switched depending on a condition.

[0060]

[Gate Delay Command Value Output from Integral Amplifier I1]

The output switch SW12 located on the subsequent stage of the integral amplifier I1 is turned on when a direction of the inverter unit output current detection value IinvUNdet is positive. For this reason, the output switch SW12 is turned

on when the direction of the inverter unit output current detection value IinvUNdet is positive, and the switching element TuN of the upper arm switches from an OFF state to an ON state, and thus delay corresponding to the command value without being changed is added to the gate command value Gref in the delay adder DelayU. The output switch SW12 is also turned on when the switching element TuN of the upper arm switches from an ON state to an OFF state, but, at this time, the gate signal falls, and thus delay is not added to the gate command value Gref.

[0061]

The input switch SW11 is turned on when the direction of the inverter unit output current detection value IinvUNdet is positive, the gate command value Gref is "1", and the switching element TuN of the upper arm is turned on. Therefore, the integral amplifier I1 receives a cross current which is generated after the switching element TuN of the upper arm switches from an OFF state to an ON state, and updates a value stored therein to a value obtained by the stored value to the input value. Through the above-described operation, the integral amplifier I1 performs delay command calculation of a turned-on state of the switching element TuN of the upper arm.

[0062]

[Gate Delay Command Value Output from Integral Amplifier

I3]

The output switch SW32 located on the subsequent stage of the integral amplifier I3 is turned on when a direction of the inverter unit output current detection value IinvUNdet is positive. For this reason, the output switch SW32 is turned on when the direction of the inverter unit output current detection value IinvUNdet is positive, and the switching element TuN of the upper arm switches from an ON state to an OFF state, and thus delay corresponding to the command value without being changed is added to the gate command value Gref in the delay adder DelayD.

[0063]

The input switch SW31 is turned on when the direction of the inverter unit output current detection value IinvUNdet is positive, the gate command value Gref is "0", and the switching element TuN of the upper arm is turned off. Therefore, the integral amplifier I3 receives a cross current which is generated after the switching element TuN of the upper arm switches from an ON state to an OFF state, and updates a value stored therein to a value obtained by the stored value to the input value.

[0064]

Since the direction of the inverter unit output current detection value IinvUNdet is positive in this condition, a diode which is reversely connected in parallel to the switching

element TxN is turned when a current flows through the lower arm. For this reason, even when the switching element TxN of the lower arm switches from an ON state to an OFF state, a current is not influenced. A current flow path is determined depending on a turned-on state of the switching element TuN of the upper arm.

[0065]

Through the above-described operation, the integral amplifier I3 performs delay command calculation of a turned-off state of the switching element TuN of the upper arm.

[0066]

[Gate Delay Command Values Output from Integral Amplifiers I2 and I4]

In the integral amplifiers I2 and I4, the output switches SW22 and SW42 are turned on when the direction of the inverter unit output current detection value IinvUNdet is positive. For this reason, the output switch SW22 is turned on when the direction of the inverter unit output current detection value IinvUNdet is negative, and the switching element TuN of the upper arm switches from an ON state to an OFF state, and thus delay corresponding to the command value without being changed is added to the gate command value Gref in the delay adder DelayD.

[0067]

In addition, the output switch SW42 is turned on when

the direction of the inverter unit output current detection value IinvUNdet is negative, and the switching element TuN of the upper arm switches from an OFF state to an ON state, and thus delay corresponding to the command value without being changed is added to the gate command value Gref in the delay adder DelayD. In a case where the direction of the inverter unit output current detection value IinvUNdet is negative, a current flow path is determined depending on a switching state of the switching element TuN of the upper arm. Therefore, the integral amplifiers I2 and I4 output delay command values of the lower arm.

[0068]

Through the above-described operation, the integral amplifier I2 performs turning-off of the switching element TxN of the lower arm, and the integral amplifier I4 performs turning-on of the switching element TxN of the lower arm.

[0069]

An operation of the cross current suppression control block will be described by using an example. Herein, it is assumed that the sign of the inverter unit output current detection value IinvUNdet is positive, and the inverter unit output current detection value IinvUNdet is smaller than the inverter unit output current command value IinvUdet/N, that is, a deviation therebetween is positive and thus an output current of the control target inverter unit N is small. In

addition, the gate command value Gref is assumed to be "1".

[0070]

If a peak of the carrier triangular wave Vcarry is detected by the peak detector 22, the gate delay command value calculation block 23 operates, and the input switch SW11, and the output switches SW12 and SW32 are turned on. When the gate delay command value calculation block 23 operates in the previous time, the carrier triangular wave Vcarry reaches a peak at the gate command value Gref of "0", then the gate command value Gref goes to "1", and a cross current generated due to turning-on of the switching element TuN of the upper arm is detected by the sign detector 25. Therefore, the AND element AND1 outputs a signal of "1" so as to turn on the input switch SW11, and thus the deviation (cross current) is input to the integral amplifier I1 so that a timing delay amount of turning-on of the switching element TuN of the upper arm is updated.

[0071]

In addition, since the output switch SW32 is turned on, DelayrefD is a result of adding outputs from the proportional amplifier P and the integral amplifier I3 together. The proportional amplifier P detects the present cross current, and adjusts a timing of the gate signal in the next switching operation. Since an output signal from the sign detector 25 has a positive sign, the current detection value IinvUNdet of

the inverter unit N is in a state of passing through the switching element TuN of the upper arm, and since the gate command value Gref is "1", the switching element TuN of the upper arm is turned off from now on. For this reason, the output switch SW32 is turned on so that an output from the integral amplifier I3 which performs turning-off of the switching element TuN of the upper arm is reflected in the falling gate delay command value DelayrefD, and thus a timing of the gate signal in a turned-off state of the switching element TuN of the upper arm is adjusted. At this time, the input switch SW12 is also turned on, but, in this state, the gate command value Gref falls from now on, and thus the rising delay command value DelayrefU is disregarded.

[0072]

Fig. 3 illustrates a state in which a cross current is suppressed by the above-described cross current suppression control block. In Fig. 3, it is assumed that two inverter units are provided, and only a gate command value Gref2 is delayed due to disturbance. For this reason, rsing of the gate command value Gref2 is delayed in an initial switching operation.

[0073]

In this state, the switching element Tu1 of the upper arm of the inverter unit 1 and the switching element Tx2 of the lower arm of the inverter unit 2 are turned on, and thus an inverter direct current voltage is applied to the U-phase

cross current suppression reactors L1 and L2 of the inverter unit 1 and the inverter unit 2. Since the cross current suppression reactors L1 and L2 are assumed to have small sizes, the output current IinvU1 from the inverter unit 1 rapidly increases, and the output current IinvU2 from the inverter unit 2 decreases, so that a large cross current is generated.

[0074]

In contrast, in the control according to Embodiment 1, a cross current is detected at the peak of the carrier triangular wave Vcarry corresponding to the half switching cycle, and cross current suppression control is performed. Since the output current IinvU1 from the inverter unit 1 is large, the gate delay command value calculation block 23 advances turning-off of the gate command value Gref1 and delays turning-on of the gate command value Gref2 by using the proportional amplifier P. Consequently, the cross current is reduced.

[0075]

In addition, in this case, since a direction of the inverter unit output current detection value IinvU1det is positive, it can be seen that the cross current is caused by a deviation between turning-on timings of the switching elements Tu1 and Tu2 of the upper arm. Therefore, the cross current at this time is input to the integral amplifier I1, the next gate signal for turning on the switching element Tu1

of the upper arm of the inverter unit 1 is delayed, the next gate signal for turning on the switching element Tu2 of the upper arm of the inverter unit 2 is advanced, so that a timing of a switching operation is adjusted. This operation is repeatedly performed several times so that the integral amplifier I1 learns the delay caused by disturbance and cancels out the delay, and thus timings of the switching operations of the switching elements Tu1 and Tu2 are aligned with each other.

[0076]

In Fig. 3, a cross current varies even when states of the gate command values Gref1 and Gref2 are the same as each other (a differentiation result is included in a current of each inverter unit). This is because it is assumed that there is a difference in voltage drop Vce(sat) of the switching element, voltage drop Vf of the reverse parallel diode, sizes of the cross current suppression reactors L11 and L12 attached to the respective inverter units, or a parasitic inductance component.

[0077]

In contrast, in Embodiment 1, an operation is performed so that only a cross current at a peak of the carrier triangular wave Vcarry is detected, and the cross current between the inverter units becomes zero. Since a frequency of a fundamental wave is sufficiently smaller than that of the

carrier triangular wave Vcarry, the voltage command value Vref can be regarded to be substantially constant for one cycle of the carrier signal. For this reason, the peak of the carrier triangular wave Vcarry substantially corresponds to a center of a pulse, and thus a cross current at the peak of the carrier triangular wave Vcarry can be regarded to be a mean value of cross currents between the pulses. Therefore, if the cross current becomes zero at the peak of the carrier triangular wave, a current mean value in an output voltage pulse can be equalized.

[0078]

As mentioned above, according to Embodiment 1, it is not necessary to finely sample a cross current in real time. Since a state in which a cross current rapidly increases due to a timing deviation of the switching operation is not used for control, there are advantages in that a high-speed detector is not necessary, there is no hindrance in an operation of the cross current suppression control device even if a filter for removing noise is additionally provided, and high-speed communication between the inverter units or a control board for realizing the high-speed communication is not necessary. In addition, a calculation load is reduced, and thus it is possible to realize cross current suppression with an inexpensive system and to make a cross current mean value per cycle of a carrier signal zero.

[0079]

In addition, in a case where there is a margin in control performance of the cross current suppression control device, an output current around the peak of the carrier triangular wave Vcarry is sampled several times and is subjected to a filter process, and thus it is possible to improve operation stability against noise.

[0080]

In addition, in Fig. 3, even if a steady state occurs, the timings of the gate command values Gref1 and Gref2 do not completely match each other but are deviated relative to each other. This is because, an operation is performed so that a mean value of cross currents becomes zero, and thus the timings of gate command values Gref1 and Gref2 are intentionally deviated so as to cancel out a cross current caused by the voltage drop Vce(sat) of the switching element, the voltage drop Vf of the reverse parallel diode, an error of impedance of the cross current suppression reactors L1 and L2, or the like.

[0081]

In other words, by performing the cross current suppression control using the integral amplifiers I1 to I4, timings of the gate signals for the respective inverter units do not completely match each other but the timings of the gate signals are delayed, and thus it is possible to cancel out delay

disturbance of the gate signal caused by the voltage drop Vce(sat) of the switching element, the voltage drop Vf of the reverse parallel diode, or a physical configuration associated with a distance or a shape of a gate circuit or a transmission circuit. For this reason, it is not necessary to remove disturbance in order to suppress a cross current with separate means such as an element selected for constituting a transmission circuit or a main circuit, and thus it is possible to reduce cost or a weight by reducing a size of the cross current suppression reactor even in a content in which a level of the disturbance is high.

[0082]

In addition, there is a possibility that inductance required to suppress a cross current may be secured by using a parasitic inductance component of a cable, and thus it is not necessary to provide a separate reactor in this case.

[0083]

Further, since a plurality of integral amplifiers are provided, it is possible to suppress a cross current even in a case where there is a difference between characteristics of the switching elements of the upper and lower arms, and even in a case where there are is a characteristic difference between rising and falling of a switching element.

[0084]

[Embodiment 2]

Fig. 4 illustrates a cross current suppression control block for each phase of an inverter unit in Embodiment 2. Embodiment 2 is obtained by modifying Embodiment 1 as follows.

[0085]

The integral amplifiers I3 and I4, the input switches SW31, SW41, the output switches SW32 and SW42, and the AND elements AND1 to AND4 are omitted. In addition, the input switches SW11 and SW21 are operated on the basis of only a sign of the inverter unit output current detection value IinvUNdet regardless of a state of the gate command value Gref. Further, it is assumed that the falling gate delay command value DelayrefD is obtained by adding outputs from the proportional amplifier P and the output switches SW12 and SW22 together in the adder add1, and the rising gate delay command value DelayrefU is obtained by multiplying the gate delay command value DelayrefD by -1 in the multiplier mul so as to inverse a sign thereof.

[0086]

Embodiment 2 realizes a method in which a configuration of the cross current suppression control block is simplified by removing the two integral amplifiers I3 and I4 under a condition in which characteristics of rising and falling of the switching elements are substantially the same as each other. The proportional amplifier P performs the same operation as in Embodiment 1.

[0087]

[Gate Delay Command Value Output from Integral Amplifier I1]

Both of the output switches SW11 and SW12 are turned on when a direction of the inverter unit output current detection value IinvUNdet is positive. If a deviation is positive, this indicates that an output current IinvUN of the control target inverter unit is smaller. In this case, the integral amplifier I1 outputs a positive value so as to delay falling of the gate command value GrefN and to advance rising thereof. Thus, a pulse width of the gate signal GuN increases, and a pulse width of the gate signal GxN decreases. This acts so that the inverter unit output current IinvUN increases.

[0088]

Since an output current is positive when the input switches SW11 and SW12 are turned on, the inverter unit output current IinvUN passes through the switching element TuN of the upper arm. The integral amplifier I1 adjusts timings of the gate signals in both rising and falling for the switching element TuN of the upper arm.

[0089]

[Gate Delay Command Value Output from Integral Amplifier I2]

Similarly, when the integral amplifier I2 operates, the inverter unit output current detection value IinvUNdet is

negative, and a current passes through the switching element TxN of the lower arm. The integral amplifier I2 adjusts timings of the gate signals in both rising and falling for the switching element TxN of the lower arm.

[0090]

As described above, in Embodiment 2, a learning function of only pulse width adjustment is added, and a learning function of delay correction is deleted, but delay correction using the proportional amplifier P is still effective, and thus it is possible to sufficiently handle a cross current which is within a range of delay correction of the proportional amplifier P, for example, by designing a control board or an inverter unit.

[0091]

In contrast, in a case of satisfying a condition in which voltage drop characteristics of the switching elements can be aligned, accuracy of the cross current suppression reactor can be increased, or parasitic inductance components can be aligned by equalizing lengths of wirings, pulse width adjustment may be performed by the proportional amplifier P, and delay characteristics may be corrected by the integral amplifier.

[0092]

As mentioned above, Embodiment 2 achieves the same effect as Embodiment 1, and it is possible to realize cross current suppression control with a configuration in which the integral amplifiers are removed.

[0093]

[Embodiment 3]

Fig. 5 illustrates a control block for each phase of an inverter unit in Embodiment 3. Embodiment 3 is obtained by modifying Embodiment 1 as follows.

[0094]

A deviation signal (cross current) between IinvUdet/N and IinvUN output from the subtractor sub is input to a dead-band processor 26, and an output therefrom is input to the proportional amplifier P or the integral amplifiers I1 to I4.

[0095]

The dead-band processor 26 outputs zero if an absolute value of an input signal is smaller than a threshold value, and outputs the input signal which is approximate to zero by the threshold value if greater.

[0096]

Embodiment 3 realizes a method in which, when an absolute value of a cross current is small, the proportional amplifier P outputs zero, the integral amplifiers I1 to I4 output learning results up to the previous time, and thus update is not performed.

[0097]

A case is assumed in which IinvU1det+IinvU2det+…+ IinvUNdet becomes smaller than IinvUdet for the reason such

as detection errors being included in the current detectors CTU1 to CTUN and CUT, and a current detection value IinvUdet at an output joint of the respective inverter units is greater than a sum of the individual current detection values IinvU1det+IinvU2det+…+ IinvUNdet. At this time, IinvUNdet is smaller than IinvUdet/N even in a case where a cross current is completely suppressed. As a result, all the inverter units operate so as to increase output currents. If the output currents are increased, a sum of the output currents are increased to the current detection value IinvUdet at the output joint of the respective inverter units, and thus a deviation increases. Therefore, the integral amplifiers I1 to I4 run away, and a command value increases endlessly.

[0098]

For example, when N inverter units are provided, a degree of freedom in which a current of the individual inverter unit can be freely determined is N, but a total of (N+1) control circuits including an N cross current suppression control circuits of the respective inverter units and a circuit controlling a current at an output joint of the inverter units are required, and thus the degree of freedom of N is insufficient. Here, if there are deviations between a sum of the inverter unit output current detection values IinvU1det+IinvU2det+…+IinvUNdet of the current detectors CTU1 to CUTN and the current detection value IinvUdet of the inverter

output current detector CTU, there is the occurrence in a difference between magnitudes of currents which are caused to flow through current control and cross current suppression control, and the currents interfere to each other. Thus, the integral amplifiers for the current control and the cross current suppression control run away.

[0099]

In order to prevent a defect caused by the above-described interference, the integral amplifiers I1 to I4 stop being updated in a stage in which an influence of control interference due to the difference between the current detection values easily appears and an absolute value of a cross current is reduced.

[0100]

According to Embodiment 3, in addition to the operation and effect of Embodiment 1, since the cross current suppression control is stopped when a cross current is small, it is possible to prevent the integral amplifiers from running away even in a case where there are errors in the output current sum value IinvU1det+IinvU2det+…+IinvUNdet of the inverter units and the current detection value IinvUdet at the output joint.

[0101]

[Embodiment 4]

Fig. 6 illustrates a control block for each phase of an inverter unit in Embodiment 4. Embodiment 4 is obtained by

modifying Embodiment 1 as follows.

[0102]

As an output current command value of each inverter unit, instead of the current detection value IinvUdet at the output joint of the inverter units, an output current detection value IinvU1det of a certain representative inverter unit (here, the inverter unit 1) is used. Therefore, the divider div is not necessary, and thus a process of dividing a current detection value by the number N of the inverter units is not performed. If control using feedback is performed, a cross current can also be suppressed with the configuration of the present embodiment.

[0103]

For example, if the output current detection value IinvU1det of the inverter unit 1 is smaller than those of the other inverter units under a condition in which current control is performed, the cross current suppression control of the other inverter units is performed so as to reduce output currents. Then, the output currents are reduced to a sum IinvU of the inverter output currents, but the current control is performed so as to increase the inveter output current IinvU. Therefore, the output current IinvU1 of the inverter unit 1 increases, and thus current sharing can be equalized. This is also the same for a case of employing current control.

[0104]

In the inverter unit 1, since a detection value and a command value are the same as each other, a deviation is zero at all times, and thus the cross current suppression control is not performed. For this reason, a cross current suppression control circuit of the inverter unit 1 can be omitted.

[0105]

In addition, herein, current command values of other inverter units are used as the output current detection value IinvU1det of the inverter unit 1, but each inverter unit may refer to an output current detection value of a different inverter unit as a command value. For example, if an output current detection value of an inverter unit located nearby is selected as a command value, a wiring can be simplified.

[0106]

In addition, in Embodiment 4, the same effect as that of Embodiment 3 can be achieved even if the dead-band processor 26 is not additionally provided. For example, when N inverter units are provided, a total number of control circuits is N including (N-1) cross current suppression control circuits of the inverter units and a circuit which controls currents of all the inverter units, and is the same as the degree of freedom of N in this case. For this reason, the control circuits can control currents of all the inverter units without causing interference. In a case where the current detection value IinvU1det of the representative inverter unit 1 is greater than

the output current IinvU1 of the representative inverter unit 1, all the remaining inverter units operate so as to increase output currents. Then, a cross current flows from the other inverter units to the representative inverter unit 1 so that the output current IinvU1 of the representative inverter unit 1 is reduced, and the current detection value IinvU1det of the representative inverter unit 1 is also reduced, and thus a deviation therebetween decreases. For this reason, the integral amplifier converges on a certain point, and thus it is possible to prevent the integral amplifier from running away in the cross current suppression control due to control interference.

[0107]

[Embodiment 5]

Fig. 7 illustrates a control block for each phase of an inverter unit in Embodiment 5. Embodiment 5 is obtained by modifying the gate delay command value calculation block of Embodiment 1 as follows.

[0108]

The subtractor sub which obtains a deviation between the inverter unit output current command value IinvUdet/N and the inverter unit output current detection value IinvUNdet is modified to a combination of a multiplier mul2 which multiplies the inverter unit output current detection value IinvUNdet by -1 and a dead-band processor 27.

[0109]

In addition, a sign detector 28 which outputs 1 if the inverter unit output current detection value IinvUNdet is positive and outputs -1 if negative, a heat duty equalizing block 29, and a multiplier mul3 which calculates a product of outputs from the heat duty equalizing block 29 and the sign detector 28 by each other are additionally provided. An output from the multiplier mul3 is added to an output from the proportional amplifier P in an adder add3.

[0110]

Next, the heat duty equalizing block 29 will be described.

[0111]

An effective value calculator RMS1 obtains and outputs an inverter unit output current effective value IinvUNrms on the basis of the inverter unit output current detection value IinvUNdet. In addition, an effective value calculator RMS2 obtains and outputs an inverter unit output current effective value IinvUrms on the basis of the inverter unit output current detection value IinvUNdet. The divider div divides the inverter unit output current effective value IinvUrms by the number N of inverter units so as to obtain a mean value IinvUrms/N of the inverter unit output current effective values. The subtractor sub calculates a deviation between the mean value IinvUrms/N of the inverter unit output current effective

values and an effective value IinvUNrms of the inverter unit output current detection value IinvUNdet. This deviation is input to a proportional integral amplifier PI so as to undergo a proportional integral process.

[0112]

Embodiment 5 realizes a method in which cross current suppression control is performed only on a current peak in the same manner as in Embodiment 1, and low-speed control is performed on heat duty by using a proportional integral process.

[0113]

First, in Embodiment 5, regarding a set value of the dead-band processor 27, a current in which a margin is added to a peak value of an absolute rated current of the switching element or the maximum current output from a power conversion circuit is used as the set value. The cross current suppression control is performed only in a case where the set value is exceeded, and thus prevents a situation in which a current concentrates on a specific inverter unit and thus a switching element thereof is damaged due to overcurrent.

[0114]

However, this state is a state in which a peak current is shared. For this reason, there is a possibility that, when the power conversion circuit outputs a small current, the inverter output current IinvU may concentrate on a specific

inverter unit, and thus only the inverter unit may be heated so that a component thereof is damaged. Therefore, the inverter unit output current effective value IinvUrms is detected, and the heat duty is equalized by adjusting timings of the gate signals.

[0115]

A description will be made of an operation of the proportional integral amplifier PI of the heat duty equalizing block 29 in Embodiment 5. As an example, if the mean value IinvUrms/N of the inverter unit output current effective value > the effective value IinvUNrms of the inverter unit output current detection value, and the effective value IinvUNrms of the inverter unit output current detection value > 0, this leads to a state in which an amplitude of an output current from a control target inverter unit is insufficient. At this time, an output from the proportional integral amplifier PI positive, an output from the multiplier mul3 is also positive, the rising gate delay command value DelayrefU is positive, and the falling gate delay command value DelayrefD is positive. For this reason, a pulse width of the gate signal GuN increases, and thus an output current is prompted to increase.

[0116]

If the inverter unit output current detection value IinvUNdet < 0, the rising gate delay command value DelayrefU is positive, the rising gate delay command value DelayrefD is

negative, and thus a pulse width of the gate signal GxN increases so that the amplitude of the inverter unit output current increases. Consequently, the control target inverter unit output current effective value Iinvrms increases.

[0117]

The heat duty equalizing block 29 which is additionally provided in Embodiment 5 is operated once at one cycle of a fundamental wave for the following reasons (1) and (2).

(1) It takes at least a time period of one cycle of the fundamental wave to obtain an effective value from a single-phase signal.

(2) Even if a current instantaneously increases, a temperature of the switching element does not increase much, and thus an influence on the heat duty is not great.

[0118]

Consequently, peak current equalizing control which is required to be performed at a high speed (half switching cycle) is completed in a single inverter unit, and thus current detection signals for other inverter units are not required to be obtained. For this reason, in a case where delay occurs when the current detection signal is transmitted to other inverter units or to a position far from a current joint of the inverter units, a problem caused by transmission delay can be solved by employing Embodiment 5. Since high-speed signal transmission is not necessary, and transmission may be

performed once at one cycle of the fundamental wave, an inexpensive signal transmission system can be used.

[0119]

In addition, although an effective value is used in Embodiment 5, a filter may be applied to a current detection value for rectification, and a current mean value of absolute values per cycle of the fundamental wave may be obtained and may be used for the cross current suppression control. In addition, a filter having a great time constant can be used, and thus it is possible to improve stability against noise.

[0120]

[Embodiment 6]

Fig. 8 illustrates a control block for each phase of an inverter unit in Embodiment 6. Embodiment 6 is obtained by modifying the gate delay command value calculation block 23 of Embodiment 1 as follows.

[0121]

An absolute value detection block ABS detects an absolute value of the inverter unit output current IinvUN. A comparator 30 compares the absolute value with a predetermined threshold value α, and outputs "0" if the absolute value is smaller than the threshold value and outputs "1" if greater. If the comparator 30 outputs "0", the switch SW5 is turned off, and thus "0" is input to the integral amplifiers I1 to I4 as input signals thereof. If "1" is output, the switch SW5 is turned

on, a deviation (cross current) is input to the integral amplifiers I1 to I4 as input signals thereof.

[0122]

In Embodiment 6, the switch SW5 is additionally provided on the input sides of the integral amplifiers I1 to I4. Consequently, when the absolute value of the inverter unit output current IinvUN is smaller than the threshold value α, values of the integral amplifiers I1 to I4 stop being updated.

[0123]

The reason of stopping values of the integral amplifiers I1 to I4 is that, when the absolute value of the inverter unit output current IinvUN is small, it is hard to accurately detect whether a current passes through the switching element TuN of the upper arm or the switching element TxN of the lower arm. Particularly, there is a sufficient possibility that an actual current direction may be different from a sign of a current detected by the current detector due to delay caused by the current detectors CTU1 to CUTN, delay caused by a filter, or superimposition caused by switching ripple.

[0124]

In Embodiment 6, since the integral amplifiers I1 to I4 stop being updated in a case where an absolute value of the inverter unit output current IinvUN is small as mentioned above, the cross current suppression control is prevented from being erroneously performed, and thus a cross current between the

inverter units is prevented from increasing when the inverter unit output current IinvUN increases next. In this case, there is danger in which a cross current increases when an absolute value of the inverter unit output current IinvUN is small. However, since the absolute value of the inverter unit output current IinvUN is small, the switching element is not destroyed due to the inverter unit output current Iinv exceeding an absolute rated current value even if a cross current is generated. In addition, since a loss is small, an influence on sharing of the heat duty is very small. For this reason, even if the integral amplifiers I1 to I4 stop being updated when an absolute value of the inverter unit output current IinvUN is small, a cross current between the inverter units is not problematic.

[0125]

As mentioned above, according to Embodiment 6, in addition to the operation and effect of Embodiment 1, since the cross current suppression control is stopped when an absolute value of the inverter unit output current IinvUN is small, even if a wrong sign of the inverter unit output current IinvUN is detected due to delay or noise, the cross current suppression control is prevented from being erroneously performed, and thus it is possible to prevent a cross current from increasing when the inverter output current IinvUN increases next.

[0126]

[Embodiment 7]

Fig. 9 illustrates a control block for each phase of an inverter unit in Embodiment 7. Embodiment 7 is obtained by modifying Embodiment 1 as follows.

[0127]

An activation signal of the gate delay command value calculation block 23 is changed from a signal detecting a peak of the carrier triangular wave Vcarry to a signal detecting a variation in the gate command value Gref. The variation in the gate command value Gref is detected through exclusive OR EXOR between the present gate command value Gref, and the gate command value Gref one calculation time ago.

[0128]

Consequently, a timing of detecting a cross current is also right before the switching element operates, and thus control delay can be reduced when compared with suppression control of a cross current which is detected at a peak of the carrier triangular wave Vcarry. As a result, it is possible to improve a transient response when a temperature varies, a change of an operation condition of the power conversion circuit, such as a change of an output current command value occurs, or disturbance occurs. In addition, modulation methods other than a PWM method may be employed since execution of the cross current suppression control is not dependent on

the carrier triangular wave Vcarry. Also in Embodiment 7, a cross current is not required to be finely detected, and thus a high-speed current detector is not necessary.

[0129]

However, in this method, a timing at which a cross current becomes zero is not a peak of the carrier wave but right before switching. For this reason, in terms of a mean current for one cycle of the carrier triangular wave Vcarry, a cross current in a steady state increases more than in Embodiment 1. In addition, if the gate command value Gref varies, A/D conversion, command value calculation, and timing adjustment are all required to be performed at a high speed, and thus a control device is required to have high performance. Alternatively, the gate delay command value calculation block 23 may be operated at all times so as to handle the variation in the gate command value Gref.

[0130]

According to Embodiment 7, in addition to the operation and effect of Embodiment 1, since execution of the cross current suppression control is not dependent on the carrier triangular wave Vcarry, modulation methods which do not use the carrier triangular wave Vcarry may be employed. In addition, since the gate delay command value calculation block 23 is operated right before the gate command value Gref varies, control delay in the cross current suppression control is reduced, and thus

it is possible to improve control stability and to shorten control time taken to suppress a cross current.

[0131]

[Embodiment 8]

Fig. 10 illustrates a control block for each phase of an inverter unit in Embodiment 8. Embodiment 8 is obtained by modifying Embodiment 1 as follows.

[0132]

A sign detector 31 detects a sign of the carrier triangular wave Vcarry and outputs the detected signal to the AND elements AND1 to AND4.

[0133]

An inversion signal of an output signal from the sign detector 31 is input to the AND elements AND1 and AND2, and one of conditions for turning on the input switches SW11 and SW21 is changed to a condition in which a "sign of the carrier triangular wave Vcarry is negative".

[0134]

The output signal from the sign detector 31 is input to the AND elements AND3 and AND4 without being changed, and one of conditions for turning on the input switches SW31 and SW41 is changed to a condition in which a "sign of the carrier triangular wave Vcarry is positive".

[0135]

A switch SW7 receives the rising gate delay command value

DelayrefU and is turned on when the sign of the carrier triangular wave Vcarry is positive. In addition, a switch SW6 receives the falling gate delay command value DelayrefD and is turned on when the sign of the carrier triangular wave Vcarry is negative. Output values from the switches SW6 and SW7 are added to a voltage command value VUref so as to be output as a voltage command value VurefN of the corresponding inverter unit N. The voltage command value VurefN undergoes PWM modulation and is added with dead time in a PWM modulator 21 and a dead-time processor 24, and are generated as the gate signals GuN and GxN.

[0136]

Embodiment 8 realizes a method in which a gate timing can be changed indirectly by adusting the voltage command value Vuref without directly changing the gate timing. Also in Embodiment 8, four integral amplifiers I1 to I4 are provided in the same manner as in Embodiment 8. In addition, the switches SW6 and SW7 perform switching by using a sign of the carrier triangular wave Vcarry, and thus a correction amount added to the voltage command value Vuref can be switched at a half cycle (half switching cycle) of the carrier triangular wave.

[0137]

For example, in a case where a sign of the carrier triangular wave Vcarry is positive at a peak thereof, and the

gate command value Gref rises at a half cycle of the next carrier triangular wave Vcarry, the voltage command value Vuref is increased. In addition, in a case where a sign of the carrier triangular wave Vcarry is negative at a peak thereof, and the gate command value Gref falls at a half cycle of the next carrier triangular wave Vcarry, the voltage command value Vuref is decreased. Consequently, it is possible to perform the cross current suppression control so that both rising and falling of the gate command value Gref are advanced.

[0138]

In other words, an advantage of Embodiment 8 is to advance a timing of the gate signal by performing adjustment for increasing or decreasing the voltage command value Vuref as mentioned above. In Embodiment 1, an adjustment target is not the voltage command value Vuref but the gate command value Gref, and thus only a timing of the gate command value Gref can be delayed. In a case where the gate command value Gref for a specific inverter unit is desired to be advanced in Embodiment 1, appropriate initial values are set in the integral amplifiers I1 to I4, timings of the gate command values Gref are uniformly delayed in all the inverter units, and then only a delay amount of the gate command value Gref for the specific inverter unit is required to be reduced. In Embodiment 8, this operation is not necessary, and thus control for reducing delay of a control system is more stabilized.

[0139]

[Embodiment 9]

Fig. 11 illustrates a main circuit of a power conversion circuit in Embodiment 9, and Fig. 12 illustrates a cross current suppression control block for each phase of an inverter unit in Embodiment 9. Embodiment 9 relates to a power conversion circuit in which the cross current suppression control of Embodiment 1 is applied to a 3-level inverter.

[0140]

As illustrated in Fig. 11, switching elements T11, T21, T31 and T41 are connected in series from a positive potential side of serially connected capacitors C1 and C2 which are direct current voltage sources to a negative potential side thereof. A diode is reversely connected in parallel to each of the switching elements T11, T21, T31 and T41. Clamp diodes DC1 and DC2 are respectively connected between a common connection point of the switching elements T11 and T21 and a neutral point of the capacitors C1 and C2, and between a common connection point of the switching elements T31 and T41 and the neutral point of the capacitors C1 and C2. In addition, an AC output signal corresponding to one phase is applied to a connection point between the switching elements T21 and T31. Further, the inverter units 2 to N having the same circuit configuration as that of the inverter unit 1 are connected in parallel to the inverter unit 1.

[0141]

Next, a description will be made of a difference from Embodiment 1 in the cross current suppression control block of Embodiment 9 with reference to Fig. 12. A PWM modulator 21 outputs two values including a gate command value Gref1 corresponding to gate signals for a switching element T1N and a switching element T3N and a gate command value Gref2 corresponding to gate signals for a switching element T2N and a switching element T4N.

[0142]

In addition, delay adders DelayU1, DelayD1, DelayU2 and DelayD2 respectively corresponding to the gate command values Gref1 and Gref2. Further, a dead-time processor 24 outputs four gate signals G1N, G2N, G3N and G4N having undergone a dead-time process.

[0143]

Next, a description will be made of a difference from Embodiment 1 in the gate delay command value calculation block 23.

[0144]

Buffers 32a and 32b hold values of the gate command values Gref1 and Gref2 a half cycle of the carrier triangular wave Vcarry ago. In addition, integral amplifiers I5 to I8, input switches SW51, SW61, SW71 and SW81, output switches SW52, SW62, SW72 and SW82, and AND elements AND5 to AND8 are additionally

provided.

[0145]

An output signal from the sign detector 25 is input to the AND elements AND1 to AND4, and one of conditions for turning on the input switches SW11, SW21, SW31 and SW41 is that the "inverter unit output current detection value IinvUNdet is positive". In addition, an inversion signal of an output signal from the sign detector 25 is input to the AND elements AND5 to AND8, and one of conditions for turning on the input switches SW51, SW61, SW71 and SW81 is that the "inverter unit output current detection value IinvUNdet is negative".

[0146]

Another condition for turning on the input switches SW11 and SW51 is that the gate command value Gref1 is "1", the gate command value Gref1 a half cycle of the carrier triangular wave Vcarry ago is "0", and the gate command value Gref2 a half cycle of the carrier triangular wave Vcarry ago is "1".

[0147]

Another condition for turning on the input switches SW21 and SW61 is that the gate command value Gref1 is "0", the gate command value Gref1 a half cycle of the carrier triangular wave Vcarry ago is "1", and the gate command value Gref2 is "1".

[0148]

Another condition for turning on the input switches SW31 and SW71 is that the gate command value Gref2 is "1", the gate

command value Gref2 a half cycle of the carrier triangular wave Vcarry ago is "0", and the gate command value Gref1 is "0".

[0149]

Another condition for turning on the input switches SW41 and SW81 is that the gate command value Gref2 is "0", the gate command value Gref2 a half cycle of the carrier triangular wave Vcarry ago is "1", and the gate command value Gref1 a half cycle ago is "0".

[0150]

A condition for turning on the output switches SW12, SW22, SW32 and SW42 is assumed to be that the "inverter output current detector IinvUNdet is positive". A condition for turning on the output switches SW52, SW62, SW72 and SW82 is assumed to be that the "inverter output current detector IinvUNdet is negative".

[0151]

The adder add1 adds outputs from the proportional amplifier P and the output switches SW12 and SW52, and the multiplier mul1 multiplies an addition result in the adder add1 by -1 so as to invert a sign thereof. An output from the multiplier mul1 is a gate delay command value Delayref1U at a timing at which the gate command value Gref1 rises from "0" to "1".

[0152]

The adder add2 adds outputs from the proportional

amplifier P and the output switches SW22 and SW62. An output from the adder add2 is a gate delay command value Delayref1D at a timing at which the gate command value Gref1 falls from "1" to "0".

[0153]

In addition, the adder add3 adds outputs from the proportional amplifier P and the output switches SW32 and SW72, and the multiplier mul2 multiplies an addition result in the adder add3 by -1 so as to invert a sign thereof. An output from the multiplier mul2 is a gate delay command value Delayref2U at a timing at which the gate command value Gref2 rises from "0" to "1".

[0154]

The adder add4 adds outputs from the proportional amplifier P and the output switches SW42 and SW82 together. An output from the adder add4 is a gate delay command value Delayref2D at a timing at which the gate command value Gref2 falls from "1" to "0".

[0155]

Embodiment 9 is an example of being applied to the 3-level inverter. In the 3-level inverter, four switching elements are required for each phases, and thus the eight integral amplifiers I1 to I8 are used for the cross current suppression control. Each integral amplifier will be described.

[0156]

[Integral Amplifier I1]

The input switch SW11 is turned on when the inverter unit output current detection value IinvUNdet is positive, and the gate command value Gref1 changes from "0" to "1". An output from the integral amplifier I1 is used to correct a rising timing of the gate command value Gref1. The gate command value Gref1 corresponds to the switching elements T1N and T3N, and since a direction of the inverter unit output current IinvUN is positive, the current passes through the switching element T1N at this time. For this reason, the integral amplifier I1 performs rising related to the switching element T1N.

[0157]

[Integral Amplifier I2]

The input switch SW21 is turned on when the inverter unit output current detection value IinvUNdet is positive, and the gate command value Gref1 changes from "1" to "0". An output from the integral amplifier I2 is used to correct a falling timing of the gate command value Gref1. The gate command value Gref1 corresponds to the switching elements T1N and T3N, and since a direction of the inverter unit output current IinvUN is positive, the current passes through the switching element T1N at this time. For this reason, the integral amplifier I1 performs falling related to the switching element T1N.

[0158]

[Integral Amplifier I3]

The input switch SW31 is turned on when the inverter unit output current detection value IinvUNdet is positive, and the gate command value Gref2 changes from "0" to "1". An output from the integral amplifier I3 is used to correct a rising timing of the gate command value Gref2. The gate command value Gref2 corresponds to the switching elements T2N and T4N, and since a direction of the inverter unit output current IinvUN is positive, the current passes through the switching element T2N at this time. For this reason, the integral amplifier I3 performs rising related to the switching element T2N.

[0159]

[Integral Amplifier I4]

The input switch SW41 is turned on when the inverter unit output current detection value IinvUNdet is positive, and the gate command value Gref2 changes from "1" to "0". An output from the integral amplifier I4 is used to correct a falling timing of the gate command value Gref2. The gate command value Gref2 corresponds to the switching elements T2N and T4N, and since a direction of the inverter unit output current IinvUN is positive, the current passes through the switching element T2N at this time. For this reason, the integral amplifier I4 performs falling related to the switching element T2N.

[0160]

[Integral Amplifier I5]

The input switch SW51 is turned on in the same condition

as in the input switch SW11 except that the inverter unit output current detection value IinvUNdet is negative. Since a direction of the inverter unit output current IinvUN is negative, the current passes through the switching element T3N at this time. For this reason, the integral amplifier I5 performs rising related to the switching element T3N.

[0161]

[Integral Amplifiers I6 to I8]

Similarly, the integral amplifier I6 performs falling related to the switching element T3N, the integral amplifier I7 performs rising related to the switching element T4N, and the integral amplifier I8 performs falling related to the switching element T4N.

[0162]

As mentioned above, the integral amplifiers corresponding to rising and falling related to the respective switching elements are provided, and timings of the gate signals for the switching elements, which influence a cross current, are adjusted, and thus it is also possible to cross current suppression control in the 3-level inverter in the same manner.

[0163]

In the above-described method, the control system controls a timing of the gate signal once during a half cycle of the carrier triangular wave Vcarry so as to perform the cross

current suppression control on the premise that one switching operation is performed at the half cycle of the carrier triangular wave Vcarry. However, in a multi-level inverter, the premise condition that "one switching operation is performed at the half cycle of the carrier triangular wave Vcarry" may not be established, for example, two switching operations are performed during a half cycle of the carrier triangular wave Vcarry, or a switching operation is not performed.

[0164]

Fig. 13 illustrates this state. In Fig. 13, it is assumed that a direction of the inverter unit output current IinvUN is positive. Looking at rising related to the switching element T1, in an interval E, the switching element T1 performs one switching operation during a half cycle of the carrier triangular wave Vcarry so as to change from an OFF state to an ON state. The switching element T1 also changes from an OFF state to an ON state in an interval C, but, simultaneously, the switching element T2 also changes from an OFF state to an ON state. A variation in a cross current at this time is caused not only by the switching element T1 but also by the switching element T2, and thus the cross current suppression control is required to be stopped. For this reason, the condition in which the gate command value Gref2 a half cycle of the carrier triangular wave Vcarry ago is "1" is added to the condition

in which the input switch SW11 is turned on, and thus an input value to the integral amplifier I1 becomes zero in the interval C.

[0165]

Similarly, looking at falling related to the switching element T1, in an interval D, the switching element T1 performs one switching operation during a half cycle of the carrier triangular wave Vcarry so as to change from an ON state to an OFF state. However, in an interval A, the switching element T1 remains in an OFF state and does not perform switching. A cross current generated at this time is not a deviation of a switching operation of the switching element T1 due to the voltage drop Vce(sat) in the switching element, the voltage drop vf in the reverse parallel diode, errors of the cross current suppression reactors L1 and L2, or the like, and thus the cross current suppression control is also required to be stopped in this case. For this reason, the condition in which the gate command value Gref1 a half cycle of the carrier triangular wave Vcarry ago is "1" is added to the condition in which the input switch SW21 is turned on, and thus the cross current suppression control is not performed in the interval A.

[0166]

In addition, in an interval B, the switching element T1 changes from an ON state to an OFF state, but the switching

element T2 also changes from an ON state to an OFF state. The content in which the gate command value Gref2 is "1" is an operation condition of the integral amplifier I2 so that the cross current suppression control is not performed.

[0167]

As mentioned above, integral amplifiers are additionally provided according to the number of switching elements, a switching element which has an influence on a cross current is detected on the basis of an operation condition of the switching element, and a corresponding integral amplifier performs cross current suppression control. Therefore, not only the 3-level inverter but also multi-level inverters may be employed.

[0168]

Although a 3-level NPC inverter has been described as an example in Embodiment 9, similar cross current suppression control can also be performed in a 3-level A-NPC inverter by detecting a switching element which has an influence on a cross current on the basis of an operation condition thereof and performing corresponding cross current suppression control.

[0169]

According to Embodiment 9, even when inverter units are constituted of the 3-level inverters and are connected in parallel, the same effect as in Embodiment 1 can be achieved by suppressing a cross current.

[0170]

[Embodiment 10]

In Embodiments 1 to 9, a plurality of inverter units are connected in parallel in order to achieve large capacity, and output currents from the respective inverter units are equalized. In this method, values of the integral amplifiers I1 to I4 are updated through several switching operations so that a variation in a switching operation timing caused by a difference in a switching element characteristic or a difference in a transmission path of the gate signal is corrected, and thus cross current suppression control is performed.

[0171]

However, since, when the power conversion circuit is initially operated, the extent of a variation in a timing of a switching operation cannot be known, there is a concern that a cross current may increase during a period of several cycles from an initial switching operation until cross current suppression control is completed by updating values of the integral amplifiers I1 to I4. As a countermeasure therefor, there is a method in which sizes of the cross current suppression reactors L1 to LN are increased, or a margin is given to the rating of the inverter unit, but new problems occur, such as an increase in cost of a component, a large-sized reactor, and an increase in the weight.

[0172]

PTL 5 discloses a method in which an operation timing difference of a switching element is corrected by correcting an emitter potential of a gate driving circuit. In this method, since an emitter potential corresponding to a variation is set through a pre-test or by referring to a switching element characteristic from a data sheet, cross current suppression control can be performed even in an initial switching operation. However, a delay difference on a transmission path from the control circuit to the gate driving circuit, or a delay difference in the gate driving circuit itself is not taken into consideration, and in a case where such a delay difference is great, a cross current increases due to the initial switching operation.

[0173]

In the method disclosed in PTL 4, a delay amount of a gate signal is set in advance, and an operation timing difference of the switching element is corrected. In this method, if a test is performed in consideration of a transmission path difference or a delay difference in the gate driving circuit itself in advance, a cross current can be suppressed in an initial switching operation even in a situation in which an influence thereof is great. However, a method of setting a delay amount is not disclosed, and in a case where a delay amount is manually adjusted, time is taken,

and thus the delivery date is delayed or cost increases.

[0174]

In addition, PTLs 4 and 5 do not take into consideration a characteristic variation of a circuit constituent component due to the passage of time, and if the characteristic variation occurs, a delay amount is required to be measured again. In addition, since control using feedback is not performed, a case where characteristics of the circuit constituent component are changed due to a temperature change during operation of the power conversion circuit cannot be handled.

[0175]

It is mentioned in [Technical Problem] of PTL 6 that a gate voltage increases over 15 V in normal use in a case where a short-circuit current flows through an IGBT, and thus a collector current of the IGBT increases. In a method disclosed in PTL 6, in a case where an abnormal current which exceeds a rating value flows through a switching element, a gate voltage of the element is clamped by using a zener diode so as to prevent an increase in the abnormal current. However, a method in which a gate voltage is set to be lower than in normal times only in a test operation in which an initial value of an integral amplifier is set, and a passing current of the switching element is suppressed to a value which is lower than the rating value.

[0176]

In a method disclosed in PTL 7, if overcurrent of a load

is detected, a gate voltage of a switching element is reduced so as to enter a current limiting state after a delay time has elapsed by a certain circuit configuration, and a load current is reduced in an overcurrent protection state. However, a separate current detection circuit is necessary. In addition, in PTL 7, a resistor is used to detect a current, and thus a loss increases. Further, since a gate terminal of the switching element is capacitive, it takes time to reduce a gate voltage which temporarily increases, and thus there is a problem in that delay occurs until protection becomes effective after detecting the overcurrent.

[0177]

Fig. 14 illustrates a main circuit of a power circuit in which inverter units are connected in parallel in Embodiment 10, Fig. 15 illustrates a cross current suppression control block for each phase of the inverter unit in Embodiment 10, and Fig. 16 illustrates an initial value determination block which determines initial values of the integral amplifiers I1 and I3 illustrated in Fig. 15.

[0178]

In Embodiment 10, three inverter units 1 to 3 are provided, and a switch SW1 is inserted between a power conversion circuit and a load or a system power supply. In addition, the initial value determination block 33 illustrated in Fig. 16 is assumed to obtain appropriate initial values of the integral amplifiers

I1 and I3 for each of the three inverter units 1 to 3 which are provided for each phase.

[0179]

As illustrated in Fig. 15, Embodiment 10 is obtained by modifying the cross current suppression control block of Embodiment 1 as follows.

[0180]

Reset input terminals I1a to I4a to which a reset command is input, and initial value input terminals I1b to I4b to which an initial value is input, are additionally provided to the integral amplifiers I1 to I4. In the integral amplifiers I1 to I4, if "1" is input to the reset input terminal I1a, values which are integrated in the integral amplifiers I1 to I4 are changed to an input value to the initial value input terminal I1b.

[0181]

It is assumed that a delay adjustment mode signal has a value of "0" if the inverter unit of the power conversion circuit which starts to operate is used in a normal operation except for a test operation for obtaining initial values of the integral amplifiers I1 to I4, and has a value of "1" in the test operation for obtaining appropriate initial values of the integral amplifiers I1 to I4 of the cross current suppression control block.

[0182]

A switch SWA is connected to a lower side if the delay adjustment mode signal has a value of "1", a delay process on the gate command Gref is bypassed, and thus the gate command value Gref is input to the dead-time processor 24 without being changed.

[0183]

A buffer 46 delays the delay adjustment mode signal by one calculation time.

[0184]

An AND element AND5 receives an inversion signal of the delay adjustment mode signal and an output signal from the buffer 46.

[0185]

The output signal from the AND element AND5 has a value of "1" when a value of the delay adjustment mode signal changes from "1" to "0", and this signal is input to the reset input terminals I1a to I4a of the integral amplifiers I1 to I4.

[0186]

Next, the initial value determination block 33 will be described with reference to Fig. 16.

[0187]

Noise is removed from current detection values IinvU1det, IinvU2det and IinvU3det of the respective inverter units 1 to 3 in filters 34a, 34b and 34c, and slopes of the inverter unit current detection values IinvU1det to IinvU3det are calculated

in differentiators sT. Differentiation results therein are compared with a threshold value β which is set in advance in comparators 35a, 35b and 35c. If the differentiation result is greater than the threshold value β, "1" is output, and if the differentiation result is equal to or smaller than the threshold value β, "0" is output.

[0188]

Since the delay adjustment mode signal has a value of "1" during the test operation in which the initial value determination block 33 operates, gate signals Gu1, Gu2 and Gu3 are common signals having undergone a dead-time process without being changed without performing a delay process on the gate command value Gref.

[0189]

AND elements AND6, AND8 and AND10 respectively receive the gate signals Gu1, Gu2 and Gu3 and inversion signals of the output signals from the comparators 35a, 35b and 35c. In addition, if the gate signals Gu1, Gu2 and Gu3 have a value of "1", and differentiation results of the inverter unit current detection value IinvU1det, IinvU2det and IinvU3det are equal to or smaller than the threshold value β, "1" is output, and, otherwise, "0" is output.

[0190]

AND elements AND7, AND9 and AND11 respectively receive inversion signals of the gate signals Gu1, Gu2 and Gu3 and the

output signals from the comparators 35a, 35b and 35c. In addition, if the gate signals Gu1, Gu2 and Gu3 have a value of "0", and differentiation results of the inverter unit current detection value IinvU1det, IinvU2det and IinvU3det are greater than the threshold value β, "1" is output, and, otherwise, "0" is output.

[0191]

Counters 36a to 36f measure time when the AND elements AND6 to AND11 output "1", and output the measured time.

[0192]

A maximum value calculator MAX receives the outputs from the counters 36a, 36c and 36e, and outputs the maximum value of the received values. In addition, subtractors sub1, sub3 and sub5 subtract the maximum value from the output values from the counters 36a, 36c and 36e, respectively.

[0193]

The output values from the subtractors sub1, sub3 and sub5 are used as initial values of the integral amplifiers I1 of the inverter units 1 to 3, and are input to the initial value input terminals I1b to I4b of the corresponding integral amplifiers I1.

[0194]

Multipliers mu3, mu4 and mu5 multiply the outputs from the counters 36b, 36d and 36f by -1. A minimum value calculator MIN receives outputs from the multipliers mu3, mu4 and mu5,

and outputs the minimum value of the received values. In addition, subtractors sub2, sub4 and sub6 subtract the minimum value from the outputs from the multipliers mu3, mu4 and mu5, respectively.

[0195]

Output values from the subtractors sub2, sub4 and sub6 are used as initial values of the integral amplifiers I3 of the inverter units 1 to 3, and are input to the initial value input terminals I3b of the corresponding integral amplifiers I3.

[0196]

Embodiment 10 realizes a method in which, during a test operation for obtaining an initial value of the integral amplifier, a test of turning off the switching elements Tu1 to Tu3 and Tx1 to Tx3 is performed by using the cross current suppression reactors L1, L2 and L3 which are respectively connected to the inverter units 1, 2 and 3, delay time from inputting of the gate command value Gref to actual operation of the switching elements Tu1 to Tu3 and Tx1 to Tx3 is measured, and initial values of the integral amplifiers I1 to I4 are determined.

[0197]

As preparation, the switch SW1 is turned off in the main circuit illustrated in Fig. 14 so that the power conversion circuit is disconnected from the load or the system power supply,

and thus the turning-off test does not influence the outside of the power conversion circuit. However, there is a case where the turning-off test can be performed without providing the switch SW1, for example, in a case of a three-phase three-wire type, a change in a phase voltage for a single phase does not influence the outside.

[0198]

Fig. 17 illustrates operation waveforms for obtaining initial values of the integral amplifiers I1 and I3 of the inverter unit 1. First, the gate signal Gx2 is set to "1", and thus the switching element Tx2 is turned on. Next, a pulse-ON command is set in the gate signal Gu1. Then, an inverter direct current voltage is applied to the cross current suppression reactors L1 and L2, and the output current IinvU1 from the inverter unit 1 starts to increase with a specific slope after a delay time due to a reactance component of the main circuit. Here, a differentiation result of the output current detection value IinvU1det of the inverter unit 1 is detected by the differentiator sT, and it is determined whether or not the differentiation result exceeds the threshold value β in the comparator 35a.

[0199]

The counter 36a measures time after the gate signal Gu1 is set as the ON command until the differentiation result of the output current detection value IinvU1det of the inverter

unit 1 exceeds the threshold value β, and outputs the measured time. This time is a delay amount of turning-on of the switching element Tu1, and indicates to what extent rising of the gate signal Gu1 is advanced.

[0200]

The counter 36b measures time after the gate signal Gu1 is set as an OFF command until the differentiation result of the output current detection value IinvU1det of the inverter unit 1 is equal to or smaller than the threshold value β, and outputs the measured time. This time is a delay amount of turning-off of the switching element Tu1, and indicates to what extent falling of the gate signal Gu1 is advanced.

[0201]

On the other hand, in Fig. 15, the output from the integral amplifier I1 is multiplied by -1, and is input to a rising delay adder DelayU. Since there is no inputting a negative value to the rising delay adder DelayU in order to advance the gate command value Gref through predication of a future, a positive value is necessarily input thereto. Therefore, the maximum value of delay amounts of the switching elements Tu1, Tu2 and Tu3 are selected, the maximum value is subtracted from output values of the counters 36a, 36c and 36e, and thus an initial value of the integral amplifier I1 corresponding to the switching element whose delay amount is the maximum is set to "0".

[0202]

Consequently, the gate command value Gref for the switching element whose delay amount is the maximum is not corrected, delay is added to the gate command value Gref for the switching elements whose delay amounts are not the maximum, and thus switching operations are performed at the same timing.

[0203]

This is also the same for the integral amplifier I3. The outputs from the counters 36b, 36d and 36f indicate to what extent falling of the gate signal Gu1 is advanced, but an output from the integral amplifier I3 is required to indicate to what extent falling is delayed, and thus the outputs from the counters 36b, 36d and 36f are multiplied by -1. Next, a delay amount is adjusted in the same manner as in the integral amplifier I1 so that the gate command value Gref for the switching element whose delay amount is the maximum is not corrected.

[0204]

Fig. 18 illustrates a series of operation waveforms for obtaining initial values of the integral amplifiers I1 and I3 of each of the inverter units 1 to 3. First, the gate signal Gx2 is set to "1", and thus the switching element Tx2 is turned on. Next, a pulse-ON command is set in the gate signal Gu1. A delay time from rising of the gate signal Gu1 until the inverter unit current detection value IinvU1 starts to increase,

and a delay from falling of the gate signal Gu1 to the time when the inverter unit current detection value IinvU1 stops increasing, are measured. Thereafter, the gate signal Gx2 is set to 0 so as to turn off the switching element Tu2, and the inverter unit current detection value IinvU1 decreases.

[0205]

If the output current detection value IinvU1 of the inverter unit 1 becomes zero, the gate signal Gx3 is set to 1, a pulse-ON command is set in the gate signal Gu2, and delay is measured in the same manner. This is repeatedly performed on the remaining inverter units, and delay is measured.

[0206]

In Fig. 18, the measurement is performed from the inverter unit 1, but an order of the measurement may be changed. In addition, the switching element Tx2 is turned on when delay characteristics of the switching element Tu1 are measured, but, alternatively, the switching element Tx3 may be turned on.

[0207]

By performing the above-described operation, if the switch SW1 has only to be turned off during a test operation for obtaining an initial value of the integral amplifier in advance, it is possible to measure delay characteristics of each switching element, also including characteristics of the gate driving circuit, without reconfiguration of the main circuit or preparation of an additional component. In

addition, automation is performed through sequence control, it is possible to reduce time of a test operation for obtaining an initial value. Further, even if an element, a current detector, or the like is exchanged, it is possible to immediately measure delay characteristics by performing a test operation.

[0208]

In Embodiment 10, a description has been made of a method of obtaining initial values of only the integral amplifiers I1 and I3 for a single phase, but initial values can be obtained in the same for the integral amplifiers I2 and I4, and initial values can be sequentially obtained for the other phases.

[0209]

As mentioned above, according to Embodiment 10, gate delay characteristics of the inverter unit are measured in advance so that an initial value of the integral amplifier is set, and thus it is possible to suppress a cross current right after the power conversion circuit starts to operate.

[0210]

In addition, if the power conversion circuit has only to be disconnected from the system or the load by using the switch SW1, it is possible to perform a test operation. Since the cross current suppression reactors L1 to L3 of the respective inverter units 1 to 3 are used as loads required in the test operation, other separate loads are not required

to be prepared, it is not necessary to manually change a circuit, and a test time can be reduced.

[0211]

Further, since delay characteristics are automatically measured, it is possible to reduce a test operation time for obtaining an initial value and thus to promptly handle even changes in delay characteristics due to exchange of an electrode, a current detector, or the like.

[0212]

[Embodiment 11]

Fig. 19 illustrates a control block of the initial value determination block 33 in Embodiment 11. The current detectors CTU1 to CUT3 are attached to the respective inverter units 1 to 3, and an error may be generated in a measured delay time due to personal differences of the current detectors CTU1 to CUT3. Embodiment 11 is characterized in that the same current detector CTU1 is used to detect delay.

[0213]

The initial value determination block 33 has the same configuration as that in Embodiment 10 in relation to the inverter unit 1. However, the output current detection value IinvU1det of the inverter unit 1 is also used to detect delay times of the inverter units 2 and 3.

[0214]

Only IinvU1det is used as an inverter unit current

detection value. In addition, a comparator 35d which detects that a differentiation result of the output current detection value IinvU1det of the inverter unit 1 is smaller than a threshold value -β is additionally provided.

[0215]

An AND element AND8 outputs "1" when the gate signal Gu2 has a value of "1", and a differentiation result of the output current detection value IinvU1det of the inverter unit 1 is equal to or greater than the threshold value -β. An AND element AND9 outputs "1" when the gate signal Gu2 has a value of "0", and a differentiation result of the output current detection value IinvU1det of the inverter unit 1 is smaller than the threshold value -β.

[0216]

An AND element AND10 outputs "1" when the gate signal Gu3 has a value of "1", and a differentiation result of the output current detection value IinvU1det of the inverter unit 1 is equal to or greater than the threshold value -β. An AND element AN11 outputs "1" when the gate signal Gu3 has a value of "0", and a differentiation result of the output current detection value IinvU1det of the inverter unit 1 is smaller than the threshold value -β.

[0217]

Fig. 20 illustrates a series of operation waveforms for obtaining initial values of the integral amplifiers I1 and I3

of each of the inverter units 1 to 3. In relation to the inverter unit 1, in the same manner as in Embodiment 10, a delay time from a change in the gate signal until a differentiation result of the inverter unit output current detection value changes is measured. Then, the gate signal Gx1 is set to 1 so as to turn on the switching element Tx1, and delay times of the inverter units 2 and 3 are measured. If the switching element Tu2 is turned on in a state in which the switching element Tx1 is turned on, the output current IinvU1 of the inverter unit 1 starts to flow in a negative direction. A a differentiation result of the output current detection value IinvU1det of the inverter unit 1 is compared with the threshold value $-\beta$ by the comparator 35d, and thus a rising delay time of the switching element Tu2 is measured. A falling delay time may be measured in the same manner. Then, the switching element Tx1 is temporarily turned off so as to prompt reduction of a current. If a current detection value becomes zero, the switching element Tx1 is turned on, and a delay time of the remaining inverter unit 3 is measured.

[0218]

In this method, delay times are measured by the same current detector CTU1, and thus measurement errors due to personal differences of the current detectors CTU1 to CUT3 can be removed.

[0219]

As mentioned above, according to Embodiment 11, gate delay characteristics can be measured in a state of removing errors of delay times due to personal differences of the current detectors CTU1 to CUT3, and thus it is possible to further reduce a cross current right after the power conversion circuit starts to operate.

[0220]

[Embodiment 12]

Fig. 21 illustrates a main circuit of a power conversion circuit in which inverter units are connected in parallel to each other in Embodiment 12. In the main circuit of the power conversion circuit in which the inverter units are connected in parallel to each other in Embodiment 12, a system power supply is assumed to be connected to a connection point on the AC side, and the power conversion circuit is provided with a precharge circuit 37 of an inverter direct current voltage, constituted of a switch SW2 and a resistor R. The precharge circuit 37 belongs to a general well-known technique, and thus detailed description thereof will be omitted here.

[0221]

Fig. 22 illustrates a precharge circuit control block which generates a command for the switch SW2 of the precharge circuit 37.

[0222]

In the precharge circuit control block, a comparator 38a

compares the present direct current voltage detection value Vdc of the power conversion circuit, which is detected by a voltage detector (not illustrated) or the like with a preset threshold value γ1. In addition, a comparator 38b compares the direct current voltage detection value Vdc of the power conversion circuit with a preset threshold value γ2. Here, γ1 > γ2. In addition, the delay adjustment mode signal has the same determination condition as in Embodiment 10.

[0223]

An AND element AND12 outputs "1" when Vdc>2, and the delay adjustment mode signal has a value of "1".

[0224]

An AND element AND13 outputs "1" so as to output an ON command to the switch SW2 when a precharge start command has a value of "1", Vdc>γ1 is not established, and the AND element AND12 outputs "0".

[0225]

An AND element AND14 outputs "1" so as to output an ON command to the switch SW1 when Vdc>γ1, and the delay adjustment mode signal has a value of "0".

[0226]

In addition, the initial value determination block 33 employs the same circuit as that used in Embodiment 10 illustrated in Fig. 16.

[0227]

In a case where sizes of the cross current suppression reactors L1 to L3 are small, an output current exceeds an element rating even if a pulse width of an ON command for the switching element is reduced when delay characteristics are measured during a test operation, and thus there is a concern that the switching element may be thermally damaged. Embodiment 12 realizes a method in which a direct current voltage is lowered during measurement of delay characteristics, and thus the delay characteristics can be measured without destroying the switching element despite the small-sized cross current suppression reactors L1 to L3.

[0228]

A description will be made of a switch command generation block of the precharge circuit illustrated in Fig. 22. During a normal operation other than a test operation, the "delay adjustment mode signal" has a value of "0". If a precharge start command is input in a state in which $Vdc \leq \gamma 1$ and AND12="0", the switch SW2 is turned on, and thus charging is started. Then, if the inverter direct current voltage Vdc exceeds the threshold value $\gamma 1$, the comparator 38a outputs "1", and thus the AND element AND13 outputs "0" so as to turn off the switch SW2. In addition, the comparator 38a outputs "1" at $Vdc > \gamma 1$, and the AND element AND14 outputs 1 so as to turn on the switch SW1 if the delay adjustment mode signal has a value of "0", and thus preparation for an operation is completed.

[0229]

In the test operation for measuring a delay time, the "delay adjustment mode signal" has a value of "1". If the precharge start command is input in this state, the AND element AND12 outputs "0" because of $Vdc<\gamma 2$, the comparator 38a outputs "0" because of $Vdc<\gamma 1$, and thus the AND element AND13 outputs "1" so as to turn on the switch SW2 in the same manner. Therefore, charging is started. However, since the AND element AND12 outputs "1" in a state in which the inverter direct current voltage Vdc exceeds the threshold value $\gamma 2$, the switch SW2 is turned off, and the switch SW1 is also in a turned-off state.

[0230]

Consequently, the precharge can be stopped on the way, and thus a delay time can be measured in a state in which the inverter direct current voltage Vdc is low.

[0231]

In this method, the inverter direct current voltage Vdc may vary during measurement of a delay time. However, since a characteristic which has a great influence on the inverter direct current voltage Vdc is a differentiation result of an output current, a measurement result of the delay time is not influenced much. In addition, the comparators 38a and 38b may have any hysteresis characteristic, and the variation in the inverter direct current voltage Vdc may be suppressed within

a certain range by turning on the switch SW2 again so that recharging is performed.

[0232]

As mentioned above, according to Embodiment 12, in addition to the operation and effect of Embodiment 10, since delay characteristics are measured by lowering the inverter direct current voltage Vdc even under a condition in which the cross current suppression reactors L1 to L3 have small sizes, it is possible to prevent the switching elements Tu1 to Tu3 and Tx1 to Tx3 from being destroyed.

[0233]

[Embodiment 13]

Fig. 23 is a circuit configuration diagram illustrating a gate driving circuit of a switching element in Embodiment 13. Fig. 23 illustrates only a gate driving circuit of the switching element Tx2 as a representative. This circuit is modified as follows when compared with a general gate driving circuit.

[0234]

As positive side power supplies, power supplies which output difference voltages Va and Vb are used. Here, Va>Vb is assumed.

[0235]

A switch SW3 is turned on when the power conversion circuit is in normal use other than a test operation for

determining initial values of the integral amplifiers I1 to I4. A switch SW4 is turned on when an operation of the inverter is a test operation for obtaining appropriate initial values of the integral amplifiers I1 to I4 in the cross current suppression control block 33.

[0236]

Fig. 24 illustrates an initial value determination block of Embodiment 13, and a magnitude condition of the output current detection values IinvU1det, IinvU2det and IinvU3det of the inverter units 1 to 3 is added to the condition in which the counters 36a to 36f operate. Remaining configurations are the same as those in Embodiment 10.

[0237]

Comparators 39a, 39b and 39c detect that the output current detection values IinvU1det, IinvU2det and IinvU3det of the inverter units 1 to 3 are greater than a preset current threshold value Ith1.

[0238]

Comparators 40a, 40b and 40c detect that differentiation results in the differentiators sT are greater than a threshold value $-\beta$.

[0239]

In addition, operations of the AND elements AND6 to AND11 are modified as follows when compared with Embodiment 10.

[0240]

The AND element AND6 outputs "1" when the gate signal Gu1 has a value of "1", the output current detection value IinvU1det of the inverter unit 1 is equal to or smaller than the current threshold value Ith1, and a differentiation result of IinvU1det is equal to or smaller than the threshold value β.

[0241]

The AND element AND7 outputs "1" when the gate signal Gu1 has a value of "0", the output current detection value IinvU1det of the inverter unit 1 is greater than the current threshold value Ith1, and a differentiation result of output current detection value IinvU1det of the inverter unit 1 is greater than the threshold value -β.

[0242]

The AND element AND8 outputs "1" when the gate signal Gu2 has a value of "1", the output current detection value IinvU2det of the inverter unit 2 is equal to or smaller than the current threshold value Ith1, and a differentiation result of the output current detection value IinvU2det of the inverter unit 2 is equal to or smaller than the threshold value β.

[0243]

The AND element AND9 outputs "1" when the gate signal Gu2 has a value of "0", the output current detection value IinvU2det of the inverter unit 3 is greater than the current threshold value Ith1, and a differentiation result of output

current detection value IinvU2det of the inverter unit 3 is greater than the threshold value -β.

[0244]

The AND element AND10 outputs "1" when the gate signal Gu3 has a value of "1", the output current detection value IinvU3det of the inverter unit 3 is equal to or smaller than the current threshold value Ith1, and a differentiation result of the output current detection value IinvU3det of the inverter unit 3 is equal to or smaller than the threshold value β.

[0245]

The AND element AND11 outputs "1" when the gate signal Gu3 has a value of "0", the output current detection value IinvU3det of the inverter unit 3 is greater than the current threshold value Ith1, and a differentiation result of output current detection value IinvU3det of the inverter unit 3 is greater than the threshold value -β.

[0246]

In the same manner as in Embodiment 12, Embodiment 13 also realizes a method in which an initial value of the integral amplifier can be obtained and a delay time can be measured without destroying the switching element despite the small-sized cross current suppression reactors L1 to L3. Embodiment 13 realizes a method in which voltage drop of the switching element is increased by lowering a positive side voltage of the gate driving circuit, and thus an output current

from each inverter unit is suppressed.

[0247]

A description will be made of the gate driving circuit illustrated in Fig. 23. Here, it is assumed that Va is higher than Vb, and the power supply voltage Va is a general gate driving voltage (for example, about 15 V) of an IGBT. In the power conversion circuit in a normal operation other than a test operation, the switch SW3 is turned on, and, during measurement of a delay time, the switch SW4 is turned on. As a characteristic of the IGBT, if a gate voltage is reduced, voltage drop rapidly increases when an IGBT passing current is greater than a certain value. By using such an IGBT element characteristic, an output current of the inverter unit is prevented from increasing during measurement of a delay time, and thus the switching element is protected from overcurrent.

[0248]

Fig. 25 illustrates operation waveforms for obtaining initial values of the integral amplifiers I1 and I3 of the inverter unit 1 in Embodiment 13.

[0249]

The gate signal Gx2 is set to "1", and thus the switching element Tx2 is turned on, but, at this time, the gate driving circuit of the switching element Tx2 turns on the switch SW4 so that a positive gate driving voltage is set to the voltage Vb which is lower than a general value. In this state, a

pulse-ON command is set in the gate signal Gu1. However, the gate driving circuit of the measurement target switching element Tu1 turns on the switch SW3 so as to set a positive gate driving voltage to Va, and thus the same condition as in a normal operation other than a test operation is caused. This is because, if the gate driving voltage is lowered, a switching operation time increases, and thus a delay time cannot be accurately measured.

[0250]

If the switching element Tu1 is turned on, when the output current IinvU1 of the inverter unit 1 increases but reaches a certain magnitude, voltage drop of the switching element Tx2 rapidly increases, and thus the output current IinvU1 of the inverter unit 1 stops increasing.

[0251]

The output current IinvU1 of the inverter unit 1 passes not through the switching element Tx2 but through the reverse parallel diode connected to the switching element Tu2. In this case, as illustrated in Fig. 25, the counter 36a measures time after the gate signal Gu1 has a value of "1" until the output current detection value IinvU1det of the inverter unit 1 starts to increase. If the output current IinvU1 of the inverter unit 1 stops increasing, the gate signal Gx2 is set to "0" so as to turn off the switching element Tx2.

[0252]

Then, the gate signal Gu1 is set to "0" so as to turn off the switching element Tu1. Therefore, the output current IinvU1 of the inverter unit 1 starts to decrease. The counter 36b measures time after the gate signal Gu1 has a value of "0" until the output current detection value IinvU1det of the inverter unit 1 starts to decrease.

[0253]

The above description relates to a case where delay characteristics of the switching element Tu1 are measured. In a case of measuring delay characteristics of the switching elements Tx1, Tx2 and Tx3, the switch SW4 of the gate driving circuit of each of the switching elements Tu1, Tu2 and Tu3 is required to be turned on so as to lower the positive side gate voltage, and the switch SW3 is required to be turned on so that the positive gate voltage of each of the switching elements Tx1, Tx2 and Tx3 is set to be the same value as in a normal operation other than a test operation.

[0254]

In Fig. 23, a separate power supply for a turning-off test is prepared as the voltage Vb for measuring a delay time, but a voltage obtained through voltage-division of a resistor or a zener diode of the power supply Va may be used as the power supply Vb. The switching element Tx2 may be turned on at all times during measurement of a delay time of the switching element Tu1, and since switching of the switching element Tx2

is performed when a current is zero, there is no problem even if time is taken for the switching operation of the switching element Tx2. For this reason, a resistor having a great value can be used as a resistor used for voltage division, and thus it is possible to minimize heat generation of a component of the gate driving circuit.

[0255]

If a passing current of the switching element increases, the gate driving circuit is charged when voltage drop (voltage saturation between an emitter and a collector) Vce(sat) of the switching element rapidly increases, but if a value of a resistor used to divide the power supply Va is too great, a charging speed of the gate driving circuit is higher than a discharging speed, thus the gate voltage increases, and therefore a current reduction effect deteriorates. The gate voltage may be set to a lower value in consideration of this.

[0256]

As mentioned above, according to Embodiment 13, the same operation and effect as in Embodiment 10 can be achieved, and the following operation and effect can also be achieved.

[0257]

Since the gate voltage is lowered so as to increase voltage drop of the switching element, and thus a delay time is measured, even under a condition in which the cross current suppression reactors L1 to L3 have small sizes, an increase

in a passing current of the switching element is minimized, and thus it is possible to prevent the switching element from being destroyed.

[0258]

In addition, the gate voltage Vb for measuring a delay time may be prepared by dividing a voltage with a resistor or a zener diode. Therefore, the number of components is smaller than in a case where a power supply is separately provided, and thus it is possible to reduce cost.

[0259]

Further, since the gate voltage is low from the beginning during the turning-off test, there is no delay due to a control operation, and the switching element can be reliably protected, when compared with a method in which the gate voltage is lowered after overcurrent is detected.

[0260]

[Embodiment 14]

Fig. 26 illustrates a block which determines a frequency (a carrier frequency fc) of the carrier triangular wave Vcarry for each phase in Embodiment 14. In Embodiment 14, the following elements are added.

[0261]

A comparator 41a compares the total output current detection value IinvUdet of the inverter units with a preset current threshold value Ith2, and outputs "1" when the total

output current detection value IinvUdet of the inverter units is greater than the current threshold value Ith2. A comparator 41b compares the total output current detection value IinvUdet of the inverter units with a current threshold value -Ith2, and outputs "1" when the total output current detection value IinvUdet of the inverter units is smaller than the current threshold value -Ith2.

[0262]

An AND element AND15 receives an operation command signal for the power conversion circuit and the output signal from the comparator 41a, and outputs "1" when there is the operation command signal, and the output signal from the comparator 41a is true. An AND element AND16 receives the operation command signal for the power conversion circuit and the output signal from the comparator 41b, and outputs "1" when there is the operation command signal, and the output signal from the comparator 41b is true.

[0263]

An OR element OR1 outputs "1" when the AND element AND15 outputs "1", or a buffer 45a outputs 1. An OR element OR2 outputs "1" when the AND element AND16 outputs "1", or a buffer 45b outputs 1. The outputs from the OR elements OR1 and OR2 are respectively stored in the buffers 45a and 45b.

[0264]

Time counters 42a and 42b respectively measure time

periods after the outputs from the OR elements OR1 and OR2 are "1", and output the measured time periods as times t1 and t2.

[0265]

Comparators 43a and 43b output "1" when the times t1 and t2 are greater than 0 and are equal to or smaller than a preset threshold value (here, designated as one cycle 1/fc of the carrier frequency).

[0266]

An OR element OR3 outputs "1" when at least one of the outputs from the comparators 43a and 43b is "1". A switch SW5 is connected to an upper side if the output from the OR element OR3 is "0", so that the carrier frequency fc in normal times is output. The switch SW5 is connected to a lower side if if the output from the OR element OR3 is "0", so that a carrier frequency (here, 4fc which is four times higher than the carrier frequency fc) higher than in normal times is output.

[0267]

An oscillator 44 receives the frequency output from the switch SW5 as a frequency command, and outputs the carrier triangular wave Vcarry with the frequency of the command. The carrier triangular wave Vcarry output from the oscillator 44 is input to, for example, the PWM block 21 or the peak detection block 22 illustrated in Fig. 15.

[0268]

Embodiment 14 realizes a method in which the power

conversion circuit starts to operate without performing a test operation, the carrier frequency fc is increased at the time when the total output current IinvU of the inverter units initially increases after the operation, and thus time taken for the cross current suppression control is reduced.

[0269]

First, the total output current IinvU of the inverter units is detected, and is compared with the current threshold values Ith2 and -Ith2. Typically, the current threshold values Ith2 and -Ith2 are zero, and the carrier frequency fc is increased at the same time as the start of an operation of the power conversion circuit. However, in a case where the total output current IinvU of the inverter units is small and thus the cross current suppression control is stopped as in Embodiment 6, the carrier frequency fc is required to be increased after the total output current of the inverter units increases. In this case, if the current threshold values Ith2 and -Ith2 are set to a value obtained by dividing, for example, the rating current by the number of inverter units, the inverter unit is not destroyed even if the total output current IinvU of the inverter units concentrates on a single unit prior to the cross current suppression control.

[0270]

If the total output current IinvU of the inverter units increases, the switch SW5 is connected to the lower side during

one cycle 1/fc of the carrier frequency from that time, and the carrier frequency fc increases to four times, for example. Consequently, since an interval at which a peak of the carrier triangular wave appears becomes 1/4 times, and thus an operation frequency of the gate delay command value calculation block 23 illustrated in Fig. 15 becomes four times, the cross current suppression control is completed at 1/4 of time in a normal operation. Thereafter, a cross current can be suppressed in a state in which the cross current suppression control is completed.

[0271]

However, if a direction of the total output current IinvU of the inverter units is reversed, a turned-on switching element is changed, and cross current suppression control related to delay characteristics corresponding to the switching element is not completed. For this reason, if the total output current IinvU of the inverter units increases in the reversed direction, the carrier frequency is increased again so as to prompt a reduction in cross current suppression control time. In Fig. 26, both cases where a sign of the total output current detection value IinvUdet of the inverter units is positive and negative are confirmed.

[0272]

In Embodiment 14, since the carrier frequency fc is temporarily increased, a switching loss increases. However,

currents flowing through the inverter units 1 to 3 are almost zero, and thus a loss is insignificant and the switching element is cold before the carrier frequency fc is increased, the carrier frequency fc is increased for a short time period, and the total output current IinvU of the inverter units is smaller than the rating current at this time. Therefore, the inverter units 1 to 3 constituted of the switching element which resist to heating do not fail.

[0273]

In addition, in Embodiment 14, different carrier triangular waves Vcarry are used for each phase. However, if there is a margin in the heat duty, the same carrier triangular wave Vcarry for three phases may be used, the carrier frequency fc for all the three phases may be increased when the total output current IinvU of the inverter units for any one of the three phases increases.

[0274]

In Embodiment 14, since reset means of the buffers 45a and 45b which hold outputs from the OR elements OR1 and OR2 is not provided, if the carrier frequency fc is temporarily increased, the carrier frequency fc is not required to be increased again thereafter even in a case where the total output current IinvU of the inverter units decreases or the power conversion circuit is stopped. This is because the integral amplifiers I1 to I4 of the gate delay command value calculation

block 23 are obtained only once. Thereafter, since set values of the integral amplifiers I1 to I4 are held even if the power conversion circuit is stopped, the cross current suppression control can be performed next time by using the held set value, and thus the carrier frequency fc is not required to be increased.

[0275]

For example, in a case where the inverter unit is exchanged due to a failure thereof, it is expected that the supply of power to the control circuit is stopped. At this time, values of the integral amplifiers I1 to I4 disappear, but the buffers 45a and 45b which hold outputs from the OR elements OR1 and OR2 are also reset. Therefore, the carrier frequency fc is temporarily increased in a subsequent re-operation, and thus it is possible to reduce time for the cross current suppression control.

[0276]

However, separate reset means may be provided, reset may be performed, for example, when overcurrent is generated, and the cross current suppression control may be prompted during re-operation.

[0277]

As mentioned above, according to Embodiment 14, since time until initial values of the integral amplifiers I1 to I4 are obtained is reduced by increasing the carrier frequency

fc during operation of the power conversion circuit, it is possible to suppress a cross current when a current initially increases after the power conversion circuit starts to operate, and cross current suppression control using a test operation is not necessary.

[0278]

In addition, the carrier frequency fc is increased for a short time period, and when the cross current suppression control is temporarily completed, the carrier frequency fc is not required to be increased again even if the power conversion circuit is stopped. Therefore, a loss in a normal operation is not influenced.

CLAIMS

[Claim 1]

A cross current suppression control device which suppresses a cross current in a power conversion circuit in which inverter units are connected in parallel to a direct current voltage source including a switching element, the cross current suppression control device comprising:

a gate delay command value calculation section that operates once at a half switching cycle so as to calculate a rising gate delay command value and a falling gate delay command value;

a rising delay adding section that adds the rising gate delay command value to a gate command value or a voltage command value; and

a falling delay adding section that adds the falling gate delay command value to the gate command value or the voltage command value,

wherein the rising delay adding section and the falling delay adding section are provided for each phase of each inverter unit,

wherein the gate delay command value calculation block includes

a proportional amplifier that multiplies a deviation between an inverter unit output current command value and an inverter unit output current detection value by a gain,

the deviation being obtained as a cross current;

an integral amplifier to which the cross current is input by a first switch which is turned on whenever each switching element is turned on or off and when a logical result of a sign of the inverter unit output current detection value and a sign of the gate command value is true; and

a second switch that receives a signal from the integral amplifier and is turned on by the sign of the inverter unit output current detection value, and

wherein outputs from the proportional amplifier and the second switch are added together, and thus the rising gate delay command value and the falling gate delay command value are output.

[Claim 2]

A cross current suppression control device which suppresses a cross current in a power conversion circuit in which inverter units are connected in parallel to a direct current voltage source, the cross current suppression control device comprising:

a gate delay command value calculation section that operates once at a half switching cycle so as to calculate a rising gate delay command value and a falling gate delay command value;

a rising delay adding section that adds the rising gate delay command value to a gate command value or a voltage command

value; and

a falling delay adding section that adds the falling gate delay command value to the gate command value or the voltage command value,

wherein the rising delay adding section and the falling delay adding section are provided for each phase of each inverter unit,

wherein the gate delay command value calculation block includes

a proportional amplifier that multiplies a deviation between an inverter unit output current command value and an inverter unit output current detection value by a gain, the deviation being obtained as a cross current;

an integral amplifier that is provided so as to correspond to each switching element and to which the cross current is input by a first switch which is operated by the sign of the inverter unit output current detection value; and

a second switch that receives a signal from the integral amplifier and is operated by the sign of the inverter unit output current detection value, and

wherein outputs from the proportional amplifier and the integral amplifier are added together, and thus the rising gate delay command value and the falling gate delay command value are output.

[Claim 3]

The cross current suppression control device according to claim 1 or 2, wherein, when an absolute value of the cross current is equal to or smaller than a set value, the proportional amplifier outputs zero, and the integral amplifier stops being updated, and

wherein, when the absolute value of the cross current is equal to or greater than the set value, a value obtained by subtracting the set value from the absolute value is input to the proportional amplifier and the integral amplifier.

[Claim 4]

The cross current suppression control device according to any one of claims 1 to 3, wherein the inverter unit output current command value is a value obtained by dividing an inverter output current detection value by the number of inverter units.

[Claim 5]

The cross current suppression control device according to any one of claims 1 to 3, wherein the inverter unit output current command value is an output current detection value of another certain inverter unit.

[Claim 6]

The cross current suppression control device according to any one of claims 1 to 5, wherein, when the inverter unit output current detection value is equal to or smaller than a set value, the proportional amplifier outputs zero, and the

integral amplifier stops being updated,

wherein, when an absolute value of the inverter output current detection value is equal to or greater than the set value, a value obtained by subtracting the set value from the absolute value is input to the proportional amplifier and the integral amplifier, and

wherein proportional integral calculation is performed so that the deviation between the inverter unit output current command value and the inverter unit output current detection value becomes zero, and a value obtained by adding a proportional integral calculation result and outputs from the proportional amplifier and the integral amplifier together is used as the gate delay command value.

[Claim 7]

The cross current suppression control device according to claim 6, wherein effective values of the inverter unit output current command value and the inverter unit output current detection value are used for the proportional integral calculation.

[Claim 8]

The cross current suppression control device according to claim 6, wherein absolute current mean values per cycle of a fundamental wave of the inverter unit output current command value and the inverter unit output current detection value are used for the proportional integral calculation.

[Claim 9]

The cross current suppression control device according to any one of claims 1 to 8, wherein, when an absolute value of the inverter output current is smaller than a threshold value, the integral amplifier stops being updated.

[Claim 10]

The cross current suppression control device according to any one of claims 1 to 9, wherein the gate delay command value calculation block is operated at a peak of a carrier triangular wave.

[Claim 11]

The cross current suppression control device according to any one of claims 1 to 9, wherein the gate delay command value calculation block is operated when the gate command value changes.

[Claim 12]

The cross current suppression control device according to any one of claims 1 to 11, wherein each of the inverter units is a multi-level inverter.

[Claim 13]

The cross current suppression control device according to any one of claims 1 to 12, wherein the integral amplifier stops being updated in a case where the number of times of switching is not one during a half cycle of the carrier triangular wave.

[Claim 14]

The cross current suppression control device according to any one of claims 1 to 12, wherein a gate command is output without adding delay thereto when an initial value of the integral amplifier starts to be set during a test operation of the power conversion circuit,

wherein, during the test operation of the power conversion circuit, in a state in which a switching element of an inverter unit which is out of a delay time measurement target is turned on, a pulse-ON command is output to a switching element of a delay time measurement target inverter unit, a closed circuit is formed of the two switching elements and a cross current suppression reactor, time after a gate signal is set to an ON state until a differentiation result of the inverter unit current detection value exceeds a threshold value and time after the gate signal is set to an OFF state until the differentiation result of the inverter unit current detection value is equal to or smaller than the threshold value are measured in the delay time measurement target inverter unit, and the measured times are used as initial values of the integral amplifier, and

wherein, when an operation state of the power conversion circuit is changed from the test operation to a normal operation, a value of the integral amplifier is reset, and the initial value is input to the integral amplifier.

[Claim 15]

The cross current suppression control device according to claim 14, wherein, during the test operation of the power conversion circuit, as a current detector used to detect an inverter unit current detection value, a current detector of a specific inverter unit is used in all inverter units.

[Claim 16]

The cross current suppression control device according to any one of claims 1 to 15, wherein, during the test operation of the power conversion circuit, a direct current voltage of the inverter unit is set to be lower than during a normal operation when a delay time is measured.

[Claim 17]

The cross current suppression control device according to any one of claims 1 to 16, wherein, during the test operation of the power conversion circuit, among switching elements other than the turned-on switching element of the delay time measurement target inverter unit, a positive side voltage of a gate driving circuit for a switching element of an inverter unit is lowered, and voltage drop of the switching element is set higher than during the normal operation.

[Claim 18]

The cross current suppression control device according to any one of claims 1 to 13, wherein a PWM carrier frequency is increased in a specific period after the power conversion

circuit starts to operate or a total output current of the inverter units exceeds a current threshold value.