Claims

What is claimed:

1. A method of making a wafer level chip scale package, comprising the steps (a)-(j) in sequence:

(a) providing a temporary wafer level substrate;

(b) forming a wafer level interconnect structure over the temporary wafer level substrate using wafer level processes including at a temperature greater than or equal to 200 degrees C. by,

(i) forming a first insulating layer over a surface of the temporary wafer level substrate, wherein a first surface of the first insulating layer is in direct contact with the surface of the temporary wafer level substrate, and

(ii) forming a first conductive layer in direct contact with a second surface of the first insulating layer opposite the first surface of the first insulating layer after forming the first insulating layer;

(c) disposing a plurality of first semiconductor die over the wafer level interconnect structure;

(d) depositing an underfill material between the first semiconductor die and the wafer level interconnect structure;

(e) depositing a first encapsulant over an entire surface of the wafer level interconnect structure and around the plurality of first semiconductor die;

(f) removing the temporary wafer level substrate while retaining the entire first insulating layer;

(g) forming a plurality of openings through the first insulating layer and exposing a portion of the first conductive layer;

(h) forming an under bump metallization (UBM) layer in the openings to contact the first conductive layer;

(i) forming a second insulating layer in contact with the first surface of the first insulating layer; and

(j) forming a plurality of bumps on the UBM layer,

wherein forming the wafer level interconnect structure further includes forming a third insulating layer over the first conductive layer and the first insulating layer; forming a second conductive layer over the first conductive layer and the third insulating layer; forming a fourth insulating layer over the second conductive layer and the third insulating layer; forming a third conductive layer over the second conductive layer and the fourth insulating layer; and forming a fifth insulating layer over the third conductive layer and the fourth insulating layer; removing a portion of the fifth insulating layer to expose a portion of the third conductive layer and depositing a metal layer in the removed portion of the fifth insulating layer.

2. A method of making a wafer level chip scale package, comprising the steps (a)-(j) in sequence:

(a) providing a temporary wafer level substrate;

(b) forming a wafer level interconnect structure over the temporary wafer level substrate using wafer level processes including at a temperature greater than or equal to 200 degrees C. by,

(i) forming a first insulating layer over a surface of the temporary wafer level substrate, wherein a first surface of the first insulating layer is in direct contact with the surface of the temporary wafer level substrate, and

(ii) forming a first conductive layer in direct contact with a second surface of the first insulating layer opposite the first surface of the first insulating layer after forming the first insulating layer;

(c) disposing a plurality of first semiconductor die over the wafer level interconnect structure;

(d) depositing an underfill material between the first semiconductor die and the wafer level interconnect structure;

(e) depositing a first encapsulant over an entire surface of the wafer level interconnect structure and around the plurality of first semiconductor die;

(f) removing the temporary wafer level substrate while retaining the entire first insulating layer;

(g) forming a plurality of openings through the first insulating layer and exposing a portion of the first conductive layer;

(h) forming a second conductive layer in the openings over the first conductive layer;

(i) forming a plurality of bumps over the second conductive layer; and

(j) forming a second insulating layer in contact with the first surface of the first insulating layer after removing the temporary wafer level substrate;

wherein forming the wafer level interconnect structure further includes forming a third insulating

layer over the first conductive layer and the first insulating layer; forming a second conductive layer over the first conductive layer and the third insulating layer; forming a fourth insulating layer over the second conductive layer and the third insulating layer; forming a third conductive layer over the second conductive layer and the fourth insulating layer; and forming a fifth insulating layer over the third conductive layer and the fourth insulating layer; removing a portion of the fifth insulating layer to expose a portion of the third conductive layer and depositing a metal layer in the removed portion of the fifth insulating layer

3. A method of making a wafer level chip scale package, comprising the steps (a)-(j) in sequence:

providing a temporary wafer level substrate;

forming a wafer level interconnect structure over the temporary wafer level substrate using wafer level processes including,

(a) forming a first insulating layer over a surface of the temporary wafer level substrate, wherein a first surface of the first insulating layer is in direct contact with the surface of the temporary wafer level substrate, and

(b) forming a first conductive layer over a second surface of the first insulating layer opposite the first surface of the first insulating layer after forming the first insulating layer;

(c) disposing a plurality of first semiconductor die over the wafer level interconnect structure to form a wafer;

(d) disposing a second semiconductor die over the plurality of the first semiconductor die;

(e) disposing a third semiconductor die over a first surface of one of the second semiconductor die, wherein the second semiconductor die is interposed between the first semiconductor die and the third semiconductor die;

(f) depositing an encapsulant over the wafer level interconnect structure and over and around the plurality of first semiconductor die, the second semiconductor die and the third semiconductor die;

(g) removing the temporary wafer level substrate while retaining the first insulating layer;

(h) forming a plurality of openings through the first insulating layer and exposing a portion of the first conductive layer after removing the temporary wafer level substrate;

(i) forming a second conductive layer in the openings over the first conductive layer and forming a pluarality of bumps over the second conductive layer; and

(j) singulating the wafer into a semiconductor chip scale package.

4. The method of claim 3, further including forming a portion of the wafer level interconnect structure at a temperature greater than or equal to 200 degrees C.

5. A method of making a wafer level chip scale package, comprising the steps (a)-(j) in sequence:

(a) providing a temporary wafer level substrate;

(b) forming a wafer level interconnect structure over the temporary wafer level substrate using wafer level processes including,

(i) forming a first insulating layer over a surface of the temporary wafer level substrate, wherein the first insulating layer cover an entire portion of the surface of the temporary wafer level substrate, and

(ii) forming a first conductive layer over a second surface of the first insulating layer opposite the first surface of the first insulating layer after forming the first insulating layer;

(c) disposing a plurality of first semiconductor die over the wafer level interconnect structure to form a wafer;

(d) disposing a second semiconductor die over the plurality of the first semiconductor die;

(e) disposing a third semiconductor die over a first surface of one of the second semiconductor die, wherein the second semiconductor die is interposed between the first semiconductor die and the third semiconductor die;

(f) depositing an encapsulant over the wafer level interconnect structure and over and around the plurality of first semiconductor die, the second semiconductor die and the third semiconductor die;

(g) removing the temporary wafer level substrate while retaining the first insulating layer;

(h) forming a plurality of openings through the first insulating layer and exposing a portion of the first conductive layer after removing the temporary wafer level substrate;

(i) forming a second conductive layer in the openings over the first conductive layer and forming a pluarality of bumps over the second conductive layer; and

(j) singulating the wafer into a semiconductor chip scale package.

6. The method of claim 5, further including forming a portion of the wafer level interconnect structure at a temperature greater than or equal to 200 degrees C.