

Semiconductor-on-Insulator SRAM Configured Using Partially-Depleted and Fully-Depleted Transistors

ABSTRACT OF THE DISCLOSURE

A static memory element includes a first inverter having an input coupled to a left bit node and an output coupled to a right bit node. A second inverter has an input coupled to the right bit node and an output coupled to the left right bit node. A first fully depleted semiconductor-on-insulator transistor has a drain coupled to the left bit node, and a second fully depleted semiconductor-on-insulator transistor has a drain coupled to the right bit node.

(FIG. 1)