

MATERIAL PATH ESTABLISHMENT METHOD, MATERIAL SCHEDULING METHOD, AND SEMICONDUCTOR PROCESS EQUIPMENT

TECHNICAL FIELD

[0001] The present disclosure relates to the field of semiconductor technologies, and specifically, to a material path establishment method, a material scheduling method, an electronic device, and semiconductor process equipment.

BACKGROUND

[0002] As the scale of the semiconductor industry gradually expands and production capacity demands gradually increase, the topological structures of multi-chamber film deposition equipment (such as chemical vapor deposition equipment and atomic layer deposition equipment) have gradually evolved from a single vacuum transfer robot to multiple vacuum transfer robots (VTRs), with transfer chambers being cascaded and stacked to obtain more types and greater numbers of process chambers, thereby improving the process production capacity of the entire equipment.

[0003] As the topological structure becomes more complex, the scheduling calculation logic of software also becomes more complex and challenging, so as to achieve the same process requirements and effects under more complex material paths. The transfer and processing of materials (for example, wafers) are generally defined by a route/sequence, where each step (Step) in the route corresponds to an operation, and the location of the material when the operation is executed may be, for example, a process chamber, a load/unload chamber, or the like. For equipment with two transfer chambers, if two process chambers connected to the two

transfer chambers execute the same type of process in the route, they are regarded as executing the same process, and process chambers connected to different transfer chambers are referred to as parallel modules (Parallel Module) or parallel process chambers (Parallel Chamber).

[0004] However, since one of the two transfer chambers cannot receive a material directly, the material needs to be transferred through a pass-through chamber (PassThrough) connected between the two transfer chambers, such that the material is transferred to the other transfer chamber through one of the transfer chambers and the pass-through chamber. That is, transferring the material to one of the transfer chambers does not need passing through the pass-through chamber, while transferring the material to the other transfer chamber needs passing through the pass-through chamber. This results in different numbers of path steps being needed to transfer the material to the two transfer chambers, which in turn results in different numbers of path steps being needed to transfer the material to process chambers respectively connected to the two transfer chambers. As a result, material paths for executing the same process are incompatible with parallel process chambers, making it impossible for parallel process chambers to execute the same process and thereby affecting improvements in production capacity.

SUMMARY

[0005] The present disclosure is intended to solve at least one of the technical problems existing in the related art, and provides a material path establishment method, a material scheduling method, an electronic device, and semiconductor process equipment, which can solve the problem in the related art that parallel process chambers cannot execute the same process because material paths for executing the same process are incompatible with parallel process chambers.

[0006] To achieve the purpose of the present disclosure, a material path establishment method is provided. The method is applicable to semiconductor process equipment, the semiconductor process equipment includes a load/unload chamber and $N+1$ transfer chambers connected in sequence, and each transfer chamber is connected to at least one process chamber. The method includes:

[0007] Obtaining a process path, where the process path is formed by a plurality of chambers through which a material sequentially passes during a process;

[0008] Determining whether there are parallel process chambers, the parallel process chambers being process chambers that execute the same process in the process path and are connected to different transfer chambers;

[0009] In response to the existence of the parallel process chambers, splitting the process path into a base path and N backup paths, where:

[0010] The parallel process chambers included in the base path and the N backup paths are different, the transfer chamber connected to the parallel process chambers in the base path is a first transfer chamber, and the first transfer chamber is the transfer chamber directly connected to the load/unload chamber; and the transfer chamber connected to the parallel process chambers in the i -th backup path is an $(i+1)$ -th transfer chamber arranged after the first transfer chamber, where $i=1, 2, \dots, N$, and N is an integer greater than 0.

[0011] In some embodiments, the semiconductor process equipment further includes a plurality of pass-through chambers, and two adjacent transfer chambers are connected through the pass-through chambers. The plurality of chambers in the process path further include the $N+1$ transfer chambers and the plurality of pass-through chambers.

[0012] The base path includes the first transfer chamber and the parallel process chambers connected to the first transfer chamber.

[0013] The i -th backup path includes the first transfer chamber to the $(i+1)$ -th transfer chamber, the pass-through chambers connected between each two adjacent chambers from the first transfer chamber to the $(i+1)$ -th transfer chamber, and the parallel process chambers connected to the $(i+1)$ -th transfer chamber.

[0014] In some embodiments, determining whether there are parallel process chambers includes:

[0015] Determining, according to chamber process information of each chamber through which the material passes in the process path, whether there is a plurality of process chambers that execute the same process;

[0016] If so, determining, according to a pre-stored identifier i of the transfer chamber connected to each process chamber, whether there are process chambers connected to different transfer chambers among the plurality of process chambers that execute the same process; if so, determining that the process path includes the parallel process chambers;

[0017] Splitting the process path into a base path and N backup paths in response to the existence of the parallel process chambers includes:

[0018] Splitting the process path into the base path and the N backup paths according to the identifier i of the transfer chamber connected to the parallel process chamber.

[0019] In some embodiments, obtaining the process path includes:

[0020] Displaying an editing interface of the process path, where the editing interface displays sequence numbers indicating the order in which the material passes through the chambers in the process path and chamber process information;

[0021] When an editing instruction for the sequence numbers and the chamber process information is received, storing the edited sequence numbers and chamber process information, and displaying the edited sequence numbers and chamber process information on the editing interface;

[0022] The chamber process information includes chamber name information, slot information, and process recipe information; and the process recipe information of the plurality of parallel process chambers is the same.

[0023] In some embodiments, after splitting the process path into the base path and the N backup paths, the method further includes:

[0024] Displaying a first editing interface of the base path and a second editing interface of each backup path, where the first editing interface displays sequence numbers and chamber process information of the chambers through which the material sequentially passes in the base path; and the second editing interface displays sequence numbers and chamber process information of the chambers through which the material sequentially passes in the corresponding backup path;

[0025] When an editing instruction for the chamber process information is received, displaying edited chamber process information on the first editing interface or the second editing interface on which the chamber process information is located.

[0026] As another technical solution, the present disclosure further provides a material scheduling method, including:

[0027] Obtaining material information, where the material information includes path information, and the path information includes the base path and the N backup paths obtained by using the material path establishment method provided in the present disclosure in response to the existence of the parallel process chambers;

[0028] According to the material information, when a material located at a loading position starts to move, setting the base path as a material path in response to the base path being in an idle state;

[0029] In response to the base path being in an occupied state, setting each backup path that is in an idle state among the N backup paths as a material path;

[0030] Executing the material path.

[0031] In some embodiments, in response to all the backup paths being in an occupied state, when the base path becomes idle, setting the base path as the material path.

[0032] In some embodiments, in response to the absence of the parallel process chambers, the path information includes the process path;

[0033] After obtaining the material information, the material scheduling method further includes:

[0034] Setting the process path as the material path.

[0035] As another technical solution, the present disclosure further provides an electronic device, including:

[0036] At least one processor;

[0037] A storage apparatus, on which at least one program is stored;

[0038] When the at least one program is executed by the at least one processor, the at least one processor is caused to implement the material path establishment method provided in the present disclosure; or the material scheduling method provided in the present disclosure.

[0039] As another technical solution, the present disclosure further provides semiconductor process equipment, including a plurality of process chambers, a load/unload chamber, a plurality

of transfer chambers connected in sequence, and a controller, where each transfer chamber is connected to the plurality of process chambers;

[0040] The controller includes:

[0041] At least one processor;

[0042] A memory, on which at least one program is stored;

[0043] When the at least one program is executed by the at least one processor, the at least one processor is caused to implement the material path establishment method provided in the present disclosure; or the material scheduling method provided in the present disclosure.

[0044] The present disclosure has the following beneficial effects:

[0045] In the technical solutions of the material path establishment method, the material scheduling method, the electronic device, and the semiconductor process equipment provided in the present disclosure, when parallel process chambers exist in a process path, the process path is split into a base path and N backup paths, where the parallel process chambers included in the base path and the N backup paths are different, the transfer chamber connected to the parallel process chambers in the base path is a first transfer chamber, and the transfer chamber connected to the parallel process chambers in the i-th backup path is an (i+1)-th transfer chamber arranged after the first transfer chamber. After the splitting, in response to the existence of parallel process chambers, materials can be scheduled according to a plurality of paths. That is, when a material located at a loading position starts to move, the base path is set as the material path in response to the base path being in an idle state; and in response to the base path being in an occupied state, each backup path that is in an idle state among the N backup paths is set as the material path. In this way, compatibility with parallel process chambers executing the same process can be achieved, thereby improving production capacity.

BRIEF DESCRIPTION OF THE DRAWINGS

[0046] FIG. 1 is a structural diagram of semiconductor process equipment provided with two transfer chambers that are cascaded and stacked;

[0047] FIG. 2 is a flowchart of a material path establishment method according to an embodiment of the present disclosure;

[0048] FIG. 3 is a flowchart of operation S102 of the material path establishment method according to an embodiment of the present disclosure;

[0049] FIG. 4 is a flowchart of operation S101 of the material path establishment method according to an embodiment of the present disclosure;

[0050] FIG. 5 is a display diagram of an editing interface employed in an embodiment of the present disclosure;

[0051] FIG. 6 is another flowchart of the material path establishment method according to an embodiment of the present disclosure;

[0052] FIG. 7 is a display diagram of a first editing interface employed in an embodiment of the present disclosure;

[0053] FIG. 8 is a display diagram of a second editing interface employed in an embodiment of the present disclosure;

[0054] FIG. 9 is a flowchart of the material scheduling method according to an embodiment of the present disclosure.

DETAILED DESCRIPTION OF THE EMBODIMENTS

[0055] To enable those skilled in the art to better understand the technical solutions of the present disclosure, the material path establishment method, the material scheduling method, the

electronic device, and the semiconductor process equipment provided in the present disclosure are described in detail below with reference to the accompanying drawings.

[0056] Semiconductor process equipment in which a plurality of transfer chambers are cascaded and stacked may have various structures. Taking semiconductor process equipment provided with two transfer chambers that are cascaded and stacked as an example, please refer to FIG. 1, the semiconductor process equipment at least includes:

[0057] Six process chambers (Ch1 to Ch6), where each process chamber may, for example, have a dual-chamber configuration;

[0058] Four load/unload chambers (LA, LB, LC, and LD), where each load/unload chamber LoadLock is connected to an atmospheric transfer chamber and is configured to convert an atmospheric environment into a vacuum environment. An atmospheric robot ATR is disposed in the atmospheric transfer chamber and is configured to transfer materials (for example, wafers) between FOUPs in three storage chambers (LP1, LP2, and LP3) and the load/unload chambers LoadLock;

[0059] A first transfer chamber Buffer, connected to four load/unload chambers (LA, LB, LC, and LD), connected to two process chambers (Ch1 and Ch2), and connected to two pass-through chambers (ChA and ChB); each pass-through chamber PassThrough is connected between the first transfer chamber Buffer and a second transfer chamber Transfer; and a first robot VTR1 is disposed in the first transfer chamber Buffer and is configured to transfer materials between the load/unload chambers and the two process chambers (Ch1 and Ch2), and between the load/unload chambers and the two pass-through chambers (ChA and ChB);

[0060] A second transfer chamber Transfer, connected to two pass-through chambers (ChA and ChB), and connected to four process chambers (Ch3 to Ch6); and a second robot VTR2 is

disposed in the second transfer chamber Transfer and is configured to transfer materials between the two pass-through chambers (ChA and ChB) and the four process chambers (Ch3 to Ch6).

[0061] In some embodiments, the two process chambers (Ch1 and Ch2) connected to the first transfer chamber Buffer are of different types and are configured to respectively complete two different types of processes, i.e., execute two different process operations. The type of process chamber Ch1 is, for example, the same as the type of two of the four process chambers (Ch3 to Ch6) connected to the second transfer chamber Transfer, for example, process chambers Ch3 and Ch5, such that the three process chambers Ch1, Ch3, and Ch5 complete the same type of process, i.e., execute the same process operation. The type of process chamber Ch2 is the same as the type of the other two of the four process chambers (Ch3 to Ch6) connected to the second transfer chamber Transfer, for example, process chambers Ch4 and Ch6, such that the three process chambers Ch2, Ch4, and Ch6 complete the same type of process, i.e., execute the same process operation. The above process chambers that execute the same process and are connected to different transfer chambers are referred to as parallel process chambers. For example, process chamber Ch1 and process chamber Ch3, and process chamber Ch1 and process chamber Ch5, are both parallel process chambers; and process chamber Ch2 and process chamber Ch4, and process chamber Ch2 and process chamber Ch6, are both parallel process chambers.

[0062] By using a plurality of process chambers to complete the same process operation, the production capacity of the process operation can be improved. For example, if a process operation needs 30 minutes, and the process operation is executed by one process chamber, two materials can be processed per hour; if the process operation is executed by parallel process chambers formed by two process chambers, four materials can be processed per hour. Thus, it

can be seen that configuring a plurality of process chambers having the same type of process as parallel process chambers can multiply production capacity.

[0063] However, since a pass-through chamber PassThrough is disposed between the first transfer chamber Buffer and the second transfer chamber Transfer, transferring a material to the first transfer chamber Buffer does not need passing through the pass-through chamber PassThrough, while transferring the material to the second transfer chamber Transfer needs passing through the pass-through chamber PassThrough. As a result, the number of steps needed to transfer the material to the first transfer chamber Buffer differs from the number of steps needed to transfer the material to the second transfer chamber Transfer, causing the numbers of path steps needed to reach process chambers respectively connected to the first transfer chamber Buffer and the second transfer chamber Transfer to be different. For example, the preceding operation before transferring a material to process chamber Ch1 is transferring the material to load/unload chamber LoadLock; while the preceding operation before transferring the material to process chamber Ch3 is transferring the material to load/unload chamber LoadLock and then transferring the material to pass-through chamber PassThrough. Thus, it can be seen that the number of path steps needed to reach a process chamber connected to the second transfer chamber Transfer is one step greater than the number of path steps needed to reach a process chamber connected to the first transfer chamber Buffer. Currently, software can only establish a path for transferring a material to a process chamber connected to the second transfer chamber Transfer, or a path for transferring a material to a process chamber connected to the first transfer chamber Buffer. However, these paths cannot be compatible with transferring a plurality of materials to process chambers connected to the first transfer chamber Buffer and process chambers connected to the second transfer chamber Transfer. Therefore, it is impossible for

parallel process chambers to execute the same process operation when material paths for executing the same process are incompatible with parallel process chambers, thereby affecting improvements in production capacity.

[0064] To solve the above technical problem, please refer to FIG. 2. An embodiment of the present disclosure provides a material path establishment method. The method is applicable to semiconductor process equipment, and the semiconductor process equipment includes a load/unload chamber and $N+1$ transfer chambers connected in sequence, where N is an integer greater than 0. Each transfer chamber is connected to at least one process chamber.

[0065] The material path establishment method includes:

[0066] At S101, a process path is obtained;

[0067] The process path (Route/Sequence) is formed by a plurality of chambers through which a material sequentially passes during a process. Specifically, each step (Step) in the process path corresponds to a chamber, i.e., the process path includes chambers through which the material sequentially passes during transfer, such as process chambers, load/unload chambers LoadLock, pass-through chambers PassThrough, or the like.

[0068] At S102, it is determined whether there are parallel process chambers.

[0069] The parallel process chambers are process chambers that execute the same process in the process path and are connected to different transfer chambers.

[0070] At S103, in response to the existence of parallel process chambers, the process path is split into a base path and N backup paths.

[0071] The parallel process chambers included in the base path and the N backup paths are different.

[0072] The plurality of cascaded and stacked transfer chambers refers to a plurality of transfer chambers connected in sequence through pass-through chambers PassThrough. Where the transfer chamber directly connected to the load/unload chamber LoadLock is a first transfer chamber; the transfer chamber adjacent to and arranged after the first transfer chamber is a second transfer chamber, and the second transfer chamber is connected to the first transfer chamber through a pass-through chamber PassThrough; the transfer chamber adjacent to and arranged after the second transfer chamber is a third transfer chamber, and the third transfer chamber is connected to the second transfer chamber through a pass-through chamber PassThrough. Correspondingly, the transfer chamber adjacent to and arranged after the i -th transfer chamber is an $(i+1)$ -th transfer chamber, and the $(i+1)$ -th transfer chamber is connected to the i -th transfer chamber through a pass-through chamber PassThrough, where $i=1, 2, \dots, N$, and N is the number of transfer chambers other than the first transfer chamber.

[0073] The transfer chamber connected to the parallel process chambers in the base path is the first transfer chamber; and the transfer chamber connected to the parallel process chambers in the i -th backup path is the $(i+1)$ -th transfer chamber arranged after the first transfer chamber. Taking into consideration the plurality of pass-through chambers and the $N+1$ transfer chambers, the base path includes the first transfer chamber and the parallel process chambers connected to the first transfer chamber; and the i -th backup path includes the first transfer chamber to the $(i+1)$ -th transfer chamber, the pass-through chambers connected between each two adjacent chambers from the first transfer chamber to the $(i+1)$ -th transfer chamber, and the parallel process chambers connected to the $(i+1)$ -th transfer chamber.

[0074] Taking the semiconductor process equipment shown in FIG. 1 as an example, the base path includes the first transfer chamber Buffer, process chamber Ch1 that executes a first process

operation (Step1), and process chamber Ch2 that executes a second process operation (Step2); and the first backup path includes the first transfer chamber Buffer, the second transfer chamber Transfer, process chambers Ch3 and Ch5 that execute the first process operation (Step1), and process chambers Ch4 and Ch6 that execute the second process operation (Step2). In some embodiments, taking as an example that two process chambers (Ch1 and Ch2) are connected between the first transfer chamber Buffer and the second transfer chamber Transfer, the base path includes the first transfer chamber Buffer, process chamber Ch1 that executes the first process operation (Step1), and process chamber Ch2 that executes the second process operation (Step2); and the first backup path includes the first transfer chamber Buffer, the two process chambers (Ch1 and Ch2), the second transfer chamber Transfer, process chambers Ch3 and Ch5 that execute the first process operation (Step1), and process chambers Ch4 and Ch6 that execute the second process operation (Step2).

[0075] In response to the existence of parallel process chambers, after the process path is split as described above, materials can be scheduled according to a plurality of paths (including the base path and the N backup paths). That is, when a material located at a loading position starts to move, the base path is set as the material path in response to the base path being in an idle state; and in response to the base path being in an occupied state, each backup path that is in an idle state among the N backup paths is set as the material path. In other words, in response to the existence of parallel process chambers, the base path and the N backup paths can be executed sequentially according to the occupancy status of the base path and the N backup paths, so as to enable process chambers connected to different transfer chambers to execute the same process (i.e., execute the same process operation). In this way, compatibility with parallel process chambers executing the same process can be achieved, thereby improving production capacity.

[0076] In some embodiments, the above operation S102 may be implemented by software. As shown in FIG. 3, operation S102, i.e., determining whether there are parallel process chambers, specifically includes:

[0077] At S1021, it is determined, according to chamber process information of each chamber through which the material passes in the process path, whether there is a plurality of process chambers that execute the same process;

[0078] The chamber process information may, for example, include chamber name information, slot information, and process recipe information. Whether there is a plurality of process chambers that execute the same process can be determined from the chamber process information. Taking the semiconductor process equipment shown in FIG. 1 as an example, the process chambers that execute the same process, i.e., execute the first process operation (Step1), include process chambers Ch1, Ch3, and Ch5; and the process chambers that execute the second process operation (Step2) include process chambers Ch2, Ch4, and Ch6.

[0079] At S1022, if so, i.e., if there is a plurality of process chambers that execute the same process, it is determined, according to the pre-stored identifier i of the transfer chamber connected to each process chamber, whether there are process chambers connected to different transfer chambers among the plurality of process chambers that execute the same process; and if so, it is determined that the process path includes parallel process chambers;

[0080] Taking the semiconductor process equipment shown in FIG. 1 as an example, the first transfer chamber Buffer is the first transfer chamber, i.e., its identifier is 1; and the second transfer chamber Transfer is the second transfer chamber, i.e., its identifier is 2. According to the identifiers, it can be determined that the transfer chambers connected to process chamber Ch1 and process chambers Ch3 and Ch5, which execute the same process, are different, and the

transfer chambers connected to process chamber Ch2 and process chambers Ch4 and Ch6, which execute the same process, are different. Correspondingly, it can be determined that the process path includes parallel process chambers.

[0081] Further, the above operation S103 may be implemented by software, and specifically includes:

[0082] Splitting the process path into a base path and N backup paths according to the identifier i of the transfer chamber connected to the parallel process chambers.

[0083] That is, the transfer chamber connected to the parallel process chambers in the base path is the first transfer chamber; and the transfer chamber connected to the parallel process chambers in the i-th backup path is the (i+1)-th transfer chamber arranged after the first transfer chamber.

Taking the semiconductor process equipment shown in FIG. 1 as an example, N is the number of transfer chambers other than the first transfer chamber, i.e., $N=1$. In this case, there is one backup path, and the transfer chamber connected to the parallel process chambers in the backup path is the second transfer chamber arranged after the first transfer chamber, i.e., the second transfer chamber Transfer.

[0084] In some embodiments, in response to the absence of parallel process chambers in the process path, the process path does not need to be split.

[0085] In some embodiments, the above operation S101, i.e., obtaining the process path, may be implemented by software. As shown in FIG. 4, the operation specifically includes:

[0086] At S1011, an editing interface of the process path is displayed;

[0087] The editing interface displays sequence numbers indicating the order in which the material passes through the chambers in the process path and chamber process information;

[0088] The sequence numbers indicating the order in which the material passes through the chambers are the sequence numbers of the respective steps (Step) in the process path.

[0089] At S1012, when an editing instruction for the sequence numbers and the chamber process information is received, edited sequence numbers and edited chamber process information are stored and displayed on the editing interface.

[0090] In a specific embodiment of the present disclosure, taking the semiconductor process equipment shown in FIG. 1 as an example, the editing interface of the above process path is shown in FIG. 5. On the editing interface, the sequence numbers indicating the order in which the material passes through the chambers in the process path are represented by “Step.” Where Step 1 represents the chamber having sequence number 1, specifically two load/unload chambers (LA and LB); Step 2 represents the chamber having sequence number 2, specifically process chamber Ch1; Step 3 represents the chamber having sequence number 3, specifically pass-through chamber ChA; Step 4 represents the chamber having sequence number 4, specifically process chambers Ch3 and Ch4; Step 5 represents the chamber having sequence number 5, specifically pass-through chamber ChA; and Step 6 represents the chamber having sequence number 6, specifically two load/unload chambers (LA and LB). Correspondingly, the chambers in the process path, in the order through which the material passes, are two load/unload chambers (LA and LB), process chamber Ch1, pass-through chamber ChA, process chambers Ch3 and Ch4, pass-through chamber ChA, and two load/unload chambers (LA and LB). On the editing interface, the above chamber process information may, for example, include “Chamber” (i.e., chamber name), “Slot” (i.e., slot information), and “Recipe” (i.e., process recipe information).

[0091] The above editing interface may be used to receive editing instructions for sequence numbers and chamber process information entered by a user, so as to implement an editing function for the process path.

[0092] In some embodiments, as shown in FIG. 6, after the above operation S103 is completed, the method further includes:

[0093] At S104, a first editing interface of the base path and a second editing interface of each backup path are displayed;

[0094] The first editing interface displays sequence numbers and chamber process information of the chambers through which the material sequentially passes in the base path. The second editing interface displays sequence numbers and chamber process information of the chambers through which the material sequentially passes in the corresponding backup path. The number of second editing interfaces is the same as the number of backup paths, i.e., each backup path corresponds to one second editing interface.

[0095] At S105, when an editing instruction for chamber process information is received, edited chamber process information is displayed on the first editing interface or the second editing interface on which the chamber process information is located.

[0096] The above first editing interface for displaying the base path is shown in FIG. 7, and the second editing interface of each backup path is shown in FIG. 8. The editable options displayed on the first editing interface and the second editing interface are the same as the editable options on the editing interface shown in FIG. 5. Taking as an example that three process chambers (Ch1, Ch3, and Ch5) are used to execute one type of process and the other three process chambers (Ch2, Ch4, and Ch6) are used to execute another type of process, on the first editing interface, as shown in FIG. 7, the chambers in the base path, in the order through which the

material passes, are four load/unload chambers (LA, LB, LC, and LD), process chamber Ch1, process chamber Ch2, and four load/unload chambers (LA, LB, LC, and LD). On the second editing interface, as shown in FIG. 8, the chambers in the first backup path, in the order through which the material passes, are four load/unload chambers (LA, LB, LC, and LD), pass-through chambers ChA and ChB, process chambers Ch3 and Ch5, process chambers Ch4 and Ch6, pass-through chambers ChA and ChB, and four load/unload chambers (LA, LB, LC, and LD).

[0097] The above first editing interface and second editing interface may be used to respectively display the split base path and backup paths, and receive editing instructions for chamber process information entered by a user, so as to implement editing functions for the base path and the backup paths.

[0098] It should be noted that, in this embodiment, obtaining of the process path, splitting of the process path, and determination of parallel process chambers are all implemented by software.

However, the embodiments of the present disclosure are not limited thereto. In practical applications, at least one of obtaining of the process path, splitting of the process path, or determination of parallel process chambers may be implemented by obtaining relevant information entered by a user through the above first editing interface and second editing interface, i.e., the base path and the backup paths may be directly obtained by receiving corresponding information entered by the user.

[0099] As another technical solution, please refer to FIG. 9. An embodiment of the present disclosure further provides a material scheduling method, including:

[0100] At S301, material information is obtained;

[0101] The material information includes path information, and the path information includes the base path and N backup paths obtained by using the material path establishment method

provided in the embodiments of the present disclosure in response to the existence of parallel process chambers;

[0102] At S302, according to the material information, when a material located at a loading position starts to move, operation S303 is executed in response to the base path being in an idle state; and operation S304 is executed in response to the base path being in an occupied state;

[0103] At S303, the base path is set as a material path;

[0104] At S304, in response to at least one backup path of the N backup paths being in an idle state, one of the at least one backup path that is in an idle state among the N backup paths is set as a material path;

[0105] At S305, in response to all the backup paths being in an occupied state, when the base path becomes idle, the base path is set as a material path;

[0106] At S306, the material path is executed.

[0107] In the material scheduling method provided in the embodiments of the present disclosure, in response to the existence of parallel process chambers, materials may be scheduled according to a plurality of paths. That is, when a material located at a loading position starts to move, the base path is set as a material path in response to the base path being in an idle state; and in response to the base path being in an occupied state, one of the at least one backup path that is in an idle state among the N backup paths is set as a material path. In this way, compatibility with parallel process chambers executing the same process can be achieved, thereby improving production capacity.

[0108] In some embodiments, in response to the absence of parallel process chambers in the process path, the process path does not need to be split. In this case, in the above operation S301, the obtained material information includes the above process path; and after the above operation

S301, the material scheduling method provided in the embodiments of the present disclosure further includes:

[0109] Setting the process path as a material path.

[0110] As another technical solution, an embodiment of the present disclosure further provides an electronic device, including:

[0111] At least one processor;

[0112] A storage apparatus, on which at least one program is stored;

[0113] When the at least one program is executed by the at least one processor, the at least one processor is caused to implement the material path establishment method provided in the embodiments of the present disclosure; or the material scheduling method provided in the embodiments of the present disclosure.

[0114] As another technical solution, an embodiment of the present disclosure further provides semiconductor process equipment, including a plurality of process chambers, a load/unload chamber, a plurality of transfer chambers connected in sequence, and a controller, where each transfer chamber is connected to a plurality of process chambers; the controller includes:

[0115] At least one processor;

[0116] A storage apparatus, on which at least one program is stored;

[0117] When the at least one program is executed by the at least one processor, the at least one processor is caused to implement the material path establishment method provided in the embodiments of the present disclosure; or the material scheduling method provided in the embodiments of the present disclosure.

[0118] Taking the above semiconductor process equipment shown in FIG. 1 as an example, the semiconductor process equipment at least includes:

[0119] Six process chambers (Ch1 to Ch6), where each process chamber has a dual-chamber configuration;

[0120] Four load/unload chambers (LA, LB, LC, and LD), where each load/unload chamber LoadLock is connected to an atmospheric transfer chamber and is configured to convert an atmospheric environment into a vacuum environment. An atmospheric robot ATR is disposed in the atmospheric transfer chamber and is configured to transfer materials (for example, wafers) between FOUPs in three storage chambers (LP1, LP2, and LP3) and the load/unload chambers LoadLock;

[0121] A first transfer chamber Buffer, connected to four load/unload chambers (LA, LB, LC, and LD), connected to two process chambers (Ch1 and Ch2), and connected to two pass-through chambers (ChA and ChB); each pass-through chamber PassThrough is connected between the first transfer chamber Buffer and the second transfer chamber Transfer; and a first robot VTR1 is disposed in the first transfer chamber Buffer and is configured to transfer materials between the load/unload chambers and the two process chambers (Ch1 and Ch2), and between the load/unload chambers and the two pass-through chambers (ChA and ChB);

[0122] A second transfer chamber Transfer, connected to two pass-through chambers (ChA and ChB), and connected to four process chambers (Ch3 to Ch6); and a second robot VTR2 is disposed in the second transfer chamber Transfer and is configured to transfer materials between the two pass-through chambers (ChA and ChB) and the four process chambers (Ch3 to Ch6).

[0123] The flowcharts and block diagrams in the drawings illustrate the architecture, functionality, and operation of possible implementations of systems, methods, and computer program products according to various embodiments of the present disclosure. In this regard, each block in a flowchart or block diagram may represent a module, a program segment, or a

portion of code, where the module, program segment, or portion of code includes one or more executable instructions for implementing specified logical functions. It should also be noted that, in some alternative implementations, the functions indicated in the blocks may occur in an order different from that indicated in the drawings. For example, two blocks shown in succession may in fact be executed substantially in parallel, or they may sometimes be executed in the reverse order, depending on the functions involved. It should also be noted that each block in the block diagrams and/or flowcharts, and combinations of blocks in the block diagrams and/or flowcharts, may be implemented by dedicated hardware-based systems that perform the specified functions or operations, or may be implemented by a combination of dedicated hardware and computer instructions.

[0124] It can be understood that the above embodiments are merely exemplary embodiments adopted to illustrate the principles of the present disclosure, and the present disclosure is not limited thereto. Various modifications and improvements may be made by those of ordinary skill in the art without departing from the spirit and essence of the present disclosure, and such modifications and improvements shall also fall within the scope of the present disclosure.

CLAIMS

WHAT IS CLAIMED IS:

1. A material path establishment method, applicable to semiconductor process equipment including a load/unload chamber and $N+1$ transfer chambers connected in sequence, and each transfer chamber being connected to at least one process chamber, wherein the method includes:

obtaining a process path formed by a plurality of chambers through which a material sequentially passes during a process;

determining whether there are parallel process chambers, the parallel process chambers being process chambers that execute same process in the process path and being connected to different transfer chambers;

in response to existence of the parallel process chambers, splitting the process path into a base path and N backup paths, wherein:

the parallel process chambers included in the base path and the N backup paths are different, a transfer chamber connected to the parallel process chambers in the base path is a first transfer chamber, the first transfer chamber being a transfer chamber directly connected to the load/unload chamber, and the transfer chamber connected to the parallel process chambers in the i -th backup path is an $(i+1)$ -th transfer chamber arranged after the first transfer chamber, where $i=1, 2, \dots, N$, and N is an integer greater than 0.

2. The material path establishment method according to claim 1, wherein the semiconductor process equipment further includes a plurality of pass-through chambers, and every two adjacent transfer chambers are connected through the pass-through chambers, the

plurality of chambers in the process path further include the $N+1$ transfer chambers and the plurality of pass-through chambers;

the base path includes the first transfer chamber and the parallel process chambers connected to the first transfer chamber;

the i -th backup path includes the first transfer chamber to the $(i+1)$ -th transfer chamber, the pass-through chambers connected between each two adjacent chambers from the first transfer chamber to the $(i+1)$ -th transfer chamber, and the parallel process chambers connected to the $(i+1)$ -th transfer chamber.

3. The material path establishment method according to claim 1 or 2, wherein determining whether there are parallel process chambers includes:

determining, according to chamber process information of each chamber through which the material passes in the process path, whether there is a plurality of process chambers that execute the same process;

if there is a plurality of process chambers that execute the same process, determining, according to a pre-stored identifier i of the transfer chamber connected to each process chamber, whether there are process chambers connected to different transfer chambers among the plurality of process chambers that execute the same process; and if there are process chambers connected to different transfer chambers among the plurality of process chambers that execute the same process, determining that the process path includes the parallel process chambers;

splitting the process path into the base path and the N backup paths in response to the existence of the parallel process chambers includes:

splitting the process path into the base path and the N backup paths according to the identifier i of the transfer chamber connected to the parallel process chambers.

4. The material path establishment method according to claim 3, wherein obtaining the process path includes:

displaying an editing interface of the process path, the editing interface displaying sequence numbers indicating an order in which a material passes through chambers in the process path and chamber process information;

when an editing instruction for the sequence numbers and the chamber process information is received, storing edited sequence numbers and edited chamber process information, and displaying the edited sequence numbers and the edited chamber process information on the editing interface;

wherein the chamber process information includes chamber name information, slot information, and process recipe information, and the process recipe information of the plurality of parallel process chambers is the same.

5. The material path establishment method according to claim 3, wherein after splitting the process path into the base path and the N backup paths, the method further includes:

displaying a first editing interface of the base path and a second editing interface of each backup path, the first editing interface displaying sequence numbers and chamber process information of chambers through which the material sequentially passes in the base path, and the second editing interface displaying sequence numbers and chamber process information of chambers through which the material sequentially passes in a corresponding backup path;

when an editing instruction for the chamber process information is received, displaying edited chamber process information on the first editing interface or the second editing interface on which the chamber process information is located.

6. A material scheduling method comprising:

obtaining material information including path information, the path information including the base path and the N backup paths obtained, in response to the existence of the parallel process chambers, using the method according to any one of claims 1-5;

according to the material information, when a material located at a loading position starts to move, setting the base path as a material path in response to the base path being in an idle state;

in response to the base path being in an occupied state, setting one of at least one backup path that is in an idle state among the N backup paths as a material path;

executing the material path.

7. The material scheduling method according to claim 6, wherein in response to all the backup paths being in an occupied state, when the base path becomes idle, setting the base path as the material path.

8. The material scheduling method according to claim 6, wherein in response to absence of the parallel process chambers, the path information includes the process path;

after obtaining the material information, the material scheduling method further includes:
setting the process path as the material path.

9. An electronic device, comprising:
at least one processor;
a storage apparatus, on which at least one program is stored;
wherein when the at least one program is executed by the at least one processor, the at least one processor is caused to implement the material path establishment method according to any one of claims 1-5, or the material scheduling method according to any one of claims 6-8.

10. Semiconductor process equipment, comprising a plurality of process chambers, a load/unload chamber, a plurality of transfer chambers connected in sequence, and a controller, wherein each transfer chamber is connected to the plurality of process chambers;
the controller includes:
at least one processor;
a memory, on which at least one program is stored;
wherein when the at least one program is executed by the at least one processor, the at least one processor is caused to implement the material path establishment method according to any one of claims 1-5, or the material scheduling method according to any one of claims 6-8.