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DMOS TRANSISTOR STRUCTURE & METHOD

DESCRIPTION

This invention relates to metal semiconductor (MOS) field effect devices and more specifically to lateral double-diffused MOS (DMOS) field effect transistors or transistor structures.

Lateral double-diffused metal-oxide-semiconductor (lateral DMOS) transistors of the type having a light-doped drain (LDD) region (or "LDD lateral DMOS transistors") are often found in high-voltage integrated circuits. Among these LDD lateral DMOS devices, the self-isolated devices are especially desirable because of their relative ease of integration with low-voltage devices, which are often used to perform logic functions. The self-isolated devices are so described because, for N-channel devices, each transistor's N+ drain and source regions are separated from the N+ drain and source regions of other transistors by the reverse-biased PN-junction formed between each of these drain and source regions and the P-type substrate. Because of self-isolation, the self-isolated DMOS devices occupy less area and are relatively less costly than either the junction-isolated LDD lateral DMOS devices or the dielectric-isolated LDD lateral DMOS devices discussed above can be found in "Power Integrated Circuits -- A Brief Overview" by B. Baliga, IEEE Transactions on Electron Devices, Vol. ED-33, No. 12, December 1986, pp.1936-9.

Reference is now made to the accompanying drawings, in which:

Figure 1 shows a self-isolated LDD lateral DMOS transistor in the prior art,

Figure 2 shows the electrical equipotential distribution for the self-isolated LDD lateral DMOS transistor of Figure 1,

Figure 3 shows the electrical equipotential distribution

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for a prior art self-isolated LDD lateral DMOS transistor having a gate plate, and

Figure 4 shows a prior art RESURF type lateral DMOS transistor having a buried P+ layer.

Figure 1 is a cross section of an N-channel LDD lateral DMOS transistor 100 showing the double-diffused N+ source region 102 and P-body region 103. The P-body and

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source regions 103 and 102 are commonly connected by conductor 120, which connects the P-body region 108 via the P+ contact region 101. The drain of transistor 100 is formed by the N- LDD or drift region 122 and the N+ contact region 107. Transistor 100 is controlled by the voltage of gate 109, which is situated above the gate oxide 110 and enclosed by insulation layer 121. Optionally, a deep P+ region 104 can be formed to provide a good contact to the P- substrate 105. This deep P+ region 104 does not significantly impact the breakdown voltage of transistor 100, nor increases the parasitic capacitance associated with the transistor 100. An optional N-well 106 can also be formed to provide a "deep" drain region suitable for longer-drift high-voltage devices requiring a higher breakdown voltage. Transistor breakdown often occurs at the high electric field associated with the edge of the drift region 122 next to the N+ contact region 107 ("drain-edge"), if the drift region 122 is very lightly doped. Alternatively, breakdown is more likely to occur at the edge of the drift region 122 next to the gate 109 ("gate-edge"), if the drift region 122 is relatively more heavily doped. A higher dopant concentration in the drift region 122 reduces the on-resistance of the transistor 100, thereby allowing a higher saturation current. However, a breakdown at the surface near the gate-edge of drift region 122 may leave an amount of charge in the gate oxide 110, resulting in reliability problems and an unstable breakdown voltage.

Figure 2 shows the electrical potential distribution when transistor 100 is in the "off" state. (In Figure 2, the optional deep P+ region 104 and the optional N-well 106 are not shown). As shown in Figure 2, high electric fields are indicated by the closely-spaced electrical equipotential lines "crowding" at the gate-edge of the drift region 122. The distribution of high electric fields at the gate edge lowers the breakdown voltage of transistor 100.

Figure 3 illustrates one method in the prior art to relieve the crowding of electrical equipotential lines, and thereby increases the breakdown voltage of transistor 100. As shown in Figure 3, a conductor 111, called a field plate, which is electrically connected either to the gate 109 or the source region 102, is situated above the gate-edge of the drift region 122. As shown in Figure 3, the presence of the field plate 111 reduces the crowding of equipotentials at the gate-edge of the drift region 122 above the silicon surface, and hence lowers the electric field intensities at the gate-edge. The field plate 111 can be formed using polysilicon or metal. (When the field plate is electrically connected to the gate 109, the field plate is also known as the "gate plate"). However, there still remains high electric fields at the sidewalls (indicated by arrow A) of the N- drift region 122. Hence, the relief of electrical equipotential crowding using the gate plate approach is not satisfactory, particularly because reasonable and expected process variations in the doping concentration of the N- drift region 122 can exacerbate such field crowding.

Another method to increase breakdown voltage of a LDD lateral DMOS transistor is achieved by the reduced surface field (RESURF) technique, discussed in "High Voltage Thin Layer Devices (RESURF Devices)," by J. Appels et al, International Electron Device Meeting Technical Digest, December 1979, pp. 238-41. The RESURF technique provides the LDD lateral DMOS transistor in a lightly doped N- epitaxial layer on top of a P- substrate. In the RESURF technique, adjacent transistors are junction-isolated by P+ regions.

Figure 4 shows a junction-isolated RESURF lateral DMOS transistor 200 having a field-shaping P+ buried layer 201. In Figure 4, transistor 200 is fabricated in an N- epitaxial layer 206 formed on top of the P- substrate 205. Transistor 200 comprises the N+ source and drain regions 202 and 207, the P-body region 203, and gate 209, which is

formed above a gate oxide layer 210 and enclosed in the insulator layer 221. The N+ source region 202 and the P-body region 203 are commonly connected by the metallization 220. In addition, transistor 200 is provided a field-shaping buried layer 201, which extends from the P+ isolation 204 and reaches horizontally underneath the gate region beyond the gate-edge of the drift region 222. In Figure 4, in addition to the increased breakdown voltage due to the RESURF effects, the field-shaping P+ buried layer 201 enhances the breakdown voltage further by "uncrowding" the equipotential lines in the N- epitaxial layer 206 next to the gate region underneath 209. A similar transistor is disclosed in U.S. Patent 4,300,150, entitled "lateral Double-diffused MOS transistor Device," by S. Colak, filed Jun. 16, 1980 and issued Nov. 10, 1981.

While RESURF lateral DMOS transistor 200 of Figure 4 has its breakdown voltage enhanced, due to both the use of the RESURF technique and the field-shaping P+ buried layer 201, RESURF lateral DMOS transistor 200 is expensive from the packing density stand point because additional area is required by the P+ isolation region 204. In addition, the P+ isolation region 204 must be appropriately shaped, as shown in Figure 4, to short the emitter-to-base junction of the high-gain parasitic vertical NPN transistor formed by the N+ source region 202, the P-body region 203, and the epitaxial region 206. Shorting the emitter-to-base junction prevents a phenomenon known as "common-emitter base-open breakdown voltage snap-back" ("BV_{CEO} snapback"), which can destroy the device. In fabricating the P+ isolation region 204, care must be taken to ensure that the P+ diffusion penetrates the N- epitaxial layer into the P- substrate to ensure complete isolation.

Further, the P-body region 203 of RESURF lateral DMOS transistor 200 of Figure 4 forms a reversed-bias junction with the N- epitaxial layer 206. Such reversed-biased junction increases the likelihood of punchthrough (barrier lowering) breakdown degradation in RESURF lateral DMOS

transistor 200. As a result, the ability to integrate other bipolar or high voltage devices may be restricted by design considerations of the RESURF lateral DMOS transistor.

Therefore, a self-isolated LDD lateral DMOS transistor having reduced peak electric field at the gate-edge of the drift region is highly desirable. Such transistor would allow a higher dopant concentration in the drift region without reliability or breakdown voltage degradation. Further, such self-isolated LDD lateral DMOS transistor provides the breakdown voltage and reliability characteristics without incurring the area penalty of the P+ isolation in a RESURF type lateral DMOS transistor, and allows the designer further freedom to select and use thicker epitaxial layers for other purposes, such as for providing a vertical NPN transistor.

In accordance with a structure and a method of the present invention, a self-isolated LDD lateral DMOS transistor is provided having reduced peak electric fields at the gate edge without the added area cost of a RESURF transistor. The self-isolated LDD lateral DMOS transistor is formed in a lightly-doped epitaxial layer having the same conductivity type as the conductivity types of the substrate, a double-diffused body region and a buried layer. The buried layer extends from a position substantially beneath the source region to a position substantially beneath the drift region.

In one embodiment, a conductive gate plate (which may be metal, doped polysilicon, or any other appropriate conductive material) is provided above the gate region of the self-isolated lateral DMOS transistor. In another embodiment, a deep body diffusion region is provided in the self-isolated DMOS transistor. In another embodiment, a deep drain diffusion region is provided in the self-isolated DMOS transistor. In yet another embodiment,

the gate, the buried P+ layer and the drift regions of the self-isolated LDD lateral DMOS transistor form a substantially annular structure surrounding the drain region. In these embodiments, the buried layer, in conjunction with the structure or structures mentioned above, provides field-shaping flexibility to increase the breakdown voltage by relieving electric field crowding.

In another embodiment of the present invention, the drift and the buried P+ regions form a substantially annular structure surrounding the drain region. However, in this embodiment, only one portion of the drift region is bordered by the channel region; another portion of the drift region abuts an "inactive edge" formed by a field oxide layer and the drift region. A P+ buried layer underneath the inactive edge is provided to reduce the electric field intensity at the inactive edge.

In another embodiment of the present invention, a diode is formed by eliminating the active channel region of an LDD lateral DMOS transistor. The P+ buried layer reduces the electric fields at the drift/field oxide interface, and improves the cathode-to-anode reverse-recovery characteristics.

In another embodiment of the present invention, a field oxide region is formed over the drift region prior to formation of the gate. The gate is extended over the field oxide region so as to reduce the electric field intensity at the interface between the channel and the drift regions.

The present invention is further described below, by way of example, with reference to the remaining figures of the accompanying drawings, in which:

Figure 5 shows a self-isolated LDD lateral DMOS transistor with a field-shaping P+ buried layer, in accordance with an embodiment of the present invention.

Figure 6 shows the electrical equipotential distribution for the self-isolated LDD lateral DMOS transistor 500 of Figure 5.

Figure 7 shows a self-isolated LDD lateral DMOS transistor 600 with an N-well 606, in accordance with another embodiment of the present invention.

Figure 8 compares the electric field distributions of the LDD lateral DMOS transistor of Figure 1, the LDD lateral DMOS transistor of Figure 2 (i.e. with a gate plate) and the LDD lateral DMOS transistor 500 of Figure 5, provided in accordance with the present invention.

Figure 9 shows high-voltage LDD lateral DMOS transistor 900 in accordance with the present invention integrated with low-voltage CMOS transistors 903 and 904 each using P+ and N+ buried layers to suppress the CMOS latch up phenomenon.

Figure 10a is a cross section of a self-isolated LDD lateral DMOS transistor 1000 having a partial inactive edge 1051 and a P+ buried layer 501 underneath the partial inactive edge, in accordance with the present invention.

Figure 10b is a top view of the self-isolated lateral DMOS transistor 1000 shown in Figure 10a.

Figure 11 is a cross section of a self-isolated LDD diode 1100 having a P+ buried layer 501 underneath a drift region 522, the drift region 522 being formed beneath a field oxide layer 1050, in accordance with the present invention.

Figure 12 is a cross section of a self-isolated LDD lateral DMOS transistor 1200 having a P+ buried layer 501 partially overlapped by the N- drift region 1222; the N- drift region 1222 being formed beneath a field oxide layer 1250, in accordance with the present invention.

Figure 5 shows a cross section of an LDD lateral DMOS transistor 500 provided in accordance with one embodiment of the present invention. LDD lateral DMOS transistor 500 is a substantially annular structure in which the gate 509, the drift region 522 and the P+ buried layer 501 (see below) surround the drain region on all sides.

In this embodiment, as shown in Figure 5, LDD lateral DMOS transistor 500 is formed in a lightly-doped P- epitaxial layer 512 on top of a P- substrate 505. The epitaxial layer 512 has a dopant (e.g. boron) concentration typically $1.0 \times 10^{14}/cm^3$ to $5.0 \times 10^{14}/cm^3$, although the dopant concentration can be as high as $8.0 \times 10^{15}/cm^3$. The depth of the epitaxial layer is chosen according to the intended operational conditions of all devices in the integrated circuit. Likewise, the resistivity of the P- (e.g. boron-doped) substrate 505 is chosen with consideration of the intended maximum operational voltage of all devices integrated with transistor 500 in the integrated circuit. For up to 500 volts, a 30-50 ohms-cm resistivity can be used. However, for higher voltage operations (e.g. 1000 volts or higher), a higher resistivity, even up to several hundred ohms-cm, can be used.

The P- epitaxial layer 512 can be deposited by high temperature chemical vapor deposition, or any other suitable technique known in the art. Before forming the P- epitaxial layer 512, the P+ buried layer 501 is formed by conventional technique, such as ion implantation, near the surface of the P- substrate 505. In the course of forming the P- epitaxial layer 512, the P+ buried layer

501 back diffuses towards the surface of the P- epitaxial layer 512. Dependent upon the number of thermal cycles in the process, an initial dopant concentration is provided such that the final dopant concentration of the P+ buried layer 501 is in the order of $10^{16}/cm^3$. In this embodiment, a $5.0 \times 10^{14}/cm^2$ implant dose of boron at 60 KeV provides the desirable final dopant concentration in the P+ buried layer 501. Since the back diffusion can be as much as 8 microns, this thickness limits the minimum depth the P- epitaxial layer 512 can be.

Figure 5 shows a deep P+ region 504 which, though not necessary, provides a better contact between the P-body region 503 and the P- substrate 505. If ion implantation is used to form the deep P+ region 504, a boron dose in excess of $10^{15}/cm^2$ at 60KeV can be used. Alternatively, the P+ region 504 can be formed using a P+ predeposition from a gaseous or solid boron source. The P-body region 503 determines the threshold voltage of the LDD lateral DMOS transistor 500. The implant dose (at 60 KeV) used to form the P-body region 503 ranges from $1.0 \times 10^{13}/cm^2$ to $9.0 \times 10^{13}/cm^2$, dependent upon the desired threshold voltage, with a typical dose of $5.0 \times 10^{13}/cm^2$. The threshold voltage for common N+/P-body junction depths vary from 0.7 volts to 3.0 volts, depending on the net profile as determined by the interaction in the junction between N+ 502 and P-body region 503. In this embodiment, in the course of fabrication, the P-body region 503 down-diffuses as deep as 4 microns into the substrate. Unlike the RESURF type LDD lateral DMOS transistor, such as transistor 200 shown in Figure 4, there is no reversed-bias junction in the vicinity of the P-body region 503. A reversed-bias junction is formed between the N+ drain 507 and the P- epitaxial layer 512, which is too far from the P-body region 503 to contribute to punchthrough breakdown degradation of the transistor 500.

The N+ source region 502 and the N+ drain region 507 are formed using conventional techniques with an implant

dose of 5.0 x $10^{15}/cm^2$ or higher. In this embodiment, 50%-50% mixture of phosphorus and arsenic is used, although either dopant can be used without the other. Because of the benefits of the present invention (explained below), the drift region can be formed with a total implant dose (e.g. phosphorous) up to $4.0x10^{12}/cm^2$, which is approximately four times the dopant implant dose of drift regions attainable in the prior art. The on-resistance of this transistor 500 is therefore much reduced from that of LDD lateral DMOS transistors in the prior art.

An optional N-well 506 can also be provided. When provided, N-well 506 can be 3-12 microns deep, with a dopant concentration (e.g. phosphorous) between $1.0x10^{15}/cm^3$ to $2.0x10^{16}/cm^3$. If the N-well 506 is implanted, an implant dose (e.g. phosphorous) of $3.0-8.0x10^{12}/cm^2$ at 60-100KeV can be used to provide a typical surface concentration of substantially $8.0x10^{15}/cm^3$. In addition to allowing integration with P-MOS transistors, the optional N-well 506 provides additional field-shaping flexibility (explained below).

An optional P+ region 513 (e.g. boron-doped) provides a source-P-body shunt and provides better contact to the P-body region 503. If the P+ region 513 is not provided, the P-body region 503 contacts the source/body contact 520 directly, or in combination with deep P+ region 504. The gate oxide 510 and the gate 509 of transistor 500 are formed using conventional method.

Significantly, in the structure shown in Figure 5, unlike the RESURF type lateral DMOS transistor, there is not a high-gain parasitic vertical NPN transistor susceptible to BV_{CEO} snapback. The BV_{CEO} snapback phenomenon is discussed above in conjunction with the RESURF type DMOS transistor 200 of Figure 4. In this embodiment, there is only a parasitic lateral NPN transistor having a long base (hence, lower gain) formed by the source and drain regions 502 and 507, and the P-epitaxial and P-body regions 512 and 503. Hence,

transistor 500 is less likely to exhibit BV_{CBO} snapback.

In this embodiment, an optional gate plate 511 (e.g. aluminum) is provided for reducing the electric field crowding on the silicon surface in the manner already discussed above in conjunction with the gate plate shown in Figure 2. Significantly, if reduction of the electric field at the drain-edge of the drift region 522 is desired, the conducting material 508 at the drain contact region 507 can also be made to extend over the insulation layer 521 beyond the drain-edge of the drift region 522 forming a field plate.

The electrical equipotential distribution of transistor 500 is shown in Figure 6. As shown in Figure 6, the presence of the P+ buried layer 501 pushes the electrical equipotential lines beneath the silicon surface laterally further and more evenly in the direction of the drain contact region 507. In this manner, the crowding of electrical equipotentials indicated by arrow A in Figure 3 is relieved by the presence of P+ buried layer 501. Hence, the breakdown voltage of LDD DMOS transistor 500 is enhanced by both the reduction of the electric fields at the gate-edge of the drift region 522, and by the shifting of the electric fields into the bulk silicon away from the surface charges. Because of this breakdown voltage enhancement, the dopant concentration in the drift region 522 can be increased up to four times over the prior art, correspondingly reducing the on-resistance of the transistor 500, thereby increasing LDD lateral DMOS transistor 500's ability to sustain a higher current. Furthermore, because the breakdown remains in the bulk, the avalanche breakdown voltage remains stable, and the charging of the overlying oxide 521 is minimized.

Figure 7 shows in another embodiment of the present invention the electrical equipotential distribution of an LDD lateral DMOS transistor 600 having an N-well 606. For convenience of comparison, like structures of transistors 500 and 600, respectively, of Figures 5 and 7 are given

the same reference numerals. Figure 7 shows that N-well 606 also pushes the electrical equipotentials of transistor 600 further into the bulk silicon and away from the surface charges. Hence, controlling the depth of N-well 606 provides further field-shaping flexibility for tailoring transistor 600 to the desired breakdown characteristics. N-wells, such as N-well 606, are commonly used for operating voltages above 200 volts, but are less commonly used if the operating voltage is less than 200 volts. This is because desirable breakdown characteristics are more easily achieved at less than 200 volts. An N-well also reduces the on-resistance of the high voltage transistors.

Figure 8 compares the electric field intensities along the silicon surface of (a) an LDD lateral DMOS transistor in the prior art similar to that shown in Figure 1; (b) an LDD lateral DMOS transistor similar to the transistor in (a), but having a gate plate such as the gate plate 802 shown; and (c) an LDD lateral DMOS transistor having a P+ buried layer, such as P+ buried layer 801 shown in accordance with the present invention. In Figure 8, the transistor in (a) is represented by the structure 800, minus the gate plate 802 and the P+ buried layer 801; the transistor in (b) is represented by the structure 800, minus the P+ buried layer 801; and the transistor in (c) is represented by the structure 800, with both the gate plate 802 and the P+ buried layer 801. All three transistors in (a) and (b) and (c) have the drain plate 804. The drain plate 804 modifies the field distribution at the drain-edge of the drift region 805, in the manner discussed above.

In Figure 8, the electric field intensities along the surface of the silicon is plotted against the distance in the x-direction. As shown in Figure 8, the curves labelled 820, 821 and 822 represent respectively the electric field intensity profiles of the transistors in (a), (b) and (c) described above. It is readily seen that

in all three curves 820, 821 and 822, the electric field intensity peaks at the gate-edge (point x_1) of the drift region 805, and approaches zero at the drain-edge (point x_4) of the drift region 805. As expected, the highest electric field intensity at point x_1 corresponds to the transistor in (a). In the transistor of (a), the electric field intensity (curve 820) rapidly falls off as the distance from the gate-edge of the drift region increases. The electric field in this instance, decreases at a rate which is moderated by the presence of the drain plate 804 between points x_3 and x_4. In the transistor of (b), the electric field intensity (curve 821) is more or less level for the region underneath the gate plate 802, and then decreases at a substantially constant rate similar to the rate of decrease shown in curve 820, as one moves beyond the extent of the gate plate 802 at point x_2 towards point x_4. As curves 820 and 821 illustrate, both the gate and the drain plates 802 and 804 have a levelling effect on the electric field intensity along the silicon surface under these plates. However, in accordance with the present invention and shown by the curve 822, transistor (c) having the P+ buried layer 801 has a substantially uniform electric field intensity profile along the entire length (x_1 to x_4) of the drift region 805.

In addition to the benefits discussed above, the P+ buried layer, such as P+ buried layer 501 of transistor 500 of Figure 5, reduces the injected minority carrier lifetime, thereby improving the reverse-recovery characteristics in the diode formed by the drain 507, the P- epitaxial layer 512 and the P- substrate 505. Further, at the same time when the P+ buried layer 501 is formed, P+ buried layers can also be formed beneath the low-voltage NMOS transistors used to implement the circuits, such as logic circuits, integrated on the same semiconductor substrate. The buried layers under such low-voltage NMOS transistors reduce the integrated circuit's susceptibility to the CMOS latch-up condition.

Figure 9 shows an LDD lateral DMOS transistor 901 formed in an annular fashion, integrated on the same substrate as two low-voltage CMOS transistors 903 and 904. In Figure 9, the P+ buried layers 905 and 906 serve not only as field-shaping structures for transistor 901, but also as a latch-up suppressing structure for NMOS transistor 904. Hence, from a top view, the drift, drain, P-body, the various P+ buried regions, and other structures of LDD lateral DMOS transistor 901 are annular structures. For example, as shown in Figure 9, the conductor 910 which connects both the P-body regions and source regions of LDD lateral DMOS transistor 901 is shown in Figure 9 as annular.

Figure 10a shows an LDD lateral DMOS transistor 1000, which is similar to transistor 500 of Figure 5, except that in transistor 1000, only a portion of the drift region 522 borders an active channel region under the gate 1009. That is, unlike gate 509 of transistor 500, gate 1009 of transistor 1000 is not an annular structure surrounding the drain region 507. Again, for convenience of comparison, the same reference numerals in Figures 5 and Figures 10a denote structures which are functionally and structurally alike. Further, even though given different reference numerals, the source/bulk contact 1020, the P+ region 1013, and the P-body region 1003 of transistor 1000, are similar in function to corresponding source/bulk contact 520, the P+ region 513 and the P-body region 503 of transistor 500, and can be formed in substantially the same manner as described above for transistor 500.

As shown in Figure 10a, a field oxide region 1050 is formed by a LOCOS process known in the art. This oxide region 1050, which is typically between 5000Å to 2 microns thick, is formed prior to formation of gate 1009 and shown in Figure 10a to abut the drift region 522 on the side of the drift region 522 away from the channel region. The interface 1051 between the drift region 522 and the field

oxide region 1050 is known as the "inactive edge", and the interface 1052 between the drift region 522 and the channel region is known as the "active edge." As mentioned above, as in the gate-edge, dependent upon the resistivity of the drift region 522, an adverse high electric field may develop at the inactive edge 1051. This adverse high electric field may be further increased by the presence of P-type field dopant, or by stress-induced crystalline defects present at the interface between oxide region 1050 and the drift region 522. One source of such crystalline defects is the LOCOS field oxidation step mentioned above. Therefore, in accordance with the present invention there is provided underneath the inactive edge a portion of the P+ buried layer 501. This portion of the P+ buried layer 501 pushes the electrical equipotential lines away from the inactive edge 1051 and into the bulk silicon in substantially the same manner as provided by the P+ buried layer 501 underneath the active edge 1052 described above.

The top view of one possible layout of the transistor 1000 is shown in Figure 10b. In Figure 10b, the inactive edge 1051 and the active edge 1052 are shown to be on opposite sides of the drain region 507. The extent of the P+ buried layer 501, the drift region 522, and the optional gate plate 511 are indicated respectively by bidirectional arrows 1061, 1062 and 1063. Field oxide 1050 lies outside the solid rectangle, 1057. Gate 509, source/bulk contact 520, and the source region 502 are also indicated.

In the technology described above, a diode structure can result from eliminating the active gate from an LDD lateral DMOS transistor, such as transistor 1000 of Figure 10a. Such a diode is shown in Figure 11, giving the same reference numerals to corresponding structures in Figures 10a and 11. In Figure 11, a diode is formed by the P substrate 505 (anode), the P-epitaxial layer 512 and the drain region 507 (cathode). The P substrate layer is

connected in common with the source contact 1020, and the P+ region 1013. As in transistor 1000, the P+ buried layer 501 pushes the electrical equipotential lines away from the inactive edge 1051 and into the bulk silicon to relieve high electric field that can developed at the inactive edge. In addition, as mentioned above, the P+ buried layer 501 reduces the injected minority carrier lifetime, and thereby improves the cathode-to-anode reverse-recovery characteristics of the diode.

Figure 12 is another embodiment of the present invention in an LDD lateral DMOS transistor 1200, in which a field oxide region 1250 is formed over the drift region 1222. Like transistor 500 of Figure 5, transistor 1200 is a substantially annular structure having gate 1209, drift region 1222, and the P+ buried layer 501 surround the drain region 507. Again, for the convenience of comparison, like structures of the transistors 500 and 1200 (Figures 5 and 12) are given the same reference numerals. The like structures of transistors 500 and 1200 can be formed in substantially the same manner as described above for transistor 500. In addition, the drift region 1222 can be formed in the same manner as the drift region 522 of transistor 500. Of significance in transistor 1200 is the field oxide layer 1250 not found in transistor 500 of Figure 5. This field oxide region 1250, which may be formed by the LOCOS process mentioned above, is distinguished from other available oxide layers in that it can be any thick oxide formed prior to the formation of gate 1209, thereby allowing an overlap of the gate 1209 to be formed over part of the field oxide 1250, as shown in Figure 12. This overlap by the gate over the field oxide 1250 forms an effective gate plate to prevent high electric field at the interface 1251 between the channel region 1253 and the drift region 1222, thereby further enhancing the breakdown voltage of transistor 1200.

The above detailed description and the accompanying drawings are intended to illustrate the specific embodi-

ments of the present invention and not intended to limit the present invention. Various modifications and variations within the scope of the present invention are possible. For example, it is within the ability of one of ordinary skill to provide P-channel analog of the N-channel LDD lateral DMOS transistor 500, by reversing the conductivity of all the relevant semiconductor regions, upon consideration of the above detailed description and the accompanying drawings. As another example, it is also known that the P+ body contact region 513 and the N+ contact region 502 may be separated electrically, allowing a low voltage reversed bias of a few volts to be impressed across the source-to-body junction without significantly altering the conduction or breakdown characteristics of the device. Such modification is within the scope of the present invention. The scope of the present invention is defined by the following claims.

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CLAIMS

1. A lateral DMOS transistor structure, comprising:

an epitaxial layer of a first conductivity formed on one surface of a substrate of the first conductivity;

a source region of a second conductivity formed in the epitaxial layer opposite the first conductivity;

a body region of the first conductivity formed in the epitaxial layer adjacent the source region, a portion of the body region being exposed on the surface of the epitaxial layer;

a drift region of the second conductivity formed in the epitaxial layer and spaced from the source and the body regions by an exposed portion of the epitaxial layer on the surface of the epitaxial layer away from the surface of the substrate, such that the exposed portion of the body region and the exposed portion of the epitaxial layer form a channel region between the source region and the drift region;

a drain region of the second conductivity formed in the epitaxial layer adjacent the drift region away from the channel region;

a gate region formed above the channel region; and

a buried layer of the first conductivity having a portion located underneath the interface between the channel and the drift regions.

2. A structure as claimed in claim 1 having a gate plate located above the gate and extending over the interface between the channel and drift regions.

3. A structure as claimed in claim 1 or 2 having a drain plate located above the drain region and extending over the interface between the drift and drain regions.

4. A structure as claimed in claim 1, 2 or 3 which is substantially annular about the drain region.

5. A lateral DMOS transistor structure, comprising:

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an epitaxial layer of a first conductivity formed on one surface of a substrate of the first conductivity;

a gate region above the epitaxial layer, the gate defining on the surface of the epitaxial layer a channel region underneath the gate;

a source region of a second conductivity opposite the first conductivity in the epitaxial layer having a portion exposed on the surface of the epitaxial layer region adjacent the channel region;

a body region of the first conductivity formed in the channel region in the epitaxial layer adjacent the source region;

a drift region of the second conductivity formed in the epitaxial layer adjacent the channel region away from the body region;

a drain region of the second conductivity formed in the epitaxial layer adjacent the drift region;

an oxide region adjacent the drift region and located away from the interface between the channel region and the drift region; and

a buried layer of the first conductivity having a portion located underneath the interface between the drift region and the oxide region.

6. A structure as claimed in claim 5 wherein the buried layer has a second portion located underneath the interface between the channel and drift regions.

7. A structure as claimed in claim 5 or 6 having a gate plate above the gate extending over the interface between the channel and the drift regions and extending along the boundary of the drift region to provide a portion of the gate plate above the interface between the oxide layer and the drift region.

8. A structure as claimed in any preceding claim having a deep diffusion region of the first conductivity in the

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epitaxial layer and adjacent the body region.

9. A structure as claimed in any preceding claim having a deep diffusion region of the second conductivity in the epitaxial layer and adjacent the drain region.

10. An LDD DMOS transistor structure, comprising:

a buried layer of a first conductivity formed on a surface of a substrate of the first conductivity;

an epitaxial layer of the first conductivity formed on the surface of the substrate;

a drift region of a second conductivity formed in the epitaxial layer, a portion of the boundary of the drift region being located above the buried layer;

an oxide layer formed above the drift region;

a gate formed above the epitaxial layer such that the portion of the epitaxial layer underneath the gate is adjacent the portion of the boundary of the drift region, the portion of the epitaxial layer forming a channel region;

a body region formed in the epitaxial layer and having a portion in the channel region exposed on the surface of the epitaxial layer, the exposed portion of the body region being located away from the drift region;

a source region of the second conductivity formed in the epitaxial layer adjacent the channel region and the exposed portion of said body region;

a drain region of the second conductivity formed in the epitaxial layer adjacent the drift region away from the channel region.

11. A structure as claimed in claim 10 having a deep diffusion region of the first conductivity in said epitaxial layer adjacent the body region and the buried layer.

12. A structure as claimed in claim 10 or 11

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wherein the gate extends over the oxide region forming a gate plate above the interface between the channel and drift regions.

13. A self-isolated diode structure, comprising:

a buried layer of a fist conductivity formed on one surface of a substrate of the first conductivity;

an epitaxial layer of the first conductivity formed on the surface of said substrate;

an oxide layer formed on top of the epitaxial layer, the oxide layer partially covering the epitaxial layer, and exposing first and second regions of the epitaxial layer, a portion of the boundary of the first region being located above the buried layer;

a drift region of a second conductivity formed in the first region of the epitaxial layer adjacent the oxide layer at the potion of the boundary;

a cathode region of the second conductivity formed in the first region of the epitaxial layer adjacent the drift region away from the portion of the boundary, and

an anode region of the first conductivity formed in the second region of the epitaxial layer adjacent the oxide layer.

14. A structure as claimed in claim 13 having a deep diffusion region of the first conductivity in the epitaxial layer adjacent the anode region and the buried layer.

15. A structure as claimed in any preceding claim wherein the first conductivity is p-type and the second conductivity is n-type.

16. A method of providing an LDD lateral DMOS transistor, comprising the steps of:

providing a buried layer of a first conductivity on one surface of the substrate of the first conductivity;

providing an epitaxial layer of the first

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conductivity above the surface of the substrate;

providing a gate above the surface of the epitaxial layer, thereby defining a channel region underneath the gate on the surface of said epitaxial layer;

providing a drift region of a second conductivity adjacent the channel region such that the interface between the channel and drift regions is located above the buried layer;

providing a body region of the first conductivity having a portion exposed on the surface of the epitaxial layer in the channel region away from the drift region; and

providing source and drain regions of the second conductivity in the epitaxial layer, the source region being adjacent the channel region and the exposed portion of the body region, and the drain region being adjacent the drift region away from the channel region.

17. A method as claimed in claim 16 having the step of providing a gate plate above the gate extending over the interface between the channel and drift regions.

18. A method as claimed in claim 16 or 17 having the step of providing a drain plate above the drain region extending over the interface between the drift and drain regions.

19. A method as claimed in claim 16, 17 or 18 wherein the transistor structure is substantially annular about the drain region.

20. A method of providing an LDD lateral DMOS transistor, comprising the steps of:

providing a buried layer of the first conductivity above one surface of a substrate of the first conductivity;

providing an epitaxial layer of the first

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conductivity on the surface of the substrate;

providing an oxide layer above the surface of the epitaxial layer, the oxide layer partially covering the surface of the epitaxial layer and exposing a region of the epitaxial layer;

providing a gate above the region of the epitaxial layer away from the oxide layer, thereby defining underneath the gate in the region of the epitaxial layer a channel region, and such that a portion of the boundary of the channel region lies above a first portion of the buried layer;

providing a drift region of a second conductivity at the surface of the epitaxial layer adjacent the portion of the boundary of the channel region and adjacent the oxide layer, such that the interface between the oxide layer and the drift region lies above a second portion of the buried layer;

providing a body region in the epitaxial layer and having a portion of the body region exposed on the surface of the epitaxial layer in the channel region away from the drift region; and

providing source and drain regions of the second conductivity at the surface of the epitaxial layer, the source region being adjacent the exposed portion of the body region, and the drain region located between the oxide layer and the channel region adjacent the drift region.

21. A method as claimed in claim 20 having the step of providing a gate plate above the gate and extending over the portion of the boundary of the channel region.

22. A method as claimed in claim 20 or 21 having the step of providing a drain plate above the drain and extending over the interface between the oxide and drift regions.

23. A method as claimed in any one of claims 16-22

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having the step of providing a deep diffusion region of the first conductivity in the epitaxial layer adjacent the body region.

24. A method as claimed in any one of claims 16-23 having the step of providing a deep diffusion region of the second conductivity in the epitaxial layer adjacent the drain region.

25. A method of providing an LDD DMOS transistor structure, comprising the steps of:

providing a buried layer of a first conductivity on a surface of a substrate of the first conductivity;

providing an epitaxial layer of the first conductivity on the surface of the substrate;

providing a drift region of a second conductivity in the epitaxial layer, a portion of the boundary of the drift region being located above the buried layer;

providing an oxide layer above the drift region;

providing a gate above the epitaxial layer such that the portion of the epitaxial layer underneath the gate and adjacent the portion of the boundary of the drift region forms a channel region;

providing a body region in the epitaxial layer, the body region having a portion exposed on the surface of the epitaxial layer in the channel region, the exposed portion of body region being located away from the drift region; and

providing source and drain regions of the second conductivity, the source region being formed in the epitaxial layer adjacent the portion of the body region and the drain region being formed in the epitaxial layer adjacent the drift region away from the channel region.

26. A method as claimed in claim 25 having the step of providing a deep diffusion region of the first conductivity in the epitaxial layer adjacent the body region and the

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buried layer.

27. A method as claimed in claim 25 or 26 wherein the gate extends over the oxide region formed prior to the gate providing step, thereby forming a gate plate above the interface between the channel and drift regions.

28. A method of providing a self-isolated diode structure, comprising the steps of:

providing a buried layer of a first conductivity on one surface of a substrate of the first conductivity;

providing an epitaxial layer of the first conductivity on the surface of the substrate;

providing an oxide layer on top of the epitaxial layer, the oxide layer partially covering the epitaxial layer, and exposing first and second regions of the epitaxial layer, a portion of the boundary of the first region being located above the buried layer;

providing a drift region of a second conductivity in the first region of the epitaxial layer adjacent the oxide region at said portion of the boundary;

providing a cathode region of the second conductivity in the first region of the epitaxial layer adjacent the drift region away from said portion of the boundary; and

providing an anode region of the first conductivity in the second region of the epitaxial layer adjacent the oxide region.

29. A method as claimed in claim 28 having the step of providing a deep diffusion region of the first conductivity in the epitaxial region adjacent the anode region and the buried layer.

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