CLAIMS

1. A method, comprising:

forming a silicon on insulator (SOI) over a wafer;

depositing a metal on the SOI;

forming a structure by dry-etching the metal and dry-etching the SOI;

forming a template over the structure;

etching a portion of the SOI for removal under the metal; and

growing a semiconductor where the portion of SOI was removed, wherein an interface between the metal and the semiconductor is formed in situ during growth of the semiconductor.

2. The method according to the preceding claim, wherein the metal comprises: TiN, a superconductor, a non-superconductor, ferromagnetic metal, or a combination thereof.

3. The method according to any of the preceding claims, further comprising:

exposing the SOI using a hydrofluoric acid etch prior to etching the portion of the SOI for removal.

4. The method according to any of the preceding claims, wherein the template determines a geometry of the semiconductor.

5. The method according to any of the preceding claims, wherein growing the semiconductor is implemented using metal-organic vapor phase epitaxy (MOVPE).

6. The method according to any of the preceding claims, further comprising:

depositing a dielectric on the SOI prior to depositing the metal.

7. A method, comprising:

forming a template structure comprising a metal element and a silicon element by etching a portion of the silicon element for removal; and

creating an interface between the metal element and a semiconductor by growing the semiconductor where the portion of the silicon element was removed, wherein

the interface between the metal layer and the semiconductor is created in situ during the growing of the semiconductor.

8. The method according to the preceding claim, wherein the silicon element comprises: silicon-on-insulator, polycrystalline silicon, or a combination thereof.

9. The method according to any of the two preceding claims, wherein a residual portion of the silicon element that remains after the etching provides a nucleation seed from which growth of the semiconductor commences.

10. The method according to any of the three preceding claims, wherein the semiconductor is a group III-V semiconductor.

11. The method according to any of the four preceding claims, wherein the template structure further comprises a dielectric layer overlaying the metal element and the silicon element.

12. The method according to any of the five preceding claims, further comprising:

dry-etching a metal layer and a silicon layer in a single step to self-align the metal element and the silicon element.

13. The method according to any of the six preceding claims, wherein the silicon element comprises a (110) crystal orientation.

14. The method according to any of the seven preceding claims, wherein the template structure is formed on a silicon wafer.

15. A method, comprising:

forming a cavity structure including a first side wall comprising a metal element and a second sidewall comprising a silicon element; and

growing a semiconductor within the cavity structure using the silicon element as a nucleation seed to form an interface between the metal element and the semiconductor, wherein the interface between the metal element and the semiconductor is

formed in situ during the growing of the semiconductor.

16. The method according to the preceding claim, wherein the cavity structure overlays a silicon-on-insulator wafer.

17. The method according to any of the two preceding claims, wherein forming the cavity structure comprises:

etching a portion of the silicon element for removal

18. The method according to any of the three preceding claims, wherein a length of the cavity structure corresponds with an etch time used to form the cavity structure.

19. The method according to any of the four preceding claims, wherein a height of the semiconductor is determined by a thickness of a dielectric layer overlaying the cavity structure.

20. The method according to any of the five preceding claims, wherein growth of the semiconductor is guided by one or more geometries of the cavity structure.