

PATENT SPECIFICATION

(11) 1 254 537

DRAWINGS ATTACHED



- (21) Application No. 57129/68 (22) Filed 2 Dec. 1968
 (31) Convention Application No. 79702 (32) Filed 12 Dec. 1967 in
 (33) Japan (JA)
 (45) Complete Specification published 24 Nov. 1971
 (51) International Classification G 06 f 3/14 G 06 k 15/18 G 11 c 19/00
 (52) Index at acceptance
 G4A 10EX 10F10 10FY 15A2 15B 16G 18F 18Y 1C1A 1C2
 1C4A 2A1 2AY 2B1 2B2 2BY 2C 3W10W2 3W10Y
 3W2 4X 5A 6B 6E 8C 9F
 G4C 1B 2E 2JX 4A
 G4H 13D 14B 3C 4G 6A 6B 6E 6F 7B 8B 8D 9E
 H3T 1C1 1H 1M2P 1P2 2B2 2B3 2F1 2F5 2J 2T3F 3F1 3J 3X
 4C 4M 4R 4S 5E

- (72) Inventors ISAMU WASHIZUKA
 HITOSHI HANAHARA and
 SATOSHI TERAMURA

(54) DIGITAL COMPUTER APPARATUS

(71) We, SHARP KABUSHIKI KAISHA, a Japanese Company (formerly HAYAKAWA DENKI KOGYO KABUSHIKI KAISHA) of 22-22 Nagaike-cho, Abeno-ku, Osaka, Japan, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to a digital computer apparatus, especially to a relatively small-scale operation device suitable for an electronic computer of the table type.

In a table type electronic computer or like computing device, it is necessary to perform small-scale arithmetic processes such as decimal point positioning, in addition to the numerical processing. For example, addition of the numbers of digits above the decimal point in operands is required in multiplication, and subtraction of said numbers is required in division. In order to execute such decimal point processing, an adder and its control device are needed as in the case of normal numerical processing.

In order to provide for small size and little weight, however, it is necessary to avoid adding a large-scale device for decimal point processing in multiplication and division and to take care that the device does not become bulky. Although the use of ordinary adders and their co-operating devices can be considered for numerical processing for this purpose, a number of logic gates must be added to said adders and co-operating devices and it is troublesome to control them.

Recently, circuit integration technique has been remarkably developed also in the field of electronic table computers and other digital equipment and it tends to integrate all circuit elements of each block in a single

semi-conductor substrate. In accordance with this tendency, it is proposed, for example, to integrate the numerical processing section and decimal point processing section and their co-operating sections as a single block. As described above, in the case of the adders in the numerical processing section for the decimal point processing facility, interconnections between the blocks are required and the number of terminals of the integrated semiconductor device is correspondingly increased. This fact (increase of the number of terminals) is undesirable in view of geometrical limitation of the container.

If, from these circumstances, the decimal point processing section is provided with an adder and its co-operating device similar to those in the numerical processing section, a digital operation device of same scale as in the numerical processing section will be constituted in the decimal point processing section although only a small-scale use of this device is required. This is undesirable.

Therefore, an object of this invention is to provide an improved digital operation device in which the number of additional devices can be considerably reduced in comparison with conventionally known operation devices.

A further object of this invention is to provide a digital operation device suitable especially for integration of the whole circuit and having few outer terminals when assembled in a single integrated circuit.

Another object of this invention is to provide a digital operation device suitable for an electronic computer of the table type and like computing devices and, especially, for small-scale arithmetic operations such as decimal point processing.

According to this invention, a semicon-

ductor decimal point indicating device includes at least two registers with one register storing numerical information consisting of a word or words each containing a predetermined number of digits and the other register storing information relating to the position of the decimal point in the numerical information stored in said one register, said other register including a plurality of pairs of transistors each pair connected one to the other for storing one bit of said decimal point information, a generator for least one set of timing signals corresponding in number to the number of digits and determining the boundaries of each word time, decimal point processing means including logical gating circuits connected to said generator, and connections between said decimal point processing means and said other register, said decimal point processing means modifying the information stored in the decimal point register in accordance with the new decimal point information at the termination of each set of timing signals, the modified decimal point information being read out during a period of one timing signal within each word time, and the position of one timing signal in the set of timing signals determining the decimal point position of the resulting information, and time sharing indicating means connected with said generator, the last said means including decimal point indicating elements connected in parallel to said decimal point processing means and actuated by the decimal point information at a period of one timing signal during each word time.

In order that the invention may be clearly understood and readily carried into effect, apparatus for use in an electronic computer of the table type will now be described, by way of example, with reference to the accompanying drawings, in which:—

Figure 1 is a block diagram representing the structure of a conventional computer system,

Figure 2 is a time chart representing a relation between a clock pulse and a bit timing pulse in one embodiment of the computer system according to the invention,

Figure 3 is a time chart representing a relation between a bit timing pulse and digit timing pulse,

Figure 4 is a block diagram showing the structure of the main portion of the computer system according to this invention,

Figures 5-1 to 5-5 are diagrams for assisting the explanation of the operation of the computer system shown in Figure 4,

Figure 6 is a diagram representing the logic constitution of a clock pulse control device shown in Figure 4,

Figures 7-1 and 7-2 are diagrams representing a logic constitution of a detector device shown in Figure 4,

Figure 8 is a diagram representing a practical circuit embodiment of decimal point registers shown in Figure 4,

Figure 9 is a diagram for assisting the explanation of the operating of the circuit of Figure 8,

Figures 10-1 to 10-3 are diagrams representing another circuit embodiment of the decimal point registers shown in Figure 4,

Figure 11 is a diagram representing a practical circuit configuration of the clock pulse control device shown in Figure 4,

Figure 12 is a diagram representing a circuit embodiment of the detector device shown in Figure 4, and

Figure 13 is a block diagram representing the structure of an indication section of the computer system according to this invention.

Referring to Figure 1 representing the structure of a conventional table type electronic computer, two kinds of inputs for controlling the whole system, that is, information relating to numerical values and an instruction relating to operation processing, are introduced in the computer by means of an input device 1. Said input device 1 includes a ten-key type key board 2 provided with numeral keys "0" to "9", a decimal point key and operational function keys such as "x" (multiplication), "÷" (division) and "=" (equal). The input device 1 introduces the signals relating to numerical values and operation processing according to selected keys pressed by an operator. The numerical processing section of the input device 1 is directly coupled to a first register 3 and a first decimal point register 31 and numerical information and decimal point information are respectively written in said first register 3 and said first decimal point register 31. The operation indication section of the input device 1 is directly coupled to a programmer 4 and a conditional flip-flop 5. In the case of a write-in operation of two operands, the first operand is written in the first register 3 and then transferred to the second register 6 and the second operand is thereafter introduced in the vacant register 3. In connection therewith, the decimal point portions of said two operands are similarly written in the first decimal point register 31 and the second decimal point register 61. A memory 7 and a third decimal point register 8 co-operating therewith are provided for use in multiplications by a constant number or in the addition or subtraction of products.

In the following description, it is assumed for explanation purpose that the numerical values processed in this computer system are of binary coded decimal notation (four bits in each digit) and the maximum capacities of the registers 3 and 6 and the memory 7 are sixteen digits (4×16 bits). The maximum capacities of the decimal point registers 31 and 61 are sixteen bits.

The output from the first register 3 and the output from the second register 6 or the memory 7 are both introduced in an arithmetic unit 9 and a predetermined operation is executed therein. Said arithmetic unit includes therein a full adder having addition capability of pure binary numbers, a carry memory and a decimal decoding correction device. Multiplication and division are executed using methods of repeated addition and repeated subtraction respectively. It should be noted, in this case, that the outputs of the decimal point registers 31 and 61 are not introduced in the arithmetic unit 9. A buffer register 10 is required for temporarily storing a content to be indicated and for providing a decimal output for actuating an indication tube when displaying a result of an operation or a content of the register by the use of the indication tube, which may be a gas-filled glow discharge tube. Similarly, a second buffer register 11 is provided for temporarily storing the decimal point information when this is to be displayed.

The programmer 4 generates micro orders necessary for execution of various operations in a diode matrix system. The micro orders are introduced in the inputs of logic gates provided between various sections of the device to control the passage of numerical information. In operation of said programmer 4, when, for example, several input address lines are provided for multiplication and one of said address lines is selected, a plurality of output lines coupled thereto through diodes are driven to generate several kinds of micro orders to control information transfer between related devices.

An address counter 12 is provided for sequentially designating the programme address lines with the advance of the operation processes. The conditional flip-flop 5 is provided for detecting properly the internal conditions of the various devices during the progress of the computation and selecting the programme address lines based upon its detector output to generate micro orders corresponding to the cases, thereby achieving a high efficiency of operation. Further flip-flops are provided for detection. A clock pulse generator 13 is provided for generating clock pulses used as a standard of synchronous control of the various devices. A timing signal generator 14 variously modifies said clock pulses to produce bit timing signals and digit timing signals. A relation between the clock pulse generator 13 and the decimal point processing section will now be described in detail.

In the embodiment herein described, the clock pulse generator 13 is provided with three oscillators and generates three kinds of clock pulses ϕ_1 , ϕ_2 and ϕ_3 , as shown in Figure 2, having different phases which are to be

introduced in the various registers. Said clock pulses transfer and circulate information stored in the memory cells of the registers 3 and 6 and in the decimal point registers 31 and 61 through said registers. The digit timing signals T_1 , T_2 , ..., T_{16} in Figure 3 represent a time scale indicating weights of digits in the case of viewing the information serially circulating through the registers at the output terminal of said registers and designate the boundaries of each word time (16 digits in each word). The bit timing signals t_1 , t_2 , t_3 and t_4 indicate weights 8, 4, 2 and 1, respectively, in each digit. As shown in Figures 2 and 3, the duration of one digit timing signal includes four bit timing signals and the duration of one bit timing signal includes three clock pulses ϕ_1 , ϕ_2 and ϕ_3 . However, these three kinds of clock pulses are not always required according to circuit configuration of the memory cell.

The relation between the decimal point registers 31 and 61 and the clock pulse generator 13, will now be described in detail.

Figure 4 represents a scheme of a digital operation device according to this invention. First and second decimal point registers 31 and 61 are respectively composed of sixteen memory cells (flip-flops) corresponding to sixteen bits and connected in cascade. Since the structural elements of each cell cannot store information semi-permanently and their storage time is limited, they circulate and keep the information transferring successively to the next structural elements and may be described as dynamic registers. However, both decimal point registers operate so that only one of the memory cells is in an operational state (memory state) different from those of all of the other memory cells. Of course, the bit position of said memory cell in the different operational state is made to correspond to a numerical value to be stored. The clock pulses ϕ_1 , ϕ_2 and ϕ_3 can shift the content of said memory cell in the different operational state to another memory cell corresponding to another bit position. If a set of clock pulses ϕ_1 , ϕ_2 and ϕ_3 included in one bit time are introduced in a register, the bit position corresponding to said memory cell in the operational state different from the others becomes shifted to the next by one bit. Under the circumstances that the bit position of said memory cell of the different operational state is made to correspond to the numerical value to be stored, therefore, the above-mentioned introduction of the clock pulses results in a change of the numerical value stored in the register. Accordingly, it is also possible to impart an operational function without use of conventional adders if the number of clock pulses is appropriately made to correspond to the numerical value stored as an operand in the register. In practice, however, it is a

problem how the number of clock pulses is controlled to execute addition or subtraction of the numerical value as an operand with respect to the numerical value already stored in the register.

A clock pulse control device 15 controls the number of clock pulses ϕ_1 , ϕ_2 and ϕ_3 to be introduced in the registers 31 and 61 by interrupting the clock pulses for a specific time interval of which the length is determined in accordance with a sort of addition and subtraction and the value of an operand. Therefore, said clock pulse control device 15 is supplied with the original clock pulses from the clock pulse generator 13, an operation instruction such as an addition or subtraction command and a signal relating to the operand. A detector device 16 is provided for deriving a detector output which designates how the numerical value stored in the first decimal point register 31 is added to or subtracted from the numerical value stored in the second decimal point register 61. In practice, it detects in what kind of operational state the memory cell corresponding to the least significant bit position in the first decimal point register is.

A simple example of a calculation will now be given with reference to Figure 5. All of the memory cells in the register 31 respectively take either of only two states, that is, binary "0" to "1". For example, it is assumed that the above-mentioned operational state different from the others is binary "1", the bit position of the memory cell at the right-hand end of the register has the least significant bit x_1 and the position of the memory cell at the left-hand end of said register has the most significant bit x_{16} . Moreover, it is assumed that, if the set of clock pulses ϕ_1 , ϕ_2 and ϕ_3 are introduced in the register, the content of the memory cell storing binary "1" is shifted to a less significant bit position.

Referring to Figure 5-1, it is defined that: when only the memory cell corresponding to the least significant bit x_1 stores binary "1", the register 31 stores decimal "0"; when only the memory cell corresponding to the second bit x_2 stores binary "1", said register 31 stores decimal "1"; in a similar manner, the successive decimal numerals stored in the register is made to correspond to the successive bit positions storing binary "1"; and, at last, when only the memory cell corresponding to the most significant bit x_{16} stores binary "1", said register 31 stores decimal "15".

Now, referring to Figure 5-2, consideration is made about the case of addition $X + 1$, where X generally indicates a decimal numeral stored in the register 31 and, in the present case, decimal "2" is stored in said register and $X = 2$. According to the connection with the registers in the numerical processing section, practical design is so

arranged that only one set of clock pulses ϕ_1 , ϕ_2 and ϕ_3 are introduced in the register of the decimal point processing section during the duration of one digit timing pulse, that is, the clock pulses ϕ_1 , ϕ_2 and ϕ_3 are introduced in the register 31 during only the duration of the bit timing pulse t_4 . Therefore, the bit position in the operational state different from the others is shifted by one bit in response to the introduction of the set of clock pulses at each lapse of the digit timing pulse. Moreover, the operation is executed by controlling not all but one of the set of clock pulses ϕ_1 , ϕ_2 and ϕ_3 . Only a clock pulse controlled by the control device 15 is shown in the drawings. If a binary information "1" is intended to be merely circulated at a period of one word-length time, only one clock pulse is enough to be introduced during each digit time. However, in the case of such addition as $X + 1$, it is necessary to introduce fifteen clock pulses in the register 31 during one word-length time and to interrupt the introduction of clock pulse during only one digit time. Thus, the content of the memory cell having stored binary "1" is shifted to the fourth bit position and this results in storage of decimal "3" in the register 31 and in completion of addition of one.

Figure 5-3 is illustrative of the case of subtraction, $X - 1$, where $X = 2$. By introducing the clock pulses in the register 31 during only one digit time, the content of the memory cell having stored binary "1" is shifted to the bit position corresponding to the second bit x_2 and this results in completion of the subtraction.

Figure 5-4 is illustrative of the case of addition, $X + Y$, of information stored in both the registers 31 and 61, where X indicates a decimal numeral stored in the register 31 and Y indicates that stored in the register 61 and, in the present example, $X = 3$ and $Y = 4$. It is particularly necessary in this case to make a connection with the output of the detecting device 16. The detecting device 16 detects whether or not the memory cell corresponding to the least significant bit in the register 31 stores binary "1" and, if the detection is "YES", produces a detection output G continuously from the beginning of the associated digit time to the termination of the word-length time. In the above-mentioned case where the decimal "3" is stored in the register 31 and decimal "4" is stored in the register 61, an addition command is applied to the clock pulse control device 15. Binary "1" appears from the lowermost end of the register 31 only during the time interval wherein the digit timing pulse T_4 exists and is detected by the device 16. The result is that the detector output G is derived during the time interval from the digit timing pulse T_4 to the digit timing pulse T_{16} . If an addition command is

generated and the clock pulses are arranged to be introduced in the register 61 only during the duration of the detector output G, thirteen clock pulses in total are introduced in said register 61 during one word-length time. When such number of clock pulses are introduced, the content of the memory cell storing binary "1" is shifted toward the least significant bit position, returned to the most significant bit position and, in the result, reaches the eighth bit position corresponding to the bit x_8 . This means completion of the addition, $X + Y = 7$.

Figure 5-5 illustrates the case of subtraction, $Y - X$, where $Y = 4$ and $X = 3$. If a subtraction command is generated and the clock pulses are arranged to be introduced in the register 61 only during the time interval wherein the detector output G does not exist, three clock pulses in total are introduced in the register 61 during one word-length time and, in the result, the content of the memory cell storing binary "1" is shifted to the bit position corresponding to the second bit x_2 . That is to say, desired operational function can be obtained if the clock pulses are arranged to be introduced only during the time interval wherein the detector output G exists in the case of addition and the output G does not exist in the case of subtraction.

Figure 6 represents a logic constitution of the clock pulse control device 15. It is provided with an AND gate 17 to be driven into binary condition "1" in response to application of the addition command and the detector output G, an AND gate 18 to be operated in response to application of the subtraction command and the detector output G and an OR gate 19 having the outputs of said both AND gates as its inputs. The output of said OR gate is applied to an inverter 20 and the output of said inverter 20 and a signal $t_4\phi_1$ from the outside are applied to an OR gate 21. That is, what is controlled by the clock pulse control device 15 is only the clock pulse ϕ_1 generated during the duration of the bit timing pulse t_4 . The output of the OR gate 21 in the last stage is introduced in the clock pulse input of the second decimal point register 61. On the contrary, if the operational result is required to be introduced in the first decimal point register 31, the detector device 16 may be connected to the register 61 and the output of the OR gate 21 may be introduced in the register 31.

Referring to Figure 7-1 representing the logic constitution of the detector device 16, there are provided an OR gate 22 having the addition and subtraction commands as its input and an AND gate 23 having as its inputs both the output of said OR gate and a signal x_1 derived in response to a storage of binary "1" in the memory cell corresponding to the least significant bit position of the

register. The output of said AND gate 23 is supplied to the set input terminal of a flip-flop 24 of RS-type, whose reset input terminal is supplied with the digit timing signal T_{16} . When a flip-flop 25 of D-type as shown in Figure 7-2 is used, an operational function similar to the above can be obtained by adding an AND gate 26 having as its inputs its own output and the digit timing signal T_{16} , since it has no reset input terminal. That is, in response to incoming of the digit timing signal T_{16} , the feed-back loop including the AND gate 26 is cut off and a reset condition is obtained.

The writing operation of decimal point information in the decimal point register is carried out in the following manner. Just after starting the operation, the register is cleared and binary "1" is stored in the position corresponding to the least significant bit x_1 . Then, the decimal point key is depressed to prepare for the shift of said binary "1". If the numeral keys are pushed twice after the operation of the decimal point key, said binary "1" should be shifted to the position corresponding to the third bit x_3 . Therefore, the numerical value to be stored should be changed in accordance with the number of depressions of the numeral keys after the operation of the decimal point key. Thus, if the number of additions of $X + 1$ is previously caused to correspond to the number of depressions of the numeral keys following the decimal point key utilizing addition of $X + 1$ as shown in Figure 5-2, the decimal point information is written in the register. According to the above constitution, therefore, conventional adders are no longer required.

Next, the above-mentioned devices will be described in detail referring to an embodiment constituted using MOS type field effect transistors which are advantageous for the integration of circuits.

Referring to Figure 8 representing a practical circuit configuration of the decimal point register 31, MOS field effect transistors are used as the structural elements. Each MOS field effect transistor is used as a temporary storage circuit of low power consumption storing information in its gate internal capacitance as an electrostatic charge; in view of its inherent feature of very high internal capacitance between the gate and the substrate and very high input impedance between the gate and the source. The broken line blocks 27 in Figure 8 are memory cells (D-type flip-flops) corresponding to the respective bits and having the same circuit configuration. For example, the memory cell corresponding to the second bit x_2 will be described now. All of the MOS field effect transistors constituting the respective cells are P-channel type.

Two field effect transistors 41 and 42 have inherent stray capacitances between their gate electrodes and substrates and store electrostatic charges corresponding to information pulses so as temporarily to store the information. The gate electrodes thereof serve as respective information pulse input terminals, the source electrodes are connected to ground and the drain electrodes are connected through the under-mentioned load resistors to a potential (negative) source 30.

The drain electrode of the first-stage transistor 41 is connected in cascade through a transistor 44 to the gate electrode of the second-stage transistor 42 and a charge stored in the first-stage is transferred to the gate internal capacitance of the second-stage with inverted phase. The drain electrode of the second-stage transistor 42 is connected through a transistor 45 to the gate electrode of the first-stage transistor 41 to provide a feed-back path of the information. Thus, the information can be circulated and stored through both the transistors 41 and 42 and the transistors 44 and 45 constituting the transmission paths between said transistors.

The transistors 43, 44 and 45 respectively operate as switching elements in response to the clock pulses ϕ_1 , ϕ_2 and ϕ_3 having different phases. The clock pulses ϕ_1 , ϕ_2 and ϕ_3 are introduced in the respective gate electrodes and the source-drain paths are respectively inserted in control lines to be switched. Field effect transistors 46 and 47 connected respectively to the drain electrodes of the transistors 41 and 42 operate as load resistors of the storage elements. The transistor 43 serves as a switching element for controlling information transfer between the bits.

Now, an operation of the above-mentioned circuit will be described referring to Figure 9. Whether the memory cell is storing binary "1" or "0" is decided according to whether the second-stage storage transistor is conducting or cut off. Now, it is assumed that the memory cell corresponding to the third bit x_3 stores binary "0", that is, the second-stage storage transistor of the memory cell corresponding to the bit x_3 is in the cut-off state. In this case, therefore, an output signal of negative potential is derived from said memory cell.

If the clock pulse ϕ_1 of negative level is introduced in the gate electrode of the transistor 43, said transistor is turned on and the input signal is transferred to the point A as it is. Since the input signal has a negative level, a negative charge is stored in the gate internal capacitance of the storage transistor 41 and at the same time, said transistor 41 is driven into conduction. At this time, the drain electrode of the transistor 41 is at zero potential. The input information is conserved by the gate internal capacitance while discharging at a time constant determined by

the PN junction leakage resistance and the gate internal capacitance of the switching transistor 44 until the next clock pulse ϕ_2 is applied.

When the clock pulse ϕ_2 is introduced in the gate electrode of the switching transistor 44, said switching transistor 44 is turned on and a potential at the point B is transferred to the point C as it is. Since the point B was at zero potential, however, no charge is stored in the gate internal capacitance of the storage transistor 42. Therefore, said storage transistor 42 is in the cut-off state and the point D is maintained at a negative potential. Accordingly, the memory cell corresponding to the bit x_2 stores binary "0" in this state and the operational state of the first-stage memory cell has been transferred to the second-stage memory cell in response to introduction of the clock pulses ϕ_1 and ϕ_2 . In the case the first-stage memory cell corresponding to x_3 stores binary "1" contrary to the other memory cells, the memory cell corresponding to x_2 turns to the state of "1" similarly.

If the clock pulse ϕ_3 is applied thereafter, the feed-back path from the second-stage to the first-stage is closed for the first time and the potential at the point D is returned to the point A and kept temporarily in the gate internal capacitance of the first-stage. That is, a negative charge is again stored in the gate internal capacitance since the drain terminal of the second-stage was at a negative potential.

After that, if a new information pulse is applied at the time of introduction of the clock pulse ϕ_1 , a new memory content corresponding to the input information is conserved without connection to the memory content of the first-stage. In the case of absence of new input information, it is transferred again to the gate internal capacitance of the second-stage in response to introduction of the next clock pulse. By this repetition, the information of one bit is stored statically. In addition, the gate internal capacitance has its discharging paths, at the time of the interruption of the control pulse, through the gate and source electrodes to ground and through the switching transistor in open circuit to ground. However, these paths exhibit high impedance and block quick dissipation of the information.

The clock pulse ϕ_1 controlling information transfer between the bits is controlled by the clock pulse control device 15 only during the duration of the bit timing signal t_4 . The other clock pulses ϕ_2 and ϕ_3 are required to be always applied periodically in order to prevent dissipation of the information.

Figure 10 represents modified embodiments of the memory cell of the decimal point register 31. Referring to Figures 10-1 and 10-2, there provided are

three storage transistors 51, 52 and 53 and three switching transistors 54, 55 and 56 controlled by two clock pulses ϕ_1 and ϕ_2 . Two clock pulses are sufficient for this case in contrast with the above-mentioned embodiment, but operation of the circuit is quite similar. The transistors 57, 58 and 59 serve as load resistors for the transistors 51, 52 and 53, respectively. The modified embodiment shown in Figure 10-3 includes two storage transistors 71 and 72 and two switching transistors 73 and 74. Since this embodiment somewhat differs from the memory cells in the above-mentioned embodiments and has no feed-back path, it cannot execute an apparently static storage. Transistors 75 and 76 operate as load resistors.

Figure 11 represents a practical circuit configuration of the clock pulse control device 15 using MOS field effect transistors. An AND gate 17 surrounded by a broken line block is driven for the first time in response to the detector output G and an addition command. Transistors 81 and 82 operate as gate elements. The gate electrodes thereof are connected to input sources, the source electrodes are connected to ground and the drain electrodes are connected in common through the undermentioned load resistance to a potential (negative) source 30. A transistor 83 operates as an output element. Though the gate circuit thereof itself is well known in the art, some explanation will be given below.

If both the detector output G and the addition command are at zero potential, both transistors 81 and 82 do not conduct and the gate electrode of the output transistor 83 is maintained at a negative potential. Therefore, said transistor 83 conducts and the potential of its drain electrode is raised to nearly zero potential. Thus, the gate output corresponding to binary "1" is derived. Transistors 84 and 85 operate as load resistors. On the other hand, an AND gate 18 operates in response to the detector output G and a subtraction command and transistors 91, 92, 93 and 94 which are the structural elements thereof operate in correspondence with the above-mentioned AND gate 17. The drain electrodes of the output transistors 83 and 93 are connected in common to the gate electrode of a transistor 101 in an inverter 20 in the next stage. By use of such connection, the OR gate 19 in the logic constitution of Figure 6 can be omitted. This is a so-called wired OR gate. A section surrounded by a broken line block in the last stage is an OR gate 21. Transistors 111 and 112 and a transistor 113 respectively operate as gate elements and an output element. It is noted that the clock pulses ϕ_1 , ϕ_2 and ϕ_3 are negative pulses when the OR gate 21 is operated.

When the drain electrode of the inverter transistor 101 is at a negative potential, that is, when the conditions of the detector output G and the addition command or the conditions of the detector output G and the subtraction command are fulfilled, the gate electrode of the transistor 111 directly coupled thereto has a negative potential and the transistor 111 is driven into conduction. On the other hand, since the transistor 112 is also driven into conduction when the clock pulse ϕ_1 is generated, the gate electrode of the output transistor 113 is led to zero potential. Accordingly, the transistor 113 is cut off and the drain electrode thereof drops down to the negative potential. This results in the clock pulse ϕ_1 appearing as it is from the drain electrode without interruption. Since the system is being described as a positive logic system throughout this Specification with the zero potential corresponding to binary "1" and the negative potential to binary "0", this state corresponds to two inputs of "0" and an output of "0".

If the condition is not fulfilled and the drain electrode of the inverter transistor 101 becomes zero potential, however, the transistor 111 is cut off and the output transistor 113 inverts into conduction. Therefore, the drain electrode of the transistor 113 is raised to zero potential and the clock pulse ϕ_1 is not received from the drain electrode in spite of the fact that it is generated. This state corresponds to a state wherein one input is "1", the other inputs are "0" and the output is "1", and clearly indicates a function of OR gate. Transistors 102, 114 and 115 serve as load resistors.

Figure 12 represents a practical circuit configuration of the detector device 16 similarly using MOS field effect transistors. An OR gate 22 surrounded by a broken line block includes a gate transistor 121 having the addition command as an input, a gate transistor 122 having the subtraction command as an input, an output transistor 123 and two transistors 124 and 125 for load resistors, and its operation is of the same type as the above-mentioned OR gate 21. An AND gate 33 following the OR gate 22 includes a gate transistor 131 having the output of the first stage OR gate 22 as an input, a gate transistor 132 having the least significant bit x_1 of the decimal point register as an input, an output transistor 133 and two transistors 134 and 135 for load resistors. The output of said AND gate is introduced in a D-type flip-flop 36 for detection. This flip-flop 36 has a circuit configuration substantially the same as that of the memory cell of the register and includes two storage transistors 141 and 142, three switching transistors 143, 144 and 145 and two load resistor transistors 146 and 147. An AND gate 37 includes a gate transistor 151 having

the digit timing signal T_{16} as an input, a gate transistor 152 having the output of the flip-flop 36 as an input, an output transistor 153 and two load resistor transistors 154 and 155. These gate circuits are well known and the operation of the whole detector device should be easily understood from the above description.

Interruption of the clock pulse determining the propagation speed of information in the registers for a specific time interval necessitates variation of the frequency or period of the clock pulse.

Although registers of the circulation type (so-called dynamic register) using supersonic delay lines have been known in the art, said delay lines have their own inherent propagation speeds and the propagation speed of information has been considered to be impossible to change in response to external signals. In a register having MOS field effect transistors as the structural elements, however, since the MOS field effect transistors preferably exhibit very high impedance, its possible storage time extends to several seconds and the frequency of the clock pulse can be arbitrarily changed from one kilocycle to several megacycles. The above-described computer device has been completed upon the principle of changing the frequency of the clock pulse which decides the propagation speed of information.

Figure 13 represents a block diagram of a display device in which a decimal point indicating section is also included. While the display tubes to be used may be either of the glow discharge type or of the fluorescent type, the apparatus will be described in connection with the latter. A display tube of the fluorescent type is a directly heated cathode ray tube and becomes luminescent when thermions collide with a plurality of phosphors arranged in a plane. A thermion emitting filament, phosphor anode electrodes shaped to character patterns to be displayed, and an accelerating and diverging grid electrode arranged therebetween are sealed in a tube envelope. If a suitable voltage is applied to heat the cathode filament in such a display tube, thermions are emitted toward the phosphors. The thermions are accelerated and caused to diverge by the grid electrode and then uniformly collide against only the phosphors on the anode electrodes to which an operation voltage is applied to excite said phosphors. Luminescence control is controlled by making the potential of the grid electrode nearly equal to the potential of the cathode (filament potential) to cut off display tube. The device in the drawing is based upon a dynamic indication system utilizing such luminescence control by means of the grid electrode.

For indication of the numeral portion, the digit timing signals $T_2, T_3, \dots, T_{16}$ and T_1

are supplied to the grid electrodes of the respective display tubes 63 from a digit time counter 65 and information signals obtained by decoding the information in a first dynamic register 3 of the numerical processing section in synchronism with the digit timing signals, are supplied to the anode electrodes from a decoder circuit 64, so that both the signals co-operate in the respective tubes to indicate numerical character patterns.

The information (binary coded decimal number of 16 digits) in the first dynamic register 3 is circulated as being shifted in time through an arithmetic unit 9. However, the arithmetic unit 9 does not perform an arithmetic function during the display cycle since no other input is applied thereto.

Said information in the register is supplied through a buffer register 10 for indication to the decoder circuit 64. The respective digit positions of the information in the first dynamic register 3 appearing at the arithmetic unit 9 are such that the digit timing signal T_2 corresponds to the first position (least significant bit position), the digit timing signal T_3 corresponds to the second position, and the digit timing signal T_1 corresponds to the sixteenth position (most significant bit position). The binary information in the register is converted in the decoder circuit 64 into decimal outputs (allocated respectively to the decimal digits 1 to 9) to select the anode segments constituting the respective numeral patterns to be indicated. A bit time counter 66 generates the bit timing pulses t_1, t_2, t_3 and t_4 .

Since a decimal point register 67 stores binary "1" in only one memory cell thereof and its bit position always corresponds to the numerical value stored in the register, the time at which the register output "1" appears coincides with said numerical value stored in the register. That is, when the register output appears during the digit timing signal T_1 , the decimal point register 67 stores a numerical value "0", and, when the register output appears during the digit timing signal T_3 , it stores a numerical value "2". Accordingly, if the decimal point segments of the respective display tubes are connected in common, the position of the decimal point can be simply indicated without use of the decoder circuit 64, and the driving circuit for decimal point indication can be remarkably simplified. A buffer register 11 is provided for delay by one digit time.

WHAT WE CLAIM IS:—

1. A semiconductor decimal point indicating device including at least two registers with one register storing numerical information consisting of a word or words each containing a predetermined number of digits and the other register

the digit timing signal T_{16} as an input, a gate transistor 152 having the output of the flip-flop 36 as an input, an output transistor 153 and two load resistor transistors 154 and 155. These gate circuits are well known and the operation of the whole detector device should be easily understood from the above description.

Interruption of the clock pulse determining the propagation speed of information in the registers for a specific time interval necessitates variation of the frequency or period of the clock pulse.

Although registers of the circulation type (so-called dynamic register) using supersonic delay lines have been known in the art, said delay lines have their own inherent propagation speeds and the propagation speed of information has been considered to be impossible to change in response to external signals. In a register having MOS field effect transistors as the structural elements, however, since the MOS field effect transistors preferably exhibit very high impedance, its possible storage time extends to several seconds and the frequency of the clock pulse can be arbitrarily changed from one kilocycle to several megacycles. The above-described computer device has been completed upon the principle of changing the frequency of the clock pulse which decides the propagation speed of information.

Figure 13 represents a block diagram of a display device in which a decimal point indicating section is also included. While the display tubes to be used may be either of the glow discharge type or of the fluorescent type, the apparatus will be described in connection with the latter. A display tube of the fluorescent type is a directly heated cathode ray tube and becomes luminescent when thermions collide with a plurality of phosphors arranged in a plane. A thermion emitting filament, phosphor anode electrodes shaped to character patterns to be displayed, and an accelerating and diverging grid electrode arranged therebetween are sealed in a tube envelope. If a suitable voltage is applied to heat the cathode filament in such a display tube, thermions are emitted toward the phosphors. The thermions are accelerated and caused to diverge by the grid electrode and then uniformly collide against only the phosphors on the anode electrodes to which an operation voltage is applied to excite said phosphors. Luminescence control is controlled by making the potential of the grid electrode nearly equal to the potential of the cathode (filament potential) to cut off display tube. The device in the drawing is based upon a dynamic indication system utilizing such luminescence control by means of the grid electrode.

For indication of the numeral portion, the digit timing signals $T_2, T_3, \dots, T_{16}$ and T_1

are supplied to the grid electrodes of the respective display tubes 63 from a digit time counter 65 and information signals obtained by decoding the information in a first dynamic register 3 of the numerical processing section in synchronism with the digit timing signals, are supplied to the anode electrodes from a decoder circuit 64, so that both the signals co-operate in the respective tubes to indicate numerical character patterns.

The information (binary coded decimal number of 16 digits) in the first dynamic register 3 is circulated as being shifted in time through an arithmetic unit 9. However, the arithmetic unit 9 does not perform an arithmetic function during the display cycle since no other input is applied thereto.

Said information in the register is supplied through a buffer register 10 for indication to the decoder circuit 64. The respective digit positions of the information in the first dynamic register 3 appearing at the arithmetic unit 9 are such that the digit timing signal T_2 corresponds to the first position (least significant bit position), the digit timing signal T_3 corresponds to the second position, and the digit timing signal T_1 corresponds to the sixteenth position (most significant bit position). The binary information in the register is converted in the decoder circuit 64 into decimal outputs (allocated respectively to the decimal digits 1 to 9) to select the anode segments constituting the respective numeral patterns to be indicated. A bit time counter 66 generates the bit timing pulses t_1, t_2, t_3 and t_4 .

Since a decimal point register 67 stores binary "1" in only one memory cell thereof and its bit position always corresponds to the numerical value stored in the register, the time at which the register output "1" appears coincides with said numerical value stored in the register. That is, when the register output appears during the digit timing signal T_1 , the decimal point register 67 stores a numerical value "0", and, when the register output appears during the digit timing signal T_3 , it stores a numerical value "2". Accordingly, if the decimal point segments of the respective display tubes are connected in common, the position of the decimal point can be simply indicated without use of the decoder circuit 64, and the driving circuit for decimal point indication can be remarkably simplified. A buffer register 11 is provided for delay by one digit time.

WHAT WE CLAIM IS:—

1. A semiconductor decimal point indicating device including at least two registers with one register storing numerical information consisting of a word or words each containing a predetermined number of digits and the other register



5 storing information relating to the position of the decimal point in the numerical information stored in said one register, said other register including a plurality of pairs of transistors each pair connected one to the other for storing one bit of said decimal point information, a generator for generating at least one set of timing signals corresponding in number to the number of digits and determining the boundaries of each word time, decimal point processing means including logical gating circuits connected to said generator, and connections between said decimal point processing means and said other register, said decimal point processing means modifying the information stored in the decimal point register in accordance with new decimal point information at the termination of each set of timing signals, the modified decimal point information being read out during a period of one timing signal within each word time, and the position of one timing signal in the set of timing signals determining the decimal point position of

the resulting information, and time sharing indicating means connected with said generator, the last said means including decimal point indicating elements connected in parallel to said decimal point processing means and actuated by the decimal point information at a period of one timing signal during each word time.

2. A device, according to claim 1, in which said transistors are MOS field effect transistors connected in cascade and said one bit of decimal point information is capacitively stored in the capacitor formed between each gate electrode and the substrate of each transistor.

3. A semiconductor storage device substantially as described with reference to the accompanying drawings.

A. M. & Wm. CLARK,
5 Stone Buildings,
Lincoln's Inn,
London, WC2A 3XT.

(8728) Printed by Her Majesty's Stationery Office Press, Edinburgh, 1971.
Published by The Patent Office, 25 Southampton Buildings, London, WC2A 1AY,
from which copies may be obtained.

