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METHOD FOR FORMING DUAL-LAYER LOW DIELECTRIC BARRIER FOR INTERCONNECTS AND DEVICE FORMED

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Field of the Invention

The present invention generally relates to a method for forming a low dielectric barrier for interconnects and device formed and more particularly, relates to a method for forming a dual-layer low dielectric barrier on copper interconnects in a semiconductor structure for diffusion barrier and adhesion improvement with subsequently deposited layers and device formed by such method.

Background of the Invention

The technology of making interconnections for providing vias, lines and other recesses in semiconductor chip structures, flat panel displays, and package applications has been developed for many years. For instance, in developing interconnection technology for very-large-scale-integrated (VLSI) structures, aluminum has been utilized as the primary metal source for contacts and interconnects in semiconductor regions or devices located on a single substrate. Aluminum has been the material of choice because of its low cost, good ohmic contact and high conductivity. However, pure aluminum thin-film conductors have

undesirable properties such as a low melting point which limits its use to low temperature processing, possible Si diffusion into Al during annealing which leads to contact and junction failure, and poor electromigration resistance. The electromigration phenomenon occurs when the superposition of an electric field onto random thermal diffusion in a metallic solid causes a net drift of ions. Consequently, a number of aluminum alloys have been developed which provide advantages over pure aluminum. For instance, U.S. Patent No. 4,566,177 discloses a conductive layer of an alloy of aluminum containing up to 3% by weight of silicon, copper, nickel, chromium and manganese to improve electromigration resistance. U.S. Patent No. 3,631,304 discloses aluminum alloys with aluminum oxide which were also used to improve electromigration resistance.

More recently VLSI and ULSI technology has placed more stringent demands on the wiring requirements due to the extremely high circuit densities and faster operating speeds required of such devices. This leads to higher current densities in increasingly smaller conductor lines. As a result, conductive wiring is desired which requires either larger cross-section wires for aluminum alloy

conductors or a different wire material that has a higher conductivity. The obvious choice in the industry is to develop the latter using copper based on its desirable high conductivity.

In the formation of VLSI and ULSI interconnection structures such as vias and lines, copper is deposited into a line, via or other recesses to interconnect semiconductor regions or devices located on the same substrate. Copper is known to have problems at semiconductor device junctions due to its fast reaction rate with Si. Any diffusion of copper atoms or ions into the silicon substrate can cause device failure. In addition, copper diffusion into the intermetal dielectric can also cause device failure by generating shorts and opens. It is therefore vital to the reliability of a copper interconnect that the interconnect be coated with layers which act to prevent the interdiffusion of copper with the surrounding materials. These layers, commonly called "liners", "barriers" and "caps", must also exhibit good adherence between the copper interconnect and the various dielectric layers and contact vias.

In the metallization process of chip network interconnection for copper back-end-of-line (BEOL), vias and trenches are metallized utilizing standard sequential procedures of a thick dielectric deposition, via and trench openings,

deposition of thin liners on via and trench walls, filling via and trenches with copper, planarization of the top copper surface and finally, capping the top surface with a protective layer for preventing copper migration into the next upper level dielectric and for minimizing interactions with copper while the upper level dielectric is being deposited. The final capping layer further serves as a reactive ion etching stop layer for the next upper layer dielectric. The metallization process is repeated for each level of interconnect wiring.

In the conventional process, the most common dielectric material used to cap each copper BEOL level is silicon nitride (SiN). It has been reliably manufactured in ULSI where Cu is the intermetal dielectric and silicon dioxide (SiO_2) is the interconnect dielectric. However, for continued performance improvements of interconnects the ULSI industry is driving towards low dielectric constant (low k) intermetal dielectrics. SiN has a relatively high dielectric constant of 7 to 8 and significantly increases the effective intralevel capacitance. The application of SiN in future BEOL interconnects will be minimized or replaced to meet low k requirements.

Solutions have been proposed by others to solve the copper low k BEOL difficulties. For instance, one solution is to

use a self-aligning metal cap layer to cover and protect the top surface of copper lines, to provide good adhesion and further, to act as a barrier for copper diffusion. However, in order to meet the desired copper barrier properties, the thickness of the metal cap layer must be at least 1,000 ~ 2,000 Å which may cause a short between conductor lines when the spacing between the lines is smaller than 3,000 Å. The use of a metal only cap also presents difficulties in processing the next level dielectric. During reactive ion etching (RIE) of the top level dielectric there is no etch stop and the lower metal and dielectric would be prone to etching and contamination from this RIE process.

Still others have proposed a solution by using a thin, low k dielectric film formed of materials such as those containing Si, C, H or Si, C, O, H in a thickness up to 800 Å. However, these low k films (with dielectric constants of less than 4) typically do not function as good copper diffusion barriers. They are also not good barriers to copper oxidation during the manufacture of the BEOL interconnect and can cause catastrophic failure as CuO formation greatly weakens adhesion and forms voids. In comparison

SiN is generally deposited by plasma enhanced chemical vapor deposition (PECVD) of SiH_4 and NH_3 which in itself does not cause oxidation of copper and SiN is known to be a good oxygen barrier.

It is therefore an object of the present invention to provide a method for forming a barrier layer on a copper conductor that does not have the drawbacks or shortcomings of the conventional copper barrier layers.

It is another object of the present invention to provide a method of reducing the SiN cap thickness and improving its adhesion to copper.

It is another object of the present invention to provide a method for forming a low dielectric barrier layer on a copper conductor that improves both the diffusion barrier and adhesion properties.

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It is a further object of the present invention to provide a method for forming a dual-layer low dielectric barrier on a copper conductor in which a metal alloy film containing phosphorus or boron and a low dielectric material containing silicon are sequentially deposited on top of a copper conductor.

It is another further object of the present invention to provide a method for forming a dual-layer low dielectric barrier on a copper conductor by depositing two separate layers for adhesion and diffusion barrier followed by an annealing process.

It is still another object of the present invention to provide a method for forming a dual-layer low dielectric barrier on a copper conductor used as a via or interconnect in a copper back- end-of-line process.

It is yet another object of the present invention to provide a method for forming a dual-layer low dielectric barrier on a copper conductor in which a deposition process of a phosphorus or boron-containing metal alloy film is followed by an annealing process to cause the metal alloy to diffuse into at least 2~4 atomic layers in the copper conductor.

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It is still another further object of the present invention to provide an electrical conductor in a semiconductor structure that includes a metal conductor, a film of a phosphorus or boron-containing metal alloy, and a film of a low k dielectric material on top.

It is yet another further object of the present invention to provide an electrical conductor in a semiconductor structure wherein a layer of phosphorus or boron-containing metal alloy film of between 50 Å and 200 Å thick is first deposited on the metal conductor, and a low k dielectric material of between 100 Å and 500 Å thick is then deposited on top of the metal alloy film.

Summary of the Invention

In accordance with the present invention, a method for forming a dual-layer low dielectric barrier on a copper conductor and structures formed are disclosed.

In a preferred embodiment, a method for forming a dual-layer low dielectric barrier on a copper conductor can be carried out by the operating steps of providing a pre-processed substrate which has a copper conductor formed in an insulator layer;

depositing a phosphorus or boron-containing metal alloy film on top of the copper conductor; heating the pre-processed substrate in a first heating process to a temperature of at least 300°C in a reducing gas atmosphere for a length of time sufficient for the phosphorus or boron-containing metal alloy to diffuse into at least 2~4 atomic layers in the top surface of the copper conductor; depositing a low k dielectric film on top of the phosphorus or boron- containing metal alloy film; and heating the pre-processed substrate in a second heating process in a reducing atmosphere to a temperature of at least 300°C for at least 1 hour. When specifying a reducing gas atmosphere, it is meant to include vacuum, H_2, forming gas and inert gas atmospheres.

Alternatively, the two layers (metal and dielectric) can be deposited in sequence, followed by a single annealing step process at a temperature of 400°C in a reducing atmosphere for 2 hours.

In the method for forming a dual-layer low dielectric barrier on a copper conductor, the first heating process may be conducted at a temperature of at least 325°C for at least 1 hour. The second heating process may be conducted at a temperature of at least 350°C for at least 2 hours. The reducing atmosphere

used in the first and second heating process may be a forming gas of hydrogen (N_2 + H_2) nitrogen or vacuum. The deposition process for the phosphorus or boron-containing metal alloy film may be conducted by an electroless plating technique. Alternatively, it is also possible to combine the two annealing procedures into a single one by subsequent deposition of the first metal layer containing the phosphorous or boron alloy film, followed by the deposition of the dielectric film and conducting a final heating of the double layer at 400°C for 2 hours in nitrogen or a reducing atmosphere comprising forming gas, H_2, nitrogen or vacuum. The dielectric film may be deposited on the phosphorus or boron- containing metal alloy film by a plasma enhanced chemical vapor deposition technique. The method may further include the step of depositing a nucleation layer of palladium on the pre-processed substrate prior to the step of depositing the phosphorus or boron- containing metal alloy film. The phosphorus or boron-containing metal alloy film may be Me-X-P or Me-X-B, wherein Me is a primary component of the alloy film and X is an alloy modifier.

The method for forming a dual-layer low dielectric barrier on a copper conductor may further include the step of depositing a palladium nucleation layer on the copper conductor by a selective ion exchange method utilizing a diluted palladium

sulfate solution in sulfuric acid. The phosphorus or boron-containing metal alloy film may further include between about 86 wt % and about 90 wt % Me, between about 2 wt % and about 4 wt% X and between about 6 wt % and about 12 wt% P or B. The dielectric film deposited may have a dielectric constant of not more than 5. The method may further include the step of depositing the phosphorus or boron-containing metal alloy film to a thickness between about 50 Å and about 300 Å, and preferably between about 100 Å and about 200 Å. The method may further include the step of depositing the phosphorus or boron-containing metal alloy film by an electroless deposition process in a hypophosphite solution containing cobalt sulfate, ammonium tungstate, sodium citrate and boric acid at a temperature between about 70°C and about 80°C, at a pH between about 8 and about 9. The method may further include the step of conducting the first heating process at a temperature between about 325°C and about 400°C for a time period between about 0.5 hours and about 2 hours. The method may further include the step of depositing the dielectric film of a material selected from the group consisting of a material containing Si, C, O, N, and/or H, a material containing Si, C, H, N and diamond-like carbon. The method may further include the step of depositing the dielectric film to a thickness between about 100 Å and about 500 Å, and preferably between about 250 Å and about 350 Å. The method may further include the step of conducting

the second heating process at a temperature between about 350°C and about 400°C for a time period between about 1 hour and about 5 hours. The phosphorus or boron-containing metal alloy film may be Me-X-P or Me-X-B, wherein Me is Co or Ni, X is W or Sn.

The present invention is further directed to an electric conductor in a semiconductor structure that includes a copper conductor situated in an insulating layer, a film of a phosphorus or boron-containing metal alloy being diffused into at least three atomic layers in a top surface of the metal conductor, and a film of a low k dielectric material on top of the phosphorus or boron-containing metal alloy film.

In the electrical conductor in a semiconductor structure, the phosphorus or boron-containing metal alloy is present into at least 2~4 atomic layers of the top surface of the metal conductor. The metal conductor may include copper. The phosphorus or boron- containing metal alloy may be a binary or ternary alloy of Me-P, Me-B, Me-X-P or Me-X-B with Me being Co or Ni and X being Si, W or Sn. The phosphorus or boron-containing metal alloy may be deposited to a thickness between about 10 Å and about 1,000 Å, and preferably between about 50 Å and about 200 Å. The phosphorus or boron-containing metal alloy may be deposited by an electroless plating technique. The dielectric

material deposited may be selected from the group consisting of a material containing Si, C, O, N and H. The dielectric material may be deposited to a thickness between about 10 Å and about 5,000 Å, and preferably between about 100 Å and about 500 Å. The semiconductor structure may be formed on a substrate selected from the group consisting of silicon, silicon germanium, silicon-on-insulator and gallium arsenide.

Brief Description of the Drawings

These and other objects, features and advantages of the present invention will become apparent upon consideration of the specifications and the appended drawing, in which:

Figure 1 is an enlarged, cross-sectional view of a present invention dual-layer low dielectric barrier formed on a copper conductor in a dual damascene structure with a second dual damascene structure formed on top.

Figure 2 is an enlarged, cross-sectional view of another embodiment of the present invention illustrating a dual-layer diffusion barrier/adhesion enhancer formed on a copper conductor. Figure 3 is a graph illustrating the dependency of the secondary ion counts of elements in a

multi-layer barrier test structure as a function of depth into the structure of the present invention. In this example, the Co-W-P film is 300 Å thick and a low k dielectric film of SiCOH is on top.

Figure 4 is a graph illustrating the dependency of the secondary ion counts for various elements in a multi-layer barrier structure as a function of depth into the structure of the present invention. In this example, the CoSnP film is 300 Å thick and a low k dielectric SiCOH film on top is 500 Å thick, wherein the metal alloy film has been annealed at 350°C for 2 hours.

Figure 5 is a table of data illustrating the dependency of adhesion test results on the structure and treatment of the silicon nitride film on copper with a metal alloy film therein between.

Figure 6 is a table of data illustrating the dependency of adhesion test results on the structure and annealing of the dual-layer barrier filing of SiCOH/liner metal.

Detailed Description of the Preferred Embodiment

The present invention discloses a method for forming a dual-layer low dielectric barrier for interconnects by first providing a pre-processed substrate that has a copper conductor formed in an insulating layer, then depositing a phosphorus or boron-containing metal alloy film on top of the copper conductor, heating the pre-processed substrate to a temperature of at least 300°C in a reducing atmosphere for a length of time that is sufficient for the metal alloy to diffuse into a surface layer in the copper conductor, then depositing a dielectric film on top of the metal alloy film, and heating the pre-processed substrate in a reducing atmosphere to a temperature of at least 300°C for a time period of at least 1 hour.

The present invention further discloses an electrical conductor in a semiconductor structure that includes a metal conductor situated in an insulating layer, a film of a phosphorus or boron-containing metal alloy on top of the metal conductor, and a film of a dielectric material on top of the phosphorus or boron- containing metal alloy film.

In the method or device provided by the present invention, the phosphorus or boron-containing metal alloy film may be represented by Me-X-P or Me-X-B, wherein Me is a primary component of the alloy film, while X is an alloy modifier. Me may be Co or Ni, and X may be W or Sn. P and B represent phosphorus and boron. The phosphorus or boron-containing metal alloy may further include between about 86 wt% and about 90 wt% Me, between about 2 wt% and about 4 wt% X and between about 6 wt% and about 12 wt% P or B. The metal alloy film is deposited to a thickness between about 50 Å and about 300 Å.

The heating process or the annealing process utilized in the present invention novel method is important to the properties of the final dual-layer dielectric barrier formed. For instance, in the first annealing process, the semiconductor substrate is heated to a temperature of at least 300°C or preferably to a temperature between about 350°C and about 400°C for a length of time that is sufficient for the phosphorus or boron-containing metal alloy to diffuse into at least the surface layer, i.e. at least 2~4 atomic layers in the copper conductor. The sufficient length of time may be between about 0.5 hour and about 2 hours. The second annealing process, conducted after the deposition of the low dielectric barrier layer, can be carried

out at a temperature of at least 300°C, or preferably between about 350°C and about 400°C for a time period between about 1 hour and about 5 hours. Alternatively, the two annealing steps can be combined into a single one by heating the dual layer for 2 hours at 400°C in a reducing atmosphere.

The dielectric layer may be deposited of a material such as that containing Si, C, O, N and/or H. The thickness of the dielectric film deposited is between about 100 Å and about 500 Å, or preferably between about 100 Å and about 350 Å.

The present invention novel method combines an electroless plated metal film with a film of low k (dielectric constant) dielectric cap layer deposited in sequence to a polished (such as by chemical mechanical polishing) copper/dielectric top surface to produce a dual-layer barrier. The dual-layer barrier presents the desirable properties of a copper diffusion barrier, good adhesion to copper, low dielectric constant, while maintaining the reactive ion etching (RIE) stop performance for the next upper level dielectric. Additional benefits of the present invention dual-layer barrier is the minimization of the dielectric cap layer thickness which generally decreases the effective dielectric constant of the

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interconnect structure and provides conductor redundancy which has been shown to minimize electromigration.

The structure of the present invention dual-layer barrier can be formed by the following process. Starting with a planarized structure consisting of a copper wiring embedded in a dielectric with a copper surface exposed in the dielectric layer. In the first step, a self-aligned selective application of a metal cap layer which has strong adhesion to the copper surface is performed to form a metal-to-metal bond. The metal cap layer has a thickness between about 100 Å and about 400 Å, thus providing greater electrical reliability and improved electromigration resistance. The metal cap layer further provides the copper surface with greater stability in its capability of closing voids and hillocks. After a first annealing, or heating process is conducted, which shall be described in more detail in a later section, a second deposition process for a blanket dielectric cap layer is performed. The blanket dielectric cap layer is most preferably prepared from very low dielectric constant materials, such as a material that contains Si, C, O, N and/or H or a material that contains Si, C, H,

N and diamond-like carbon. Alternatively, SiN may also be used, however, at a much reduced thickness than what is normally required as a single layer barrier.

Results obtained from a dual-layer cap prepared from selective cobalt-based electroless process, specifically but not limited to Co-W-P, combined with SiN, SiCH or SiCOH film have shown very good adhesion and achieved stability of Cu and control of Cu diffusion.

The chemical steps for forming the present invention dual-layer cap for diffusion barrier and adhesion can be described in more detail as follows: the overall objective of the present invention novel method is to create a dual-layer metal/dielectric film on the copper surface after a CMP process. In the first step of deposition on the copper surface, a metallic film is deposited by selective deposition achieved by an electroless plating of a layer between about 100 Å and about 400 Å thick. The layer is formed by an alloy that has the general structure of Me-X-P, wherein Me represents the primary component of the alloy, X is an alloy modifier which imparts to the film very specific properties of increased adhesion to copper and diffusion barrier properties, and P represents a certain amount of phosphorus coprecipitated during the process of film

formation. In a preferred embodiment of the present invention, X is selected to be 3 to 5 atomic % of W, while P is of the order of 7 to 9 atomic % in the alloy film.

In the second step of the present invention process, the copper structure is annealed with the top alloy film in a reducing atmosphere, for instance, forming gas or hydrogen at 350°C for at least 2 hours. The temperature treatment allows the components of the alloy to blend intimately and diffuse in a few atomic layers, into the top copper surface to provide chemical and metallurgical bonding and to form excellent adhesion with copper. Alternatively, the annealing step can be performed during or after the dielectric deposition.

In the third step of the present invention process, a dielectric film is applied on top of the metal film to form the dual-layer structure. This is typically accomplished by a plasma enhanced chemical vapor deposition (PECVD) process. In the process, the dielectric material is deposited over the Me-X-P layer that was previously deposited on the copper and is generally of a thickness between about 100 Å and about 500 Å. It has been found that the preferred dielectric films are those based on silicon compounds such as SiCOH, SiCH or SiN. A low dielectric constant material such as a diamond-like carbon (DLC)

may also be used. The preferred dielectric material is SiCOH as it exhibits the lowest dielectric constant.

In the fourth step of the present invention process, an annealing treatment is applied to the double layer in a reducing atmosphere of either hydrogen, nitrogen or forming gas at a temperature of at least 300°C for at least 2 hours. This final annealing process removes from the metallic cap/dielectric interface organic impurities and possibly other volatile products that detract from achieving good adhesion properties.

The final structure formed by the various chemical steps of the present invention process is shown in Figure 1. Figure 1 illustrates an enlarged, cross-sectional view of a dual damascene interconnect structure 10 with the incorporation of the first preferred embodiment of the present invention. The structure 10 is shown with two dielectric interconnect levels 20 and 30 which contain both vias 22,32 and trenches 24,34. The structure is built on a semiconducting substrate 12 which has an active device 14 formed in a top surface 16. Onto the substrate 12, a first dielectric layer 18 is deposited and patterned with an opening for via 32 and an opening for trench 34. The via and trench openings are then lined with a liner, i.e. a barrier layer 36, filled with metal 38, and planarized by a chemical mechanical

polishing method achieving a planarized top surface 40 on the trench 34.

In the next step of the process, which incorporates the present invention novel method, is the application of an electrolessly deposited cap layer 44 of Co-W-P that selectively deposits on top of the metal trench 34 only. The cap layer 44 prevents out-diffusion of metal 38 into the dielectric layer 50 as well as preventing contamination of trench metal 34 due to continued processing. The metal layer 44 is used with an optional dielectric cap layer 52 as the primary means of isolating the trench metal from any interaction during subsequent processing or during operation of the semiconductor device. The optional cap layer 52 can be used to further improve the barrier properties of the metal alloy layer 40 of Co-W-P or as an integration enhancement layer such as a reactive ion etch (RIE) stopping layer. The second dielectric layer 50, as shown in Figure 1, is used after the RIE process to form the dual damascene cavity for via 22 and trench 24. In this case, the dielectric cap layer 52 is used as a RIE stop. When it is used, the RIE stop layer 52 is etched to open to the

second level trench 24 in the process starting with the liner layer 36 is repeated until the necessary number of interconnect levels are obtained.

Figure 2 is an enlarged, cross-sectional view of a copper test vehicle used for adhesion testing and diffusion barrier performance with the present invention dual-layer barrier formed on top. It is seen that on top of the silicon substrate 12 is first deposited a barrier layer 36 which includes a metal liner layer about 800 Å thick. A copper conductor 38 of 2,000 Å thick is then sputter deposited on top of the liner 36. The electroless metal cap layer 44 deposited can be either a Co-W-P or Co-Sn-P layer having a thickness between 300 Å and 500 Å. A low k dielectric layer 52 of SiCOH having a thickness of 500 Å is then deposited on top. To enhance SIMS signal, a layer of diamond-like carbon 54 was be deposited on top of the SiCOH layer 52.

Figures 3 and 4 illustrate SIMS/plot obtained on the structure shown in Figure 2. As seen in Figures 3 and 4, when only a 300 Å thick electrolessly deposited metal layer of Co-W-P or Co- Sn-P, and a 500 Å layer of SiCOH are deposited, after annealing which would promote diffusion of copper to cross into the surface layers of the metal layer into the SiCOH, the

copper remains completely behind and under the electrolessly deposited metal alloy layer 44 and does not penetrate across the layer 44 into the dielectric layer 52. These results indicate that the present invention structure stops the copper migration and the effect of copper potential oxidation by oxygen molecules that may come across the SiCOH layer 52, at least under the effect of thermal energy. Therefore, the structure shown is an effective system as a stopper for thermal migration of copper and oxygen atoms.

Figure 5 is a table illustrating data obtained on the adhesion strength between a copper conductor and a SiN dielectric layer utilizing various metal alloy films therein between. It is shown that the adhesion of copper to silicon nitride depends strongly on the pre-treatment of the copper surface prior to the nitride application. Optimum results are obtained by using Co-W-P inner-layer, Co-Sn-P inner-layer, and high-density plasma (HDP) deposited nitride. The adhesion strength indicated in the table of Figure 5 is shown in units of MPa x $m^{1/2}$.

Test results of the adhesion of the dual-layer cap with electrolessly deposited cap layer on copper with a dielectric layer of SiCOH are shown in Figure 6. Six samples were run with the structure of Si-SiO_2/liner metal/Cu (2,000 Å). The samples

were electrolessly plated with either Co-W-P, Co-P and Co-Sn-P. The samples were next run in a tool in which 500 Å of SiCOH dielectric material was applied over the surface of the cap layer. Some samples were thermally annealed after the electroless deposition process and after the deposition of SiCOH layer, while others only after SiCOH. The results shown in Figure 6 indicate that Co-W-P produces the best adhesion values.

The samples shown in Figure 6 were further tested by SIMS analysis for checking the thermal copper migration across the Co-W- P film. The SIMS data indicate that copper stays behind the cap layer and does not migrate to the dielectric layer as predicted.

Test data found increased adhesion of dielectric SiCOH to Cu by using a Co-W-P inner-layer are shown in Figure 6. It has been found that the adhesion of the dielectric SiCOH layer to copper can be increased significantly by using a reducing atmosphere pretreatment after the dielectric application. Best results are obtained by using a Co-W-P cap layer and annealing in forming gas at 350°C for at least 2 hours after the SiCOH deposition. These samples appear to be failing at the correct interface, i.e. SiCOH to the electrolessly deposited layer, as

opposed to when the system is not annealed after SiCOH when the adhering, annealed films were failing below the copper layer.

The present invention novel method and device formed by the method have therefore been amply described in the above description and in the appended drawings of Figures 1 through 6. It has been shown that the technical issues and problems in the single use of low k dielectric materials such as SiCOH is due to the fact that SiCOH does not have good adhesion to copper, and SiCOH is somewhat permeable to oxygen. These two factors thus combined to cause copper oxidation and delamination at the interface of dielectric/copper resulting in reliability problems. The present invention novel method therefore utilizes a dual-layer
barrier, for instance, Cu/Co-W-P/SiCOH and Cu/Co-Sn-P/SiCOH so that copper does not move through the layer of the electrolessly deposited cap layer of the metal alloy and remains behind it, even after annealing at 380°C for 2 hours.

While the present invention has been described in an illustrative manner, it should be understood that the terminology used is intended to be in a nature of words of description rather than of limitation.

Furthermore, while the present invention has been described in terms of a preferred and alternate embodiment, it is to be appreciated that those skilled in the art will readily apply these teachings to other possible variations of the inventions.

The embodiment of the invention in which an exclusive property or privilege is claimed are defined as follows.

Claims

1. A method for forming a dual-layer low dielectric barrier on a copper conductor comprising the steps:

providing a pre-processed substrate having a copper conductor formed in an insulator layer;

depositing a phosphorus or boron-containing metal alloy film on top of said copper conductor;

heating said pre-processed substrate in a first heating process to a temperature of at least 300°C in a reducing atmosphere for a length of time sufficient for said phosphorus or boron- containing metal alloy to diffuse into at least three atomic layers in a top surface of said copper conductor;

depositing a low k dielectric film on top of said phosphorus or boron-containing metal alloy film; and

heating said pre-processed substrate in a second heating process in a reducing atmosphere to a temperature of at least 300°C for at least 1 hour.

2. A method for forming a dual-layer low dielectric barrier on a copper conductor according to claim 1, wherein said first heating process being conducted at a temperature of at least 325°C for at least 1 hour.

3. A method for forming a dual-layer low dielectric barrier on a copper conductor according to claim 1, wherein said second heating process being conducted at a temperature of at least 350°C for at least 2 hours.

4. A method for forming a dual-layer low dielectric barrier on a copper conductor according to claim 1, wherein the metal layer and the dielectric layer are deposited sequentially with only one final thermal treatment after the dielectric deposition by heating for 2 hours at 400°C in a reducing atmosphere.

5. A method for forming a dual-layer low dielectric barrier on a copper conductor according to claim 1, wherein said deposition process for said phosphorus or boron-containing metal alloy film being conducted by an electroless plating technique.

6. A method for forming a dual-layer low dielectric barrier on a copper conductor according to claim 1, wherein said dielectric film being deposited on said phosphorus or boron-containing metal alloy film by a plasma enhanced chemical vapor deposition technique.

7. A method for forming a dual-layer low dielectric barrier on a copper conductor according to claim 1, wherein said reducing atmosphere used in said first and second heating process is a forming gas, nitrogen or hydrogen.

8. A method for forming a dual-layer low dielectric barrier on a copper conductor according to claim 1 further comprising the step of depositing a nucleation layer of palladium on said pre-processed substrate prior to said step of depositing said phosphorus or boron-containing metal alloy film.

9. A method for forming a dual-layer low dielectric barrier on a copper conductor according to claim 1, wherein said phosphorus or boron-containing metal alloy film is Me-X-P or Me-X- B, wherein Me is a primary component of said alloy film and X is an alloy modifier.

10. A method for forming a dual-layer low dielectric barrier on a copper conductor according to claim 1 further comprising the step of depositing a palladium nucleation layer on said copper conductor by a selective ion exchange method utilizing a diluted palladium sulfate solution in sulfuric acid.

11. A method for forming a dual-layer low dielectric barrier on a copper conductor according to claim 9, wherein said phosphorus or boron-containing metal alloy film further comprises between about 86 wt % and about 90 wt % Me, between about 2 wt % and about 4 wt % X, and between about 6 wt % and about 12 wt% P or B.

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12. A method for forming a dual-layer low dielectric barrier on a copper conductor according to claim 1, wherein said dielectric film deposited has a dielectric constant of not more than 5.

13. A method for forming a dual-layer low dielectric barrier on a copper conductor according to claim 1 further comprising the step of depositing said phosphorus or boron-containing metal alloy film to a thickness between about 50 Å and about 300 Å.

14. A method for forming a dual-layer low dielectric barrier on a copper conductor according to claim 1 further comprising the step of depositing said phosphorus or boron-containing metal alloy film to a thickness between about 50 Å and about 300 Å, and preferably between about 100 Å and about 200 Å.

15. A method for forming a dual-layer low dielectric barrier on a copper conductor according to claim 1 further comprising the step of depositing said phosphorus or boron-containing metal alloy film by an electroless deposition process in a hypophosphite solution containing cobalt sulfate, ammonium tungstate, sodium citrate and boric acid at a temperature between about 70°C and about 80°C, a pH value between about 8 and about 9.

16. A method for forming a dual-layer low dielectric barrier on a copper conductor according to claim 1 further comprising the step of conducting said first heating process at a temperature between about 350°C and about 400°C for a time period between about 0.5 hour and about 2 hours.

17. A method for forming a dual-layer low dielectric barrier on a copper conductor according to claim 1 further comprising the step of depositing said dielectric film of a material selected from the group consisting of Si, C, O, N and H.

18. A method for forming a dual-layer low dielectric barrier on a copper conductor according to claim 1 further comprising the step of depositing said dielectric film to a thickness between about 100 Å and about 500 Å.

19. A method for forming a dual-layer low dielectric barrier on a copper conductor according to claim 1 further comprising the step of depositing said dielectric film to a thickness between about 100 Å and about 500 Å, and preferably between about 250 Å and about 350 Å.

20. A method for forming a dual-layer low dielectric barrier on a copper conductor according to claim 1 further comprising the step of conducting said second heating process at a temperature between about 350°C and about 400°C for a time period between about 1 hour and about 5 hours.

21. A method for forming a dual-layer low dielectric barrier on a copper conductor according to claim 9, wherein said Me is Co or Ni, said X is W or Sn.

22. An electrical conductor in a semiconductor structure comprising:

a copper conductor situated in an insulator layer;

a film of a phosphorus or boron-containing metal alloy being diffused into at least three atomic layers in a top surface of said metal conductor; and

a film of a low k dielectric material on top of said phosphorus or boron-containing metal alloy film.

23. An electrical conductor in a semiconductor structure according to claim 22, wherein said phosphorus or boron-containing metal alloy is present under at least two atomic layers in a top surface of said metal conductor.

24. An electrical conductor in a semiconductor structure according to claim 22, wherein said phosphorus or boron-containing metal alloy is a binary or ternary alloy of Me-P, Me-B, Me-X-P or Me-X-B with Me being Co or Ni, and X being Si, W or Sn.

25. An electrical conductor in a semiconductor structure according to claim 22, wherein said phosphorus or boron-containing metal alloy is a binary or ternary alloy of Me-P, Me-B, Me-X-P or Me-X-B with Me being Co or Ni, and X being Si, W or Sn deposited to a thickness between about 10 Å and about 1,000 Å.

26. An electrical conductor in a semiconductor structure according to claim 22, wherein said phosphorus or boron-containing metal alloy is a binary or ternary alloy of Me-P, Me-B, Me-X-P or Me-X-B with Me being Co or Ni, and X being Si, W or Sn being deposited to a thickness preferably between about 50 Å and about 200 Å.

27. An electrical conductor in a semiconductor structure according to claim 22, wherein said phosphorus or boron-containing metal alloy is a binary or ternary alloy of Me-P, Me-B, Me-X-P or Me-X-B with Me being Co or Ni, and X being Si, W or Sn being deposited to a thickness between about 10 Å and about 1,000 Å by an electroless plating technique.

28. An electrical conductor in a semiconductor structure according to claim 22, wherein said dielectric material has a dielectric constant of not more than 5.

29. An electrical conductor in a semiconductor structure according to claim 22, wherein said dielectric material contains Si, C, O, N and H.

30. An electrical conductor in a semiconductor structure according to claim 22, wherein said dielectric material is selected from the group consisting of a material containing Si, C, O, N and H and a material containing Si, C, H and deposited to a thickness of between about 10 Å and about 5,000 Å.

31. An electrical conductor in a semiconductor structure according to claim 22, wherein said dielectric material contains Si, C, O, N and H deposited to a thickness between about 100 Å and about 500 Å.

32. An electrical conductor in a semiconductor structure according to claim 22, wherein said semiconductor structure being formed on a substrate selected from the group consisting of silicon, silicon germanium, silicon-on-insulator and gallium arsenide.