

ABSTRACT

A non-volatile memory device includes a memory cell region and a peripheral circuit region. The memory cell region includes an upper substrate, channel structures, and a first upper metal line extending in a first direction. The peripheral circuit region includes a first lower metal line extending in a second direction and a first via structure on the first lower metal line and a second via structure on the first lower metal line, a top surface of the second via being in contact with the upper substrate. The memory cell region further includes a first through-hole via structure passing through the upper substrate and the first via structure, and electrically connecting the first upper metal line to the first lower metal line; and the first upper metal line is electrically connected to the upper substrate through the first through-hole via structure, the first lower metal line, and the second via structure.

FIG. 8