CLAIMS:

1. A multilayer structure comprising:

a single crystal silicon wafer handle substrate comprising two major, generally parallel surfaces, one of which is a front surface of the single crystal silicon wafer handle substrate and the other of which is a back surface of the single crystal silicon wafer handle substrate, a circumferential edge joining the front and back surfaces of the single crystal silicon wafer handle substrate, and a central plane of the single crystal silicon wafer handle substrate between the front and back surfaces of the single crystal silicon wafer handle substrate, wherein the single crystal silicon wafer handle substrate has a bulk resistivity of at least about 5000 ohm-cm, an interstitial oxygen concentration of less than about $1x10^{16}$ atoms/cm^3, and a nitrogen concentration of at least about $1x10^{13}$ atoms/cm^3 and further wherein the single crystal silicon wafer handle substrate comprises a p-type dopant at a concentration of less than $1x10^{12}$ atoms/cm^3 and further wherein a concentration of oxygen thermal double donors, new donors, and excess thermal donors, or any combination thereof is at least an order of magnitude less than the concentration of the p-type dopant;

a trap rich layer in interfacial contact with the front surface of the single crystal silicon wafer handle substrate;

a dielectric layer in interfacial contact with the trap rich layer; and

a single crystal semiconductor device layer in interfacial contact with the dielectric layer.

2. The multilayer structure of claim 1 wherein the single crystal silicon wafer handle substrate comprises a silicon wafer sliced from a single crystal silicon ingot grown by the float zone method and further wherein the wafer has a diameter of at least about 150 mm.

3. The multilayer structure of claim 1 wherein the single crystal silicon wafer handle substrate comprises a silicon wafer sliced from a single crystal silicon ingot grown by the float zone method and further wherein the silicon wafer has a diameter of at least about 200 mm.

4. The multilayer structure of claim 1 wherein the single crystal silicon wafer handle substrate has a bulk resistivity of at least about 7,500 ohm-cm.

5. The multilayer structure of claim 1 wherein the single crystal silicon wafer handle substrate has a bulk resistivity of at least about 10,000 ohm-cm.

6. The multilayer structure of claim 1 wherein the single crystal silicon wafer handle substrate has a bulk resistivity of at least about 15,000 ohm-cm.

7. The multilayer structure of claim 1 wherein the single crystal silicon wafer handle substrate has a bulk resistivity of at least about 20,000 ohm-cm.

8. The multilayer structure of claim 1 wherein the single crystal silicon wafer handle substrate has a bulk resistivity of less than about 100,000 ohm-cm.

9. The multilayer structure of claim 1 wherein the single crystal silicon wafer handle substrate has an excess thermal donor concentration of less than $1x10^{11}$ donors/cm^3.

10. The multilayer structure of claim 1 wherein the single crystal silicon wafer handle substrate has an excess thermal donor concentration of less than $5x10^{10}$ donors/cm^3.

11. The multilayer structure of claim 1 wherein the single crystal silicon wafer handle substrate comprises a p-type dopant at a concentration of less than $1x10^{11}$ atoms/cm^3 and further wherein the concentration of oxygen thermal double donors, new donors, and excess thermal donors, or any combination thereof is at least an order of magnitude less than the concentration of the p-type dopant.

12. The multilayer structure of claim 1 wherein the single crystal silicon wafer handle substrate has an interstitial oxygen concentration of less than about $1x10^{15}$ atoms/cm^3.

13. The multilayer structure of claim 1 wherein the single crystal silicon wafer handle substrate has a nitrogen concentration of at least about $1x10^{14}$ atoms/cm^3.

14. The multilayer structure of claim 1 wherein the single crystal silicon wafer handle substrate has a nitrogen concentration of less than about $3x10^{15}$ atoms/cm^3.

15. The multilayer structure of claim 1 wherein the single crystal silicon wafer handle substrate has a nitrogen concentration of less than about $1x10^{15}$ atoms/cm^3.

16. The multilayer structure of claim 1 wherein the single crystal silicon wafer handle substrate has a nitrogen concentration of less than about $7x10^{14}$ atoms/cm^3.

17. The multilayer structure of claim 1 wherein the single crystal silicon wafer handle substrate has a nitrogen concentration between about $5x10^{14}$ atoms/cm^3 and about $2x10^{15}$ atoms/cm^3.

18. The multilayer structure of claim 1 wherein the trap rich layer comprises one or more polycrystalline semiconductor layers, wherein each of the one or more polycrystalline semiconductor layers comprises a material selected from the group consisting of silicon, SiGe, SiC, and Ge.

19. The multilayer structure of claim 1 wherein the trap rich layer comprises one or more amorphous semiconductor layers, wherein each of the one or more amorphous semiconductor layers comprises a material selected from the group consisting of silicon, SiGe, SiC, and Ge.

20. The multilayer structure of claim 1 wherein the trap rich layer has a resistivity greater than about 1000 Ohm-cm.

21. The multilayer structure of claim 1 wherein the trap rich layer has a resistivity greater than about 3000 Ohm-cm.

22. The multilayer structure of claim 1 wherein the trap rich layer has a resistivity between about 2000 Ohm-cm and about 10,000 Ohm-cm.

23. The multilayer structure of claim 1 wherein the trap rich layer has a resistivity between about 3000 Ohm-cm and about 10,000 Ohm-cm.

24. The multilayer structure of claim 1 wherein the trap rich layer has a resistivity between about 3000 Ohm-cm and about 5,000 Ohm-cm.

25. The multilayer structure of claim 1 wherein the trap rich layer has a thickness between about 0.1 micrometer and about 50 micrometers.

26. The multilayer structure of claim 1 wherein the dielectric layer comprises a material selected from among silicon dioxide, silicon nitride, silicon oxynitride, hafnium oxide, titanium oxide, zirconium oxide, lanthanum oxide, barium oxide, aluminum oxide, aluminum nitride, and any combination thereof.

27. A multilayer structure comprising:

a single crystal silicon wafer handle substrate comprising two major, generally parallel surfaces, one of which is a front surface of the single crystal silicon wafer handle substrate and the other of which is a back surface of the single crystal silicon wafer handle substrate, a circumferential edge joining the front and back surfaces of the single crystal silicon wafer handle substrate, and a central plane of the single crystal silicon wafer handle substrate between the front and back surfaces of the single crystal silicon wafer handle substrate, wherein the single crystal silicon wafer handle substrate has a bulk resistivity of at least about 5000 ohm-cm, an interstitial oxygen concentration of less than about $1x10^{16}$ atoms/cm^3, and a nitrogen concentration of at least about $1x10^{13}$ atoms/cm^3 and further wherein the single crystal silicon wafer handle substrate comprises an n-type dopant at a concentration of less than $1x10^{12}$ atoms/cm^3 and further wherein a concentration of oxygen thermal double donors, new donors, and excess thermal donors, or any combination thereof is at least an order of magnitude less than the concentration of the n-type dopant;

a trap rich layer in interfacial contact with the front surface of the single crystal silicon wafer handle substrate;

a dielectric layer in interfacial contact with the trap rich layer; and

a single crystal semiconductor device layer in interfacial contact with the dielectric layer.

28. The multilayer structure of claim 27 wherein the single crystal silicon wafer handle substrate comprises a silicon wafer sliced from a single crystal silicon ingot grown by a float zone method and further wherein the silicon wafer has a diameter of at least about 150 mm.

29. The multilayer structure of claim 27 wherein the single crystal silicon wafer handle substrate comprises a silicon wafer sliced from a single crystal silicon ingot grown by a float zone method and further wherein the silicon wafer has a diameter of at least about 200 mm.

30. The multilayer structure of claim 27 wherein the single crystal silicon wafer handle substrate has a bulk resistivity of at least about 7,500 ohm-cm.

31. The multilayer structure of claim 27 wherein the single crystal silicon wafer handle substrate has a bulk resistivity of at least about 10,000 ohm-cm.

32. The multilayer structure of claim 27 wherein the single crystal silicon wafer handle substrate has a bulk resistivity of at least about 15,000 ohm-cm.

33. The multilayer structure of claim 27 wherein the single crystal silicon wafer handle substrate has a bulk resistivity of at least about 20,000 ohm-cm.

34. The multilayer structure of claim 27 wherein the single crystal silicon wafer handle substrate has a bulk resistivity of less than about 100,000 ohm-cm.

35. The multilayer structure of claim 27 wherein the single crystal silicon wafer handle substrate has an excess thermal donor concentration of less than $1x10^{11}$ donors/cm^3.

36. The multilayer structure of claim 27 wherein the single crystal silicon wafer handle substrate has an excess thermal donor concentration of less than $5x10^{10}$ donors/cm^3.

37. The multilayer structure of claim 27 wherein the single crystal silicon wafer handle substrate comprises the n-type dopant at a concentration of less than $1x10^{11}$ atoms/cm^3 and further wherein the concentration of oxygen thermal double donors, new donors, and excess thermal donors, or any combination thereof is at least an order of magnitude less than the concentration of the n-type dopant.

38. The multilayer structure of claim 27 wherein the single crystal silicon wafer handle substrate has the interstitial oxygen concentration of less than about $1x10^{15}$ atoms/cm^3.

39. The multilayer structure of claim 27 wherein the single crystal silicon wafer handle substrate has the nitrogen concentration of at least about $1x10^{14}$ atoms/cm^3.

40. The multilayer structure of claim 27 wherein the single crystal silicon wafer handle substrate has the nitrogen concentration of less than about $3x10^{15}$ atoms/cm^3.

41. The multilayer structure of claim 27 wherein the single crystal silicon wafer handle substrate has the nitrogen concentration of less than about $1x10^{15}$ atoms/cm^3.

42. The multilayer structure of claim 27 wherein the single crystal silicon wafer handle substrate has the nitrogen concentration of less than about $7x10^{14}$ atoms/cm^3.

43. The multilayer structure of claim 27 wherein the single crystal silicon wafer handle substrate has the nitrogen concentration between about $5x10^{14}$ atoms/cm3 and about $2x10^{15}$ atoms/cm^3.

44. The multilayer structure of claim 27 wherein the trap rich layer comprises one or more polycrystalline semiconductor layers, wherein each of the one or more polycrystalline semiconductor layers comprises a material selected from a group consisting of silicon, SiGe, SiC, and Ge.

45. The multilayer structure of claim 27 wherein the trap rich layer comprises one or more amorphous semiconductor layers, wherein each of the one or more amorphous semiconductor layers comprises a material selected from a group consisting of silicon, SiGe, SiC, and Ge.

46. The multilayer structure of claim 27 wherein the trap rich layer has a resistivity greater than about 1000 Ohm-cm.

47. The multilayer structure of claim 27 wherein the trap rich layer has a resistivity greater than about 3000 Ohm-cm.

48. The multilayer structure of claim 27 wherein the trap rich layer has a resistivity between about 2000 Ohm-cm and about 10,000 Ohm-cm.

49. The multilayer structure of claim 27 wherein the trap rich layer has a resistivity between about 3000 Ohm-cm and about 10,000 Ohm-cm.

50. The multilayer structure of claim 27 wherein the trap rich layer has a resistivity between about 3000 Ohm-cm and about 5,000 Ohm-cm.

51. The multilayer structure of claim 27 wherein the trap rich layer has a thickness between about 0.1 micrometer and about 50 micrometers.

52. The multilayer structure of claim 27 wherein the dielectric layer comprises a material selected from among silicon dioxide, silicon nitride, silicon oxynitride, hafnium oxide, titanium oxide, zirconium oxide, lanthanum oxide, barium oxide, aluminum oxide, aluminum nitride, and any combination thereof.