CLAIMS

WE CLAIM:

1. A method, comprising:

forming a recess in a dielectric layer of a substrate;

forming a first transition metal layer in the recess on corner portions of the recess;

forming a second transition metal layer in the recess over the first transition metal layer to line the recess;

filling the recess with a fill layer;

annealing the substrate, wherein the first transition metal layer and the second transition metal layer form an alloy portion proximate the corner portions during the annealing, wherein the alloy portion has a reduced wettability for a material of the fill layer than the second transition metal; and

polishing the substrate to remove portions of the fill layer extending above the recess.

2. The method of claim 1, wherein the fill layer comprises copper.

3. The method of claim 1, wherein filling the recess comprises forming a seed layer over the second transition metal layer and forming material of the fill layer over the seed layer.

4. The method of claim 1, wherein the second transition metal layer comprises ruthenium.

5. The method of claim 4, wherein the first transition metal layer comprises titanium.

6. The method of claim 1, wherein polishing the wafer comprises forming a recess between the fill layer and the alloy portion proximate the corner portion.

7. The method of claim 1, wherein the first transition metal is substantially absent from sidewall and bottom portions of the recess.

8. The method of claim 1, further comprising forming a barrier layer in the recess prior to forming the first transition metal layer.

9. The method of claim 8, wherein the barrier layer comprises tantalum nitride.

10. The method of claim 1, wherein the recess comprises a trench.

11. The method of claim 1, wherein the recess comprises a via opening.

12. A method, comprising:

forming a recess in a dielectric layer of a substrate;

forming a titanium layer in the recess on corner portions of the recess;

forming a ruthenium layer over the titanium layer to line the recess;

filling the recess with copper;

annealing the substrate, wherein the titanium layer and the ruthenium layer form an alloy portion proximate the corner portions during the annealing; and

polishing the substrate to remove portions of the copper extending above the recess.

13. The method of claim 12, further comprising forming a barrier layer in the recess prior to forming the titanium layer.

14. A semiconductor device, comprising:

a recess having a corner portion defined in a dielectric layer;

an interconnect structure defined in the recess, the interconnect structure comprising:

an alloy of a first and second transition metal disposed on the corner portion;

a layer of the second transition metal lining sidewall portions of the recess; and

a fill material substantially filling the recess, wherein the second transition metal has a higher wettability for the fill material than the alloy.

15. The device of claim 14, further comprising a barrier layer disposed in the recess beneath the alloy layer and the layer of the second transition metal.

16. The device of claim 14, wherein the second transition metal comprises ruthenium.

17. The device of claim 16, wherein the first transition metal comprises titanium.

18. A semiconductor device, comprising:

a recess having a corner portion defined in a dielectric layer;

an interconnect structure defined in the recess, the interconnect structure comprising:

an alloy of titanium and ruthenium disposed on the corner portion;

a layer of ruthenium lining sidewall portions of the recess; and

copper substantially filling the recess.

19. The device of claim 18, further comprising a barrier layer disposed in the recess beneath the alloy and the layer of ruthenium.

20. The device of claim 19, wherein the barrier layer comprises tantalum nitride.

CLAIMS

1. A method, comprising:

forming a recess in a dielectric layer of a substrate, said recess having corner portions adjacent an upper surface of said dielectric layer and sidewalls having a substantially vertical length;

forming a first transition metal layer in the recess above said corner portions of the recess and above a portion, but not all, of said vertical length of said sidewalls of said recess;

forming a second transition metal layer in the recess over the first transition metal layer to line the recess;

filling the recess with a fill layer;

annealing the substrate, wherein the first transition metal layer and the second transition metal layer form an alloy portion proximate at least the corner portions during the annealing, wherein the alloy portion has a reduced wettability for a material of the fill layer than the second transition metal; and

polishing the substrate to remove portions of the fill layer extending above the recess.

2. The method of claim 1, wherein the fill layer comprises copper.

3. The method of claim 1, wherein filling the recess comprises forming a seed layer over the second transition metal layer and forming material of the fill layer over the seed layer.

4. The method of claim 1, wherein the second transition metal layer comprises ruthenium.

5. The method of claim 4, wherein the first transition metal layer comprises titanium.

6. The method of claim 1, wherein polishing the wafer results in the formation of a recess between the fill layer and the alloy portion proximate the corner portion.

7. The method of claim 1, wherein the first transition metal is substantially absent from bottom portions of the recess.

8. The method of claim 1, further comprising forming a barrier layer in the recess prior to forming the first transition metal layer.

9. The method of claim 8, wherein the barrier layer comprises tantalum nitride.

10. The method of claim 1, wherein the recess comprises a trench.

11. The method of claim 1, wherein the recess comprises a via opening.

12. A method, comprising:

forming a recess in a dielectric layer of a substrate, said recess having corner portions adjacent an upper surface of said dielectric layer and sidewalls having a substantially vertical length;

forming a titanium layer in the recess above said corner portions of the recess and above a portion, but not all, of said vertical length of said sidewalls of said recess;

forming a ruthenium layer over the titanium layer to line the recess;

filling the recess with copper;

annealing the substrate, wherein the titanium layer and the ruthenium layer form an alloy portion proximate the corner portions during the annealing; and

polishing the substrate to remove portions of the copper extending above the recess.

13. The method of claim 12, further comprising forming a barrier layer in the recess prior to forming the titanium layer.

14. The method of claim 1, wherein forming said first transition metal layer comprises performing a plasma assisted physical vapor deposition process without a bias voltage to form said first transition metal layer.

15. The method of claim 12, wherein forming said titanium layer comprises performing a plasma assisted physical vapor deposition process without a bias voltage to form said titanium layer.

16. An interconnect structure fabricated in accordance with any one of the preceding claims.

17. An integrated circuit device having an interconnect structure fabricated in accordance with any one of the claims 1-15.