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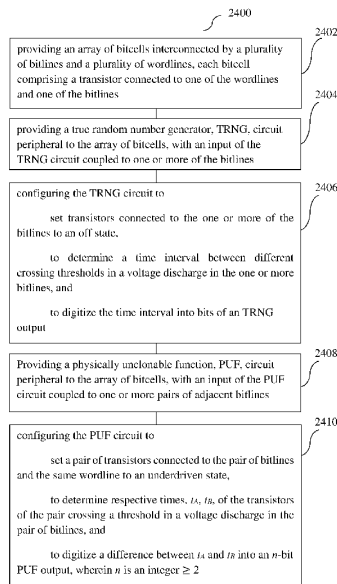


Figure 24

(57) Abstract: Embedded memory structures and methods of fabricating an embedded memory structure. In one embodiment, the method comprises providing an array of bitcells interconnected by a plurality of bitlines and a plurality of wordlines, each bitcell comprising a transistor connected to one of the wordlines and one of the bitlines; providing a TRNG circuit peripheral to the array of bitcells, with an input of the TRNG circuit coupled to one or more of the bitlines; configuring the TRNG circuit to set transistors connected to the one or more of the bitlines to an off state, to determine a time interval between different crossing thresholds in a voltage discharge in the one or more bitlines, and to digitize the time interval into bits of a TRNG output; providing a PUF circuit peripheral to the array of bitcells, with an input of the PUF circuit coupled to one or more pairs of adjacent bitlines; and configuring the PUF circuit to set a pair of transistors connected to the pair of bitlines and the same wordline to an underdriven state, to determine respective times, t_A , t_B , of the transistors of the pair crossing a threshold in a voltage discharge in the pair of bitlines, and to digitize a difference between t_A and t_B into an n -bit PUF output, wherein n is an integer ≥ 2 .

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