

METHOD AND SYSTEM FOR TESTING INTEGRATED CIRCUIT DEVICES AT
THE WAFER LEVEL

BACKGROUND OF THE INVENTION

1. Technical Field:

The present invention relates to a method and system for providing a passive electrical test structure for wafer-level testing of integrated circuit devices. In particular, the present invention relates to a method and system for interconnecting integrated circuit devices that permits wafer-wide testing of device functionality in an efficient and cost-effective manner. More particularly, the present invention relates to a method and system that utilize unoccupied regions of a wafer that separate successive rows and columns of integrated circuit devices, referred to hereinafter as "kerf" regions, as the staging areas from which to electrically access and interconnect the input/output contacts of multiple integrated circuit devices. Still more particularly, the present invention relates to a method and system for wafer-level integrated circuit device testing wherein an orthogonal grid of conductive traces is formed in the kerf regions of a wafer, thereby providing a reliable and efficient test structure that does not diminish the amount of wafer surface area available for product devices.

2. Description of the Related Art:

Mechanically probing each integrated circuit device (hereinafter "device") on a semiconductor wafer (hereinafter "wafer") to apply an electrical test is very expensive and

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slow. Very accurate X, Y and Z spatial positioning is required, and very small geometry device input/output peripheral or area array probe pads make reliable electrical contact very difficult, requiring very fine geometry precision probes. This difficult, slow probing process is a major contributor to device manufacturing test costs. Imperfect test probe contact can reduce wafer yield by causing a defect-free device to appear to be defective during testing thus causing it to be discarded. Furthermore, as the number of device input/output connections, commonly known as device input/output "counts", increase, as device operating frequency increases, and as power consumption increases, the physical and electrical limits of mechanical probing will limit the possible number of device input/output counts, testing frequency and maximum device power.

In response to these problems, increasing emphasis is being placed on designing integrated circuit devices to accommodate device testing methods which reduce the number of input/output pads that must be physically contacted, while maintaining test comprehensiveness. One such design structure, known as boundary-scan test design, is described by R.W. Basset et al., in "Boundary Scan Design Principles for Efficient LSSD ASIC Testing", IBM J. Res. Develop. Vol. 34, No. 2/3, March/May 1990, which is incorporated in its entirety by reference. Boundary-scan testing utilizes a design in which multiple shift register latches (SRLs) are cascaded in series. In test mode, data may be serially scanned in or out of the SRLs at the input/output periphery of the devices to be tested. The testing process is simplified to inputting a known data sequence, from the cascaded SRLs to the functional circuitry, storing the results, and shifting the stored values

out of the SRLs.

A problem associated with boundary-scan testing is that, although such testing does verify the functionality of internal device circuitry, such testing does not permit comprehensive testing of the integrity of the external input/output pad structure. An invention that addresses this problem is described by Walther, Dasgupta and Srikishnan in U.S. Pat. No. 5,787,098, "Complete Chip I/O Test Through Low Contact Testing Using Enhanced Boundary Scan", issued on July 28, 1998. This invention describes a method for evaluating the integrity of solder ball input/output pads and is incorporated in its entirety by reference.

Based on the foregoing, it can be appreciated that a need exists for a method and system that utilize an electrical interconnection network among the integrated circuit devices on a wafer in order to reduce or eliminate the need to use mechanical probing for wafer-level testing of the integrated circuit devices. Such a method and system would be useful by providing simultaneous electrical access to the input/output contacts of multiple integrated circuit devices, thereby providing a means with which to test multiple integrated circuit devices at the wafer level with greater efficiency and effectiveness.

SUMMARY OF THE INVENTION

It is therefore an object of the invention to provide a passive electrical test structure for wafer-level testing of integrated circuit devices.

It is another object of the invention to provide a method and system for interconnecting integrated circuit devices that permits wafer-wide testing of device functionality in an efficient and cost-effective manner.

It is still another object of the invention to provide a method and system that utilize the kerf regions of a wafer as the staging areas from which to electrically access and interconnect the input/output contacts of multiple integrated circuit devices.

It is yet another object of the invention to provide a method and system for wafer-level integrated circuit device testing wherein an orthogonal grid of conductive traces is formed in the kerf regions of a wafer, thereby providing a reliable and efficient test structure that does not diminish the amount of wafer surface area available for product devices.

The above and other objects are achieved as is now described. A method and system are disclosed that utilize a passive electrical network for wafer-level testing of integrated circuit devices. According to the present invention, multiple integrated circuit devices are formed on a semiconductor wafer in a fabrication process. During, and as a part of the process by which the integrated circuit

devices are fabricated on the wafer, conductive traces, conductive straps and test pads are deposited onto otherwise unoccupied areas of the wafer. Such unoccupied areas include regions at the wafer periphery and the kerf regions that separate adjacent integrated circuit devices. The conductive traces form a conductive network confined to the kerf regions between adjacent integrated circuit devices. The conductive straps are utilized both to strategically interconnect the conductive traces and also to connect the traces to input/output contacts on the integrated circuit devices. The test pads are formed on the unused peripheral regions of the wafer and are electrically connected to the conductive trace network. An on-wafer electrical testing structure is thereby formed from which the integrated circuit devices can be tested prior to being cut from the wafer.

BRIEF DESCRIPTION OF THE DRAWINGS

The novel features believed characteristic of the invention are set forth in the appended claims. The invention itself, however, as well as a preferred mode of use, further objects, and advantages thereof, will best be understood by reference to the following detailed description of an illustrative embodiment when read in conjunction with the accompanying drawings, wherein:

FIG. 1 depicts a conceptual layout of a wafer and how large geometry test pads are positioned to feed or be fed by all or subsets (columns or rows) of integrated circuit devices in accordance with a preferred embodiment of the present invention;

FIG. 2 illustrates a 2x2 matrix of integrated circuit devices from among an m-by-n array of integrated circuit devices in a wafer in accordance with a preferred embodiment of the present invention;

FIG. 3A depicts a typical wafer level map in accordance with a preferred embodiment of the present invention;

FIG. 3B illustrates some of the details of the kerf region immediately adjacent to an integrated circuit device;

FIG. 4 depicts a magnified region of a wafer in accordance with a preferred embodiment of the wafer-level test structure invention;

FIG. 5 illustrates a magnified portion of a wafer kerf

region on which conductive traces have been formed in accordance with a preferred embodiment of the present invention;

FIG. 6 is a graphical representation of the orientation of typical integrated circuit device input/output contacts; and

FIG. 7 illustrates the integrated circuit device interconnection network near the perimeter of a wafer in accordance with a preferred embodiment of the present invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENT

The present invention, in a preferred embodiment, is utilized in conjunction with both boundary-scan "reduced pins" testing techniques and the enhancement described in the aforementioned U.S. Pat. No. 5,787,098 and applies those techniques to the testing of entire wafers in order to achieve reduced pins testing at the wafer level as well as creating a structure that no longer requires complex test fixtures nor the step and repeat process in which probes are moved from device to device during wafer level testing. This improvement will reduce the cost of wafer-level testing by reducing testing time and by reducing the complexity of the test fixture. Fixed larger geometry contacts also remove the uncertainty of making good contact between probes and pads associated with known wafer steppers and probers, thus eliminating the false yield loss due to poor electrical contact.

A wafer-level integrated circuit device testing structure and processes for forming and utilizing the same are now described. Such a structure or a similar structure can be utilized for comprehensive wafer-level testing of integrated circuit devices. **FIGURES 1 and 2** each depict conceptual layouts of a wafer and, in conjunction, how common test pads are positioned to feed or be fed by all or subsets (rows or columns) of integrated circuit devices. **FIG. 3A** illustrates a typical wafer-level map. Note that the separation between integrated circuit device sites, shown as lines in **FIG. 3A**, in reality constitutes a kerf region typically between 0.3 to 0.9 mm wide, most of which is lost when the integrated circuit devices are cut from the wafer. Also note the shaded,

incomplete, unusable integrated circuit device sites 124 around the periphery of the wafer that leave room for the large geometry test pads. FIGURES 4 through 7 illustrate one of the methods for realizing the present invention in which a conductive trace network is formed in the kerf and perimeter regions of the wafer, with all the required connections necessary to implement the disclosed test structure.

A method and system for utilizing a testing structure to comprehensively test integrated circuit devices will first be described, followed by a description of its composition and how it is formed. FIG. 1 is an overhead schematic view depicting the allocation of the available surface area of semiconductor wafer 10, hereinafter wafer 10. Most of the surface area of wafer 10 is occupied by a product device region 12 that is populated by multiple integrated circuit devices including integrated circuit devices 24 and 26. Narrow, unoccupied pathways such as kerf region 14 lie among integrated circuit devices as depicted by kerf region 14 which is located between adjacent integrated circuit devices 24 and 26. The remaining surface area of wafer 10 lies outside of product device region 12 on the peripheral regions of wafer 10. As depicted in FIG. 1, the peripheral regions of wafer 10 can be utilized as a convenient location for placing power pads 16, ground pads 20, and test input/output pads 18 and 22.

Referring to FIG. 2, test control structure 30 is depicted for a 2x2 matrix of integrated circuit devices 32, 34, 36 and 38, from among an m-by-n array of integrated circuit devices on a wafer. FIG. 2 also depicts an example of

the types of common controls, such as test mode select lines 40 and 42 (TMS1 and TMS2) that can be utilized to test the devices. These controls connect to wafer-level test pads (depicted in FIG. 7 as test pads 300) that are fixed and do not need to be stepped from device to device. Given that test pads 300 are spaced around the periphery of the wafer and not crowded around a jig over a single device, there is a natural reduction in the complexity of the tester probe mechanics and electronics needed to provide noise-free, reliable, high-frequency signals. Power lines 46 and 48, and ground lines 60 and 62 supply all devices through shared grids per column or per row. In one embodiment of the present invention, test mode selection lines 40 and 42 (TMS1 and TMS2) as well as test clock line 44 (TCK) meet the IEEE 1149.1 standard for boundary-scan testing and can be utilized for testing devices as described below.

Level sensitive scan design (LSSD) clocks and controls 50, are the inputs that provide LSSD control of internal scan latches to provide scan, built-in self test (BIST), or other tests as required to supplement or to replace the tests applied per the IEEE 1149.1 standard. Also, two row select lines 52 and 54 (X1 and X2) from among a total of m row select lines, select individual rows of devices if needed. Similarly, two column select lines 56 and 58 (Y1 and Y2) from a total of n column select lines, select individual columns of devices if needed. When testing integrated circuit devices according to the IEEE 1149.1 standard, the Y-controls may not be necessary if the TMS lines can be utilized for column selection. Test data inputs 64 and 66 (TDI1 and TDI2 among m such inputs) each feed the scan inputs of all devices in a particular row of the wafer. Likewise, row-wise test data

outputs 68 and 70 (TDO1 and TDO2 among m such outputs) are fed by all of the scan outputs of a given row.

With the test control network implemented in accordance with FIG. 2, wafer-level testing of integrated circuit devices can be accomplished in several ways. To test all the devices in a single column simultaneously, all of the X-controls are enabled while only one of the Y-controls is selected, or the TMS lines are utilized to enable one device per row to be tested. The test data inputs 64 and 66 then feed test data to the selected device in each row. Likewise, the test data outputs 68 and 70 scan out the test results from the selected device in each row. This test control procedure allows m devices (one per row) to be tested simultaneously, leading to an m times increase in tester throughput. By sequencing through all of the TMS/Y-controls, all columns of devices can be tested in a total of n steps. For diagnostic purposes, a single row select line, 52 or 54, and a single columns select line, 56 or 58 are simultaneously activated to select an individual device which can then be analyzed with greater scrutiny than during a normal manufacturing test.

After wafer-level testing is complete, the integrated circuit devices are cut from the wafer and the test control lines, which reside in kerf regions, are destroyed. The fragments of test control lines which remain attached to each integrated circuit device, are no longer connected to test pads, and create a potential source of interference with device performance. To prevent these "loose ends" from interfering with device functionality, the testing network is originally designed so that the control lines connect to regular device input/output contacts that can eventually be

connected to power or ground or otherwise controlled so as not to introduce noise or interfere with the normal logical functionality of the design. Alternatively, the circuitry feeding or fed by the test pads can be designed so that these networks do not interfere with normal device operation.

The arrangement of a passive electrical testing structure and a set of processes for forming the same are now described by reference to **FIGURES 3A** through 7. The process steps described here are chosen for minimum deviation from conventional wafer processing steps. As described in the following sections, the aforementioned testing structure utilizes a network strategy wherein the input/output contacts of multiple integrated circuit devices are interconnected utilizing conductive traces formed in wafer kerf regions. This network strategy permits simultaneous wafer-level testing of multiple integrated circuit devices while reserving the maximum wafer surface area available for product devices.

FIG. 3A represents a wafer map wherein the rectangular blocks represent integrated circuit devices 120 (DRAMs for example), that are each bordered by kerf regions 122. An x-y coordinate is superimposed onto wafer 100 in **FIG. 3A** as a convenient reference. Integrated circuit devices 120 are oriented such that their sides are parallel to the x- and y-directions. Wafer notch 130 points along the y-direction.

The current generation of integrated circuit devices utilizes multilevel wiring to connect internal device circuitry with terminations (terminal vias or bonding pads) on the surface of the device. The internal device interconnections have wiring levels that are typically made of

Al-Cu and these wiring levels are separated by thin films of insulators. In some technologies, copper lines may be utilized in place of Al-Cu lines. Wiring patterns and vias in the insulators are defined by projection lithography (5X for example), utilizing steppers and reticles. Usually, each of the devices is exposed individually and one at a time.

Device fabrication concludes with the formation of device terminals, typically utilizing a 1X mask lithography procedure. The advantage of 1X lithography is that costs are reduced by exposing the entire wafer in one step. The device terminals are designed to be suitable for connection to a printed circuit (PC) board using either wire-bonding or IBM's controlled collapse chip solder ball connection (C4). Most semiconductor integrated circuit products such as microprocessors or application specific integrated circuits (ASICs), have wafer maps similar to that shown in **FIG. 3A**, except for the dimensions of the rectangles.

FIG. 3B depicts some of the details of a kerf reticle pattern **142** that is exposed along with the product at each level. As previously explained, a kerf region is generally defined as the narrow dicing lines separating adjacent integrated circuit device sites that is ultimately destroyed when the devices are cut from the wafer. The kerf region usually contains several functional regions including test structures, lithography and dicing marks, etc. **FIG. 3B** illustrates functional kerf regions **140** that are located along two edges of each device site **144**, and include lithography marks, such as alignment aids, critical dimension measurement sites (CDs) etc. Along another edge of device site **144**, is a rectangular test region **150** containing test structures for

yield and parametric measurements.

FIGURES 4 and 5 depict a magnified view of a portion of a wafer (not depicted) on which integrated circuit devices **162, 164, 166 and 168** reside. The horizontal conductive traces **160** and vertical conductive traces **180** are aligned in the illustrated x- and y-directions respectively, outside of test regions **150** or alignment regions **140** of kerf regions **145** and **155**. The dimensions of conductive traces **160** and **180** are magnified in **FIGURES 4 and 5** relative to test and alignment regions **140** and **150**. Actually, the space occupied by each group of conductive traces **160** and **180** is likely to be narrower than test and alignment regions **140** and **150**. Therefore, although conductive traces **160** and **180** are depicted as residing outside of test and alignment regions **140** and **150**, they can easily be located immediately adjacent to each of integrated circuit devices **162, 164, 166 and 168**, if so preferred by the design layout.

Conductive traces **180**, utilized to carry input/output signals, can be designed 5 μm wide with a 10 μm pitch, thus a space of approximately 50 μm would be required to accommodate 5 traces. A space of less than 0.1 mm (100 μm) would therefore be required to accommodate 5 traces on both sides of each device and would easily fit within kerf region **155** which is typically 0.3-0.9 mm wide. Conductive traces **160** are utilized to provide power and ground to the devices being tested and may be designed with wider conductors than those utilized for signal-carrying conductive traces **180**. For example, a wiring track consisting of four conductive traces, each 10 μm wide and spaced 5 μm apart, divided between the two

edges will occupy a width of less than 0.1 mm. Conductive traces 160 can be widened to accommodate higher currents if necessary. Given their relatively short duty cycle however, they can usually be designed for much higher currents than similar-sized conductive traces utilized in product devices.

As a reference for the following explanation, it will be assumed that the integrated circuit devices have a terminal metal layer which connects the devices to a printed circuit board or other suitable substrate, and that beneath the terminal metal, the wiring level will be called "final metal". For devices that do not have a terminal metal, the last two metalization layers (or wiring steps) will be utilized for the purpose of creating the testing structure.

Again referring to **FIGURES 4 and 5**, conductive traces 160 and 180 are formed at the same time the final metal level is defined and are made of the same metallurgy used at that level (Al-Cu, or Cu, for example). Conductive traces 160 and 180 are contained within the exposure field of a stepper as depicted in the magnified views of kerf regions 145 and 155. The patterns for conductive traces 160 and 180 are intentionally designed to remain outside of the active device region and entirely within the kerf regions, most of which will be destroyed when the devices are cut from the host wafer. If any portions of conductive traces 160 or 180 remain, the exposed Al or Cu trace material is isolated to the kerf region and does not affect the reliability of integrated circuit metallization. Dotted lines 190 illustrate the midpoint imaginary boundaries between adjacent device/kerf areas. Each trace stops short of crossing into an adjacent device/kerf area by several microns (5 to 50 um).

The patterns for conductive traces **160** and **180** are formed during the same processes utilized to define the wiring patterns in the product devices, namely wet or dry etching processes or damascene chemical/mechanical polishing. If for some types of products the wiring patterns at this level is formed by a 1X mask, then conductive traces **160** and **180** are formed utilizing the 1X mask.

After the final metal patterning step, in which the patterns for conductive traces **160** and **180** and the integrated circuit wiring are formed, the entire conductor pattern is encapsulated by an insulator (not depicted in **FIGURES 4** or **5**), usually plasma deposited silicon dioxide, and in some cases an organic insulator such as polyimide. The insulator provides a scratch resistant coating as well as providing insulation from potentially corrosive moisture.

Following deposition of the insulating layer, two sets of vias, **200** and **210**, are opened in the insulating layer. In the embodiment depicted in **FIG. 5**, vias **200** are opened near the ends of the segmented conductive traces **160** and **180** so that short conductive straps **220** can be utilized to form continuous but separate conduction paths along rows and columns of devices. In this way, all of the contiguous segments of conductive traces **160** are electrically connected and all of the contiguous segments of conductive traces **180** are electrically connected. Conductive paths **160** and **180** thereby form an orthogonal conductive network having continuous conductive paths in the illustrated x- and y-directions. **FIG. 4** depicts an alternative embodiment of the present invention in which conductive traces **180** are deposited as continuous

conduction paths in the y-direction. Vias 200 and conductive straps 220 are therefore only utilized to connect contiguous segments of conductive traces 160 which run in the x-direction. As depicted in FIGURES 4 and 5, vias 210 provide the contact points for electrically connecting conductive traces 160 and 180 to integrated circuit devices 162, 164, 166 and 168, at appropriate input/output contact locations utilizing conductive straps 240.

Vias 200 and 210 are both designed according to the same guidelines and both can be fully landed and wet or dry etched to provide specified slope wall characteristics. In one embodiment of the present invention, conductive straps 220 and 240 are formed utilizing metallurgy that can remain exposed on the device without concern for corrosion, preferably the same material used to form the wire bonding or soldering terminals such as layers of Cr-Cu-Cr, Ti/Pd/Au or Cr-Ni-Au. These straps are defined by a 1X mask, usually the same mask used to pattern the terminals. If the terminal process cannot be advantageously used to simultaneously define the straps, then an additional 1X mask level can be utilized to define these straps. Although conductive straps 240 are described as residing above the final metal layer, those skilled in the art will appreciate that the connections between conductive traces 160 and 180 and input/output contacts 235, can also be made utilizing wiring layers deposited below the final metal layer, with vias between layers making the connections.

FIG. 6 is a schematic representation of a typical integrated circuit device depicting how conductive straps 240 connect to input/output contacts 235. In one embodiment of

the present invention, a set of dummy pads 245 is added to device 250. As seen from the lower region of device 250, each of dummy pads 245 is connected to each of input/output contacts 235. In this variation of the present invention, conductive straps 240 connect with dummy pads 245 thereby keeping the surface of device input/output contacts 235 clear for other terminal connection needs.

FIG. 7 illustrates details of the testing structure near the perimeter of a semiconductor wafer 100 for one embodiment of the present invention. In this embodiment, if wafer 100 has 64 devices in an 8x8 array, and if 10 signal traces and 4 power/ground traces are required for each device, then a total of 80 conductive traces 180 are formed in the y-direction for supplying test signals, and 32 conductive traces 160 are formed in the x-direction for supplying power and ground. Conductive traces 180 are connected to test pads 300 near the perimeter of the wafer 100 by utilizing conductive straps 280. Those skilled in the art will appreciate that although not depicted in the accompanying figures, testing devices can be connected to test pads 300 to provide input test signals for wafer-level integrated circuit testing. Those skilled in the art will also appreciate that off-wafer receiving devices can be connected to test pads 300 to receive output test results.

Conductive traces 180 can be divided so that half of them are terminated on one end and the other half at the opposite end of the wafer, if desired. Though not depicted in **FIG. 7**, test pads similar to test pads 300 are placed on the left and right halves of wafer 100 and connect to conductive traces 160

by utilizing conductive straps similar to conductive straps 280. The patterns for conductive straps 280 and test pads 300 are formed at the same time, and utilize the same mask as for straps 220 and 240.

At the perimeter of semiconductor wafer 100, test pads 300 provide the capability of sending unique signals and/or power to a set of devices in a column (y-direction) or to send unique signals and/or power to a set of devices in a row (x-direction). Thus a unique device located at the intersecting point of a selected row and column can be tested, an entire column can be tested, an entire row can be tested, or all devices can be tested simultaneously if desired.

While the invention has been particularly shown as described with reference to a preferred embodiment, it will be understood by those skilled in the art that various changes in form and detail may be made therein without departing from the spirit and scope of the invention. It is therefore contemplated that such modifications can be made without departing from the spirit or scope of the present invention as defined in the appended claims.

CLAIMS:



What is claimed is:

1. A method of electrically accessing and interconnecting a plurality of integrated circuit devices at the wafer-level for the purpose of conducting wafer-level tests on said integrated circuit devices, said method comprising the steps of:

forming a plurality of integrated circuit devices on a semiconductor wafer, utilizing a fabrication process;

during said fabrication process, depositing one or more conductive traces onto kerf regions of said semiconductor wafer, thereby forming a conductive network;

during said fabrication process, depositing conductive straps that connect input/output contacts of one or more of said integrated circuit devices to one or more of said conductive traces within said conductive network;

during said fabrication process, forming test pads on unused peripheral regions of said semiconductor wafer; and

during said fabrication process, depositing conductive straps for connecting each of said conductive traces to one or more of said test pads, such that said plurality of integrated circuit devices may be tested.

2. The method of claim 1 wherein said conductive network forms an orthogonal grid of conductive traces among said integrated circuit devices in kerf regions surrounding each of



said integrated circuit devices.

3. The method of claim 1 further comprising the step of:

electrically connecting at least one testing device to said test pads in order to provide input test signals and power to said input/output contacts of said integrated circuit devices.

4. The method of claim 1 further comprising the step of:

electrically connecting at least one off-wafer receiving device to said test pads in order to receive and record output signals from said input/output contacts of said integrated circuit devices.

5. The method of claim 1 further comprising the step of:

utilizing mode select lines to selectively access subsets of said integrated circuit devices including rows and columns of said integrated circuit devices.

6. The method of claim 1 wherein:

all of said conductive traces forming said conductive network are deposited at the same metallization layer during said fabrication process.

7. The method of claim 1 wherein:

all of said conductive straps are deposited at the same metallization layer during said fabrication process.



8. A system for electrically accessing and interconnecting a plurality of integrated circuit devices at the wafer-level for the purpose of conducting wafer-level tests on said integrated circuit devices, said system comprising:

means for forming a plurality of integrated circuit devices on a semiconductor wafer utilizing a fabrication process;

means for depositing one or more conductive traces onto kerf regions of said wafer during said fabrication process, thereby forming a conductive network;

means for depositing conductive straps that connect input/output contacts of one or more of said integrated circuit devices to one or more of said conductive traces within said conductive network during said fabrication process;

means for forming test pads on unused peripheral regions of said wafer during said fabrication process; and

means for depositing conductive straps for connecting each of said conductive traces to one or more of said test pads during said fabrication process, such that said plurality of integrated circuit devices may be tested.

9. A system for testing a plurality of integrated circuit devices prior to said integrated circuit devices being cut from a semiconductor wafer, said system comprising:

a semiconductor wafer;



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a plurality of integrated circuit devices having input/output contacts, formed on said semiconductor wafer;

one or more conductive traces formed on unoccupied kerf regions of said semiconductor wafer;

means for electrically connecting said conductive traces to said input/output contacts of said integrated circuit devices;

test pads located on unused peripheral kerf regions of said semiconductor wafer; and

means for electrically connecting said conductive traces to said test pads, such that said plurality of integrated circuit devices may be tested.

10. The system of claim 8 wherein said conductive traces include mode select lines for selectively accessing subsets of said integrated circuit devices including rows and columns of said integrated circuit devices.

11. The system of claim 8 further comprising:

one or more testing devices for providing input test signals and power to said input/output contacts of said integrated circuit devices; and

means for electrically connecting said testing devices to said test pads.

12. The system of claim 10 further comprising:



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off-wafer receiving devices that receive output signals from said input/output contacts of said integrated circuit devices; and

means for electrically connecting said off-wafer receiving devices to said test pads.

13. The system of claim 10 wherein said testing devices utilize boundary scan testing techniques.

14. The system of claim 8 wherein said conductive traces form an orthogonal grid among said integrated circuit devices, said conductive traces all formed at one metallization layer.

15. A method of testing integrated circuit devices having input/output signal, power, and ground contacts, prior to said integrated circuit devices being cut from a semiconductor wafer, said method comprising the steps of:

forming a plurality of integrated circuit devices having input/output signal, power, and ground contacts, on a semiconductor wafer;

depositing a plurality of conductive traces in unoccupied portions of said semiconductor wafer including pathways between said integrated circuit devices, thereby forming a conductive network comprising columns of vertical traces that run continuously across said wafer, and rows of horizontal traces that are interrupted at points so as not to physically intersect said vertical traces;

integrating the deposition of said vertical traces and



horizontal traces into a single integrated circuit device fabrication step, such as a metallization layering step, so that no additional integrated circuit device fabrication steps are necessary to deposit said vertical and horizontal traces;

electrically connecting the interrupted paths of said horizontal traces utilizing conductive straps thereby forming continuous conduction paths in the horizontal direction while maintaining electrical isolation from said vertical traces;

electrically coupling said input/output signal contacts of one or more of said integrated circuit devices to said vertical traces;

electrically coupling said power, and ground contacts of one or more of said integrated circuit devices to said horizontal traces; and

electrically connecting said horizontal and vertical traces to test pads located on peripheral regions of said semiconductor wafer.

16. A system for testing integrated circuit devices having input/output signal, power, and ground contacts, prior to said integrated circuit devices being cut from a semiconductor wafer, said system comprising:

a plurality of integrated circuit devices having input/output signal, power, and ground contacts, formed on a semiconductor wafer;



a plurality of conductive traces formed in unoccupied portions of said semiconductor wafer including pathways between said integrated circuit devices, that form an orthogonal grid comprising columns of vertical traces that run continuously across said wafer, and rows of horizontal traces that are interrupted at points so as not to physically intersect said vertical traces;

conductive straps that electrically connect the interrupted paths of said horizontal traces thereby forming continuous conduction paths in the horizontal direction which maintain electrical isolation from said vertical traces;

means for electrically connecting said input/output signal contacts of one or more of said integrated circuit devices to said vertical traces;

means for electrically connecting said power, and ground contacts of one or more of said integrated circuit devices to said horizontal traces; and

means for electrically connecting said horizontal and vertical traces to test pads located on peripheral regions of said semiconductor wafer.