ABSTRACT

A semiconductor memory device includes a substrate including first and second surfaces opposite to each other, a first active pattern on the first surface, a first channel pattern on the first active pattern and a first source/drain pattern connected to the first channel pattern, a gate electrode provided on the first channel pattern and extending in a first direction, the gate electrode adjacent to the first source/drain pattern in a second direction intersecting the first direction, a shared contact provided under the first source/drain pattern and the gate electrode and electrically connecting the first source/drain pattern and the gate electrode to each other, and a backside metal layer on the second surface.

FIG. 4B