

ABSTRACT

STACKED 1T-*n*MEMORY CELL STRUCTURE

5 This invention relates to memory technology and new variations on memory array architecture to incorporate certain advantages from both cross-point and 1T-1Cell architectures. The fast read-time and higher signal-to-noise of the 1T-1Cell architecture and the higher packing density of the cross-point architecture are both exploited by combining certain characteristics of these layouts. A single access transistor 16 is used
10 to read multiple memory cells, which can be stacked vertically above one another in a plurality of memory array layers arranged in a “Z” axis direction.

Fig. 2



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