

SYSTEM FOR PROCESSING A SCRAMBLED VIDEO SIGNAL

This invention concerns apparatus in a subscription television system for processing a scrambled broadcast type television signal such as a television signal having a suppressed synchronizing component. In particular, this invention concerns such apparatus in a system including a noise suppression means.

In subscription television systems television programming signals are transmitted either "over the air" or through a suitable cable network, in scrambled form. Such signals may be descrambled for viewing by means of a suitable decoder associated with the television receiver of an authorized system subscriber. The decoder is usually situated in a converter unit located external to the television receiver. The programming signals may be grouped into several levels, or tiers, each representing a different programming category such as sporting events, movies, etc. The decoder of a particular subscriber is authorized to descramble the televised programming signals in selected categories, with the televised programming signals in remaining unauthorized categories being coupled to the television receiver in an unviewable scrambled form.

A horizontal synchronization suppression technique is often used to scramble a broadcast television signal. In such a "suppressed sync" technique, scrambling is accomplished by suppressing the horizontal image synchronizing (sync) pulse component of the television signal. This causes the horizontal deflection system of the receiver to lock onto random video signal peaks during the active video line trace interval, rather than locking onto the actual horizontal sync pulses, thereby producing an unstable, unviewable displayed image.

Each system subscriber is provided with a decoder unit whose "front end" circuit includes conventional tuning, intermediate frequency (IF) and video detection stages. Also, an automatic gain control circuit, adapted for responding to the tips of horizontal sync pulses, is provided within the decoder for controlling the gain of the

tuning and IF stages in accordance with the output of the video detection stage. A sync restoration circuit operates during the suppressed sync pulse interval of the video signal developed at the output of the video detector stage for producing standard horizontal sync pulses. These sync pulses are continuously inserted in the video signal developed at the output of the video detector stage for producing a descrambled video signal suitable for viewing.

An AGC voltage derived from some recurrent parameter in the scrambled signal is applied to AGC circuits in the decoder. The descrambled video signal with restored sync pulses is afterwards impressed on a standard television channel RF carrier signal by means of an RF modulator, and then coupled as a descrambled RF television signal to an antenna input of the television receiver. Each decoder may additionally include a decode authorization circuit storing a unique subscriber code which is compared to a subscriber authorization code transmitted during a horizontal line of the vertical interval of the broadcast television signal. If the stored subscriber code and the transmitted subscriber authorization code compare favorably, a decode authorization signal is developed for enabling the decoder, the decoder otherwise being disabled. Decoder systems for descrambling a suppressed sync video signal are discussed in US patent 4,408,225 - Ensinger, et al., for example.

The size, cost and complexity of a suppressed sync video signal decoder are increased by the need for the decoder to include a tuning stage, IF stage, video detector stage, AGC stage and RF modulator. These stages (except for the modulator) duplicate stages already found in the "front end" of a television receiver. Thus it is desirable to provide a decoder which does not require such stages. Accordingly, the Electronic Industry Association (EIA) of the United States has proposed a decoder-receiver interface standard which simplifies the design of decoders for use in suppressed sync television signal systems by eliminating the need for the aforementioned tuning, IF, detector, AGC

and modulator stages in a suppressed sync decoder unit. As outlined in EIA Consumer Products Standard IS-15 "NTSC Television Receiver Audio/Video Baseband Interface Specification," the EIA decoder standard provides a mutually agreeable convention, to both television receiver manufacturers and the subscription TV industry, for the implementation of a standardized sync suppressed video decoder system.

One particularly advantageous television signal descrambling and automatic gain control system suitable for the EIA standards is disclosed in U.S. Patent application Serial No. 813,315 filed 24 December 1985 and corresponding to GB-A-2184904 filed 23 December 1986 and published 1 July 1987. That system includes an interface circuit for coupling a video signal output of a suppressed sync type decoder to existing AGC circuits of the receiver for controlling the gain of the video signal, without needing tuning, IF, detector, AGC and modulator stages in the decoder.

Television receivers commonly include a video signal responsive noise suppression circuit, such as a noise inverter, for suppressing noise pulses which occur during sync pulse intervals of the video signal by means of a signal inverting or equivalent technique. This action prevents noise pulses from disrupting the operation of subsequent sync separator circuits, and also prevents noise pulses from interfering with automatic gain control (AGC) action of the receiver.

It is herein recognized that the presence of a video signal responsive noise suppression circuit such as a noise inverter in a television receiver may adversely affect the processing of a scrambled television signal such as a suppressed sync signal. For example, with a suppressed sync type scrambled signal, vertical blanking interval signal components may not be suppressed when the vertical blanking interval is intended to contain coded information, typically in digital (binary) form, for use by the scrambled signal decoder. The coded information may represent an authorization code for enabling an otherwise disabled decoder to operate, a code which identifies the type of scrambling used, or a code which assists in the

descrambling process in some way, for example.

According to one aspect of the invention, there is provided in a system for processing a broadcast type television signal and suitable for use with a video signal decoder responsive to a scrambled television signal, said system having a video signal channel including input means for receiving a broadcast type television signal and video detector means responsive to a received television signal for producing a detected baseband video signal, said detected video signal being subject to noise components during blanking intervals of said detected video signal, apparatus comprising: noise suppressing means responsive to said detected video signal for providing an output video signal with suppressed noise components during the blanking intervals; and means for inhibiting the operation of said noise suppressing means when descrambling of a scrambled television signal is in process.

According to another aspect, there is provided in combination with a system for processing an unscrambled broadcast type television signal and a scrambled broadcast type television signal, said system having a video signal channel including input means for receiving a broadcast type television signal and video detector means responsive to received unscrambled and scrambled television signals for providing detected unscrambled and scrambled video signals, apparatus comprising noise suppressing means responsive to detected video signals for providing output video signals with suppressed noise components during video signal blanking intervals; decoder means responsive to scrambled detected video signals for providing a descrambled video signal; means for providing a control signal indicative of said decoder being operative for descrambling a scrambled video signal; and means for coupling said control signal to a control input of said noise suppressing means to inhibit the operation thereof.

According to a further aspect, there is provided in a system for processing a broadcast type television signal and suitable for use with a video signal decoder responsive to a scrambled video signal, apparatus comprising

input means for receiving a television signal, said input means including means for producing an intermediate frequency (IF) signal; detector means responsive to said IF signal for producing a detected baseband video signal, said detected video signal, being subject to noise components during blanking intervals of said detected video signal; gain control means having an output coupled to said input means, and an input; noise suppressing means responsive to said detected video signal for providing, to said input of said gain control means and to said decoder, an output video signal with suppressed noise components during the blanking intervals; and means for inhibiting the operation of said noise suppressing means when descrambling of a scrambled television signal is in process.

15 In the Drawing:

FIGURE 1 shows a portion of a television receiver with apparatus embodying the present invention, as well as suppressed sync restoration apparatus;

FIGURE 2 shows additional details of apparatus embodying to the present invention;

FIGURE 3 illustrates signal waveforms helpful in understanding the operation of the sync restoration apparatus of FIGURE 1;

FIGURE 4 shows a network, in block diagram form, suitable for use in a suppressed sync decoder included in the system of FIGURE 1;

FIGURE 5 depicts a simplified version of a portion of AGC circuits of the receiver;

FIGURE 6 illustrates a transfer characteristic of an AGC detector associated with the receiver AGC circuits;

FIGURE 7 is a table summarizing operating characteristics of the disclosed sync restoration and gain control apparatus; and

FIGURE 8 illustrates the transfer characteristic of a decoder interface network included in the system of FIGURE 1.

In FIGURE 1, a source 40 is a source of RF television (TV) signals which include suppressed sync scrambled RF TV signals such as may be provided by a cable

TV subscription service. In some systems the television signal may contain unsuppressed digital information in reference portions of vertical blanking intervals. The digital information represents coded data which may be used
5 by a scrambled signal decoder under scrambled signal conditions, as mentioned previously.

The RF signals from source 40 are coupled to a television receiver, e.g., including a tuner 42, filter 44 and other units as will be discussed, where it is
10 demodulated to produce scrambled video and sound representative signals. A decoder unit 100, external to the receiver, restores the sync component of the scrambled video signal, and the restored sync (unscrambled) video signal is processed by the receiver in a conventional
15 fashion to produce an image. As will be explained in detail later, the receiver includes provision for controlling the signal gain of the tuner RF stage and the IF stage in the presence of scrambled, suppressed sync signals. In this manner separate tuner, IF and AGC stages
20 need not be provided in decoder 100.

More specifically, in FIGURE 1 tuner 42 receives the RF signals from source 40 and selectively translates the RF signal of a selected TV channel to an intermediate frequency (IF) signal including video and sound carriers
25 at, e.g., 45.75 MHz and 41.25 MHz, respectively. The IF signal includes an amplitude modulated (AM) video carrier of the vestigial sideband type representing the composite video information, and a frequency modulated (FM) sound carrier containing the sound information.

The IF output signal from tuner 42 is coupled via
30 a preamplifier and an adjacent channel sound trap (not shown) to inputs of a dual channel IF surface acoustic wave (SAW) filter 44 such as the T1802 SAW filter available from Toshiba Corporation. The IF signal from tuner 42 is split
35 into two separate channels for sound and video information demodulation in accordance with the quasi-parallel principle via the dual channels of SAW filter 44, each

channel exhibiting a bandpass response around the respective carriers.

A first differential output 44a of SAW filter 44 associated with the video channel is coupled to signal input terminals 4 and 5 of a network 45 included e.g., in an integrated circuit. This coupling is via an inductance-resistance circuit 46 which tunes out the capacitance normally associated with the SAW filter output, and via an AC coupling capacitor 47. The video channel portion of SAW filter 44 associated with output 44a exhibits a response which matches the vestigial sideband video component of the IF signal and which attenuates the 41.25 MHz sound carrier signal.

The quasi-parallel sound channel portion of SAW filter 44 associated with a differential output 44b is coupled to signal input terminals 8 and 9 of network 45 in the same manner as the video component via an inductance-resistance circuit 48 and an AC coupling capacitor 49. The sound channel portion of SAW filter 44 exhibits a double tuned response with a first peak amplitude response at the sound carrier frequency and a second peak amplitude response at the video carrier frequency.

In the video IF channel, the video component of the IF signal at input terminals 4 and 5 of network 45 is coupled to an IF amplifier stage 50 which includes plural gain controllable IF amplifiers. The amplified video component from stage 50 is AC coupled to both a limiter 52 and a video detector 54 (e.g., a four quadrant multiplier). A bandpass filter tank circuit 59 coupled via terminals 26 and 27 to the output of limiter 52 and to second inputs of detector 54 is tuned to the video carrier frequency of 45.75 MHz.

Limiter 52, filter 59 and video detector 54 form a synchronous detector for producing a baseband composite video signal at the output of detector 54. The composite detected video signal is coupled via an amplifier 55 to a noise inverter 56. In this case, inverter 56 changes

black-going blanking interval noise pulses below a given threshold level to prevent the noise pulses from disrupting the operation of subsequent sync separator circuits, and to prevent the noise pulses from interfering with automatic gain control (AGC) action.

The operation of noise inverter 56 is inhibited when decoder 100 is operative to descramble a suppressed sync video signal by restoring the sync component to the video signal. This is accomplished by means of a comparator 58 having an output coupled to a control input of noise inverter 56. Comparator 58 has a reference input coupled to a fixed reference voltage (+3.5 volts), a signal input coupled to an output of decoder 100 at the junction of terminal 12 and a biasing resistor 111.

When the voltage at terminal 12 is less than the +3.5 volt reference voltage applied to comparator 58, comparator 58 develops an output control signal which inhibits the operation of noise inverter 56. This occurs when the decoder is in the process of restoring a suppressed sync component of the video signal, signifying the presence of a received suppressed sync scrambled signal.

Thus noise inverter 56 is prevented from distorting or destroying information such as coded digital information which may be contained in the vertical blanking interval of the scrambled television signal. In this regard the scrambled suppressed sync signal containing such digital information, as applied to the input of decoder 100, may exhibit the form indicated by the waveform illustrated adjacent to the input of decoder 100. In the illustrated waveform digital (binary) signal information is contained in a reference portion of a vertical blanking interval V, and suppressed horizontal sync components are respectively included in horizontal blanking interval portions of horizontal line intervals H.

In this system decoder 100 is programmed to produce an output voltage of less than +3.5 volts when the

decoder is in the process of restoring suppressed sync video, and an output voltage of greater than +3.5 volts at other times. In another system, the noise inverter can be disabled in response to a voltage indicative of a switch 58' being placed in the DECODE position.

FIGURE 2 shows additional details of noise inverter 56 and the mechanism by which its operation is controlled. Circuit elements common to FIGURES 1 and 2 are identified by the same reference number.

In FIGURE 2 the inputs to comparator 58 are as previously discussed. The output of comparator 58 is coupled via a transistor 150 to a control input of an electronic switch 165 associated with noise inverter 56. A comparator 160 also included in noise inverter 56 receives a detected video signal from video detector 54, 55 in FIGURE 1 at an inverting input (-), and receives a positive reference voltage + VREF at a non-inverting input (+).

The output of comparator 160 is also coupled to the control input of electronic switch 165. Reference voltage VREF applied to comparator 160 substantially corresponds to the -50 IRE level of a detected baseband video signal from detector 54, 55. Electronic switch 165 receives a detected video signal from detector 54, 55 at one input, and a substitution voltage V_s (substantially corresponding to the +40 IRE level of a detected video signal) at another input. An output of switch 165 is coupled via a buffer amplifier 168 to automatic gain control (AGC) detector 62 and a video output buffer 57 in FIGURE 1.

Noise inverter 56 is enabled whenever the detected video signal applied to comparator 160 exhibits a magnitude less than (i.e., less positive than) reference voltage VREF. At such time the output of comparator 160 goes positive, causing switch 165 to operate and substitute voltage V_s into the detected video signal. Thus negative-going noise pulses are replaced by positive-going voltage V_s . Normally switch 165 occupies the position

shown for coupling a detected video signal to AGC detector 62.

The operation of noise inverter 56 is inhibited whenever the voltage at terminal 12 is less than +3.5 volts, which causes transistor 150 to conduct. The conduction of transistor 150 causes a low voltage to be developed at the control input of switch 165, whereby switch 165 remains in the normal position as illustrated for conducting a detected video signal to AGC detector 62, regardless of the output status of comparator 160.

Other aspects of the system of FIGURE 1 will now be described in detail.

The baseband video signal output of noise inverter 56 is coupled via a terminal 25, buffer amplifier 57 and a switch 58' to a video signal processor 60 including, e.g., sync separator, luminance and chrominance frequency selection, and luminance and chrominance processing circuits for developing R, G, B color image representative signals as known.

The baseband video output signal from noise inverter 56 is also coupled to an AGC peak detector 62 which peak detects the horizontal sync component of the baseband video signal to develop an AGC control voltage related to the magnitude of the sync component. This AGC control voltage is developed across a filter capacitor 64 coupled to a terminal 30 of circuit 45. The AGC voltage is also coupled via a current determining resistor 65 to an AGC filter network including a resistor 68 and a storage capacitor 69 connected to terminal 1 of circuit 45.

An AGC control voltage appearing at terminal 1 is coupled via an AGC amplifier 66 to a gain control input of IF amplifier stage 50 for controlling the gain of the amplifiers within stage 50 in accordance with the level of the detected sync pulse to maintain a desired signal gain for the video IF channel.

The AGC voltage at terminal 1 is also applied to an RF AGC comparator amplifier 70, which provides an amplified AGC voltage to a gain control input of tuner 42

via an RF AGC circuit 72. RF AGC circuit 72 is of conventional design and includes a comparator responsive to a reference voltage and to the AGC voltage derived from terminal 1 for providing an output gain control signal which determines the gain status (e.g., minimum or maximum gain) of tuner 42. A potentiometer 74 coupled via a terminal 2 to a reference input of comparator 70 establishes the operating threshold of RF AGC comparator 70 to determine the point at which comparator 70 conveys the AGC control voltage to circuit 72.

An automatic fine tuning (AFT) peak detector 75, operatively associated with a bandpass filter tank 76 tuned to the 45.75 MHz video carrier, responds to the amplitude limited video IF carrier signal from limiter 52 for developing an AFT voltage which is coupled via a buffer amplifier 77 and a terminal 29 to an AFT control input of tuner 42 to maintain proper tuning of tuner 42.

In the sound IF channel, the IF signals at terminals 8 and 9 including sound and video components are coupled to an IF amplifier stage 80 which includes plural gain controllable amplifiers. An amplified IF signal from stage 80 is AC coupled to a limiter 82, to a video IF detector 84, and to a sound IF detector 86. The output of limiter 82 is directly coupled to video IF detector 84 and via a capacitive phase shifting network 87 to sound IF detector 86. Detectors 84 and 86 illustratively comprise four quadrant multipliers.

A bandpass filter tank 85 coupled via terminals 22 and 23 to the output of limiter 82 is tuned to the video IF carrier. Limiter 82, detector 86 and tank 85 form a mixer for providing a 4.5 MHz FM intercarrier sound signal from the sound and video components of the IF signal.

The intercarrier sound signal from detector 86 is coupled via an amplifier 88, a terminal 21, a buffer 89, a 4.5 MHz bandpass filter 90 and terminals 18 and 19 to a limiter network comprising cascaded progressive limiting stages 91, 92 and 93. The stages 91-93 provide an amplitude limited FM intercarrier sound signal to an FM

detector 95. Detector 95 operates together with a discriminator tank circuit 96 coupled to terminals 15 and 16 for generating a demodulated baseband audio signal. The audio signal is applied via terminal 14 to an audio signal processor stage (not shown) including audio amplifiers.

Automatic gain control of the sound IF channel is achieved in response to a control voltage derived from the output of video IF detector 84. The detected output signal of detector 84 is coupled via an amplifier 78, a low pass AGC filter including a resistor 79 and a capacitor 81 coupled to terminal 10, and an AGC amplifier 83 to a gain control input of sound IF amplifier stage 80.

The system of FIGURE 1 also includes a suppressed sync decoder 100 designed in accordance with the proposed EIA standard. The baseband composite video signal from terminal 25 of circuit 45 is applied to a signal input of decoder 100 via buffer 57 which exhibits a suitable output driving impedance, e.g., 75 ohms. A baseband video signal "A" with a restored horizontal sync component is provided from one output of decoder 100 to a decoder interface network 110 in circuit 45 via an input terminal 12.

Interface 110 includes a comparator circuit for developing an output control signal which modifies the charge on AGC filter capacitor 69 and augments the action of the video AGC circuits particularly in the presence of received suppressed sync signals. A potentiometer 112 coupled to terminal 13 provides a reference voltage VR to a reference input of the comparator in interface 110.

A DC voltage "B" provided from another output of decoder 100 controls the operation of an electronic switch 115 to which a filter capacitor 117 is coupled. In the absence of decoder 100, no DC voltage is applied to switch 115 and capacitor 117 is decoupled from the AGC filter network including resistor 68 and capacitor 69. When decoder 100 is connected to the system, control voltage "B" causes switch 115 to be placed in the position shown whereby filter capacitor 117 is connected across AGC filter

capacitor 69, thereby increasing the AGC time constant associated with video signal AGC action.

The longer AGC time constant is necessary for stability when the decoder is active to compensate for normally expected signal processing delays (as large as 1 millisecond, or five horizontal lines) inherent in the operation of the decoder and recognized by the EIA standard. The normal, faster AGC time constant using filter capacitor 69 alone represents a compromise between a need for a time constant fast enough to accommodate a channel change condition, and a time constant slow enough to be immune to the effects of aircraft induced "flutter".

An output signal "C" from decoder 100 is a restored sync video signal developed as will be described below. The decoder output lines on which restored sync video signals "A" and "C" appear could be connected together internally to decoder 100 so that a single decoder output line results. However, some systems may require two separate decoder output lines, e.g., with one output line (C) conveying a signal with both restored sync and video information to be displayed, and another output signal line (A) conveying a composite synchronizing signal with restored sync but without video information, for a specialized use. In this example decoder output signals A and C are similar restored sync video signals containing information to be displayed.

Restored sync decoder output signal "C" is selectively coupled to video signal processor 60 via switch 58' and an AC coupling capacitor 120. Switch 58' can be a manual viewer controlled switch, or a microprocessor controlled electronic switch responsive to both user selection signals and automatic control signals received from the decoder, depending on the characteristics of a particular decoder system. Switch 58' is placed in a DECODE position when decoder 100 is present and operative to decode a received suppressed sync television signal. Switch 58' is placed in a NORMAL (illustrated) position when decoder 100 is absent or inoperative in the presence of a

received television signal with proper (non-suppressed) sync.

In the presence of a suppressed sync television signal, the input signal to decoder 100 always exhibits suppressed sync because the decoder input signal line is not included in the sync restoration control loop. Briefly, the decoder input line receives only a suppressed sync signal via output 44a of SAW filter 44, IF amplifiers 50, video detector 54 and buffer 57. One decoder output line provides a restored sync video signal C to video processor 60, and another decoder output line provides a restored sync video signal A to AGC circuits of the receiver via interface network 110 for maintaining correct receiver signal gain.

The operation of decoder 100 in conjunction with interface 110 and the AGC circuits of the receiver will now be described in detail.

Decoder 100 and the video AGC circuits of the receiver form an automatic gain control system for suppressed sync signal conditions. In accordance with the EIA standards a video signal gain change is not required when the sync tip voltage is +1.0 volt. A gain change is required, however, when the sync tip voltage is more or less than +1.0 volt. More specifically, a gain change is not required when "GM" as defined in expression (1) below is substantially equal to unity, but a gain change is required when GM is other than unity:

$$GM = \frac{2.143v. - 1.0v.}{2.143v. - DRS} \quad (1)$$

where

GM is a gain multiplier factor;
2.143v. is the voltage associated with the 120 IRE video signal level (zero carrier voltage);
1.0 v. is the desired sync tip voltage level; and
DRS is the actual sync tip voltage of a decoder restored sync component from the output of decoder 100.

When expression (1) is solved for the term DRS, expression (2) below results:

$$\text{DRS} = 2.143\text{v.} - \frac{1.143\text{v.}}{\text{GM}}$$

(2)

If the gain is wrong, e.g., too high as is typical for a suppressed sync signal, the decoder will produce an output DRS level (during the sync interval) of less than +1.0 volt, for example. This DRS level is sensed by interface 110 which then acts to modify the charge on AGC capacitor 69 as required to produce a desired correct video signal gain and an attendant DRS sync tip voltage of approximately +1.0 volt.

This is accomplished by means of comparator and current source circuits in interface network 110. The decoder itself does not produce a "correct" DRS sync tip level of +1.0 volts immediately upon receipt of a suppressed sync video signal, because the receiver would then have no means of knowing whether or not the video signal gain should be changed.

Various techniques are known for developing a suppressed sync signal. FIGURE 3 illustrates waveforms representing both one type of a suppressed sync signal, and a decoder restored sync (DRS) output signal from decoder 100. In the suppressed sync signal the normally negative going (below 0 IRE) horizontal sync component has been replaced with a 1 MHz burst marker of approximately 80 IRE peak-to-peak amplitude centered between the 0 IRE and 100 IRE levels.

If the amplitude of the received suppressed sync signal is correct, the 80 IRE burst marker will cause a given voltage to be produced when peak detected, as will be discussed subsequently. Otherwise, under incorrect gain conditions, the amplitude detected burst marker will cause another voltage, signifying that a gain change is required to be produced. The decoder restored sync (DRS) output signal from decoder 100 has a negative-going restored sync component of a magnitude which signifies to the receiver, via interface network 110, the amount of signal gain change required, if any.

FIGURE 4 illustrates a portion of a decoder arrangement suitable for restoring the sync component of a suppressed sync signal as shown in FIGURE 3.

In FIGURE 4, a suppressed sync video signal of the burst marker type is filtered by a bandpass filter 130 which passes the burst marker signal frequency. The filtered burst marker component is amplitude detected by a peak-to-peak envelope detector 132, which provides an output signal representative of the magnitude of the sync interval burst marker component. It is extremely unlikely that a false peak detector output will be produced by 1 MHz video signal image interval components, since 1 MHz video signal components are unlikely to appear with sufficient energy to produce an output from peak detector 132 corresponding to the detected output produced by the relatively high energy 1 MHz burst marker.

The detected burst marker from detector 132 is applied to one input of a comparator 134, another input of which receives a reference voltage VREF. The magnitude of the detected burst marker signal exceeds VREF under substantially all expected conditions, whereby comparator 134 produces an output GATE timing signal coincident with the sync interval. The GATE signal signifies the presence of the sync interval, and is employed as will be discussed below.

From expression (2) discussed previously, the sync tip voltage of the decoder restored sync (DRS) signal from decoder 100 is given by

$$\text{DRS} = 2.143\text{v.} - \frac{1.143\text{v}}{\text{GM}} \quad (2)$$

Gain multiplier factor GM is the ratio of the constant peak-to-peak detected sync interval burst marker voltage (V_1) which is expected to appear at the output of detector 132 under correct signal gain conditions to the variable peak-to-peak detected burst marker voltage (V_2) which is actually developed at the output of detector 132. Thus expression (2) can be rewritten as expressions (3) or (3a) below:

$$\text{DRS} = 2.143\text{v.} - \frac{1.143\text{v.}}{(V_1/V_2)} \quad (3)$$

or

$$\text{DRS} = 2.143\text{v.} - [1.143\text{v.}/V_1] V_2 \quad (3a)$$

- 5 Under correct video signal gain conditions $V_1 = V_2$, i.e., the burst marker amplitude is correct, and the DRS sync tip level is +1.0 volt as desired for correct video signal gain conditions.

10 The transfer function represented by expression (3a) can be implemented by means of the portion of the network in FIGURE 4 including an amplifier 140 and a differential amplifier 142.

Amplifier 140 translates detected signal V_2 with a constant amplification factor $K=1.143/V_1$, where V_1 is a constant. Amplifier 140 may act as an amplifier, an
 15 attenuator, or as a unity gain amplifier for values of K greater than unity, less than unity or unity, respectively. The output signal from amplifier 140 is applied to an inverting input (-) of differential amplifier 142. A
 20 reference voltage of +2.143 volts is applied to a non-inverting input (+) of differential amplifier 142. Amplifier 142 provides an output DRS voltage in accordance with expression (3a).

The DRS output voltage from amplifier 142 is
 25 applied to one input of an electronic switch 145, another input of which receives the suppressed sync video signal, e.g., as derived from input circuits of decoder 100. The position of switch 145 is controlled by the GATE signal from the output of comparator 134 such that during each
 30 sync interval, switch 145 is placed in the position shown for conveying the DRS voltage to the decoder output. At other times, when the GATE signal is absent, switch 145 is placed in its other position whereby the remaining portion of the video signal is conveyed to the decoder output.
 35 Thus during each sync interval, switch 145 substitutes the DRS voltage from amplifier 142 for the burst marker in the suppressed sync video signal to thereby produce a video

signal with a restored sync component at the output of the decoder.

As mentioned previously, the sync tip voltage of the restored sync video signal will be substantially equal to +1.0 volt under correct signal gain conditions, or less than +1.0 volt if the gain is too high, for example. The latter condition will be sensed by interface network 110, which will act to adjust the AGC circuits of the receiver to produce a correct video signal gain. Under incorrect video signal gain conditions, the AGC circuits of the receiver will respond to a control current output of interface network 110 related to the DRS output level of decoder 100 for incrementally changing the video signal gain toward the desired correct gain. The AGC circuit action causes the amplitude of the suppressed sync video signal applied to the input of decoder 100 to incrementally approach the correct peak-to-peak video signal amplitude, and the restored sync component of video signals A and C from the output of decoder 100 will incrementally approach the desired correct value of +1.0 volt.

The operation of the receiver AGC system for both normal and suppressed sync conditions is described in detail below with regard to FIGURES 5-8.

FIGURE 5 depicts a simplified version of the receiver video AGC system of FIGURE 1, wherein corresponding elements are identified by the same reference number. AGC detector 62, a negative peak detector, charges capacitor 64 with a voltage related to the magnitude of the negative-going peaks of the detected baseband video signal, i.e., the sync tips in the case of a conventional television signal. Resistor 65 converts the voltage on capacitor 64 to a current, I , which represents a charging component of AGC capacitor 69. A current, I' , conducted by a current source associated with interface network 110 represents a discharging component of capacitor 69. The magnitude of current I' varies in accordance with the nature of a given suppressed sync condition.

A total AGC current I_T equal to the difference between currents I and I' represents the net charging current of capacitor 69 and serves to develop a voltage across capacitor 69 which is conveyed to AGC circuits of the receiver via amplifiers 65 and 70. Current I_T equals zero for correct gain steady state conditions.

AGC detector 62 exhibits a gain change vs. current conduction characteristic as shown in FIGURE 6. The detector exhibits a linear gain change up to a gain increase of +0.5 db and up to a gain decrease of -0.5 db, and a nonlinear response for gain changes above and below +0.5 db and -0.5 db. Detector 62 operates in a saturated region in the nonlinear case, exhibiting either a positive saturation current output $I_s(+)$ or a negative saturation current output $I_s(-)$. In the saturated region the rate at which the voltage on capacitor 69 is permitted to change is restricted to help maintain the stability of the AGC control loop. An AGC detector characteristic with linear and nonlinear (saturated) regions such as that illustrated is well known and widely used in television receiver AGC systems.

With the decoder connected to the receiver under suppressed sync conditions, correct video signal gain will be established for steady state conditions. The internal AGC system of the receiver alone would be unable to achieve correct gain under suppressed sync signal conditions, and would produce a video signal with too much gain. The overall AGC system including the combination of decoder 100, interface 110 and the existing internal AGC system of the receiver operates in a similar way to the way the internal AGC system of the receiver operates alone under normal, non-suppressed sync conditions to establish correct gain.

Under steady state conditions when correct gain is achieved and the DRS sync tip voltage substantially equals +1.0 volt, current I conducted to terminal 1 from the output of peak detector 62 substantially equals current I' conducted from terminal 1 via interface 110, i.e.,

interface current I' opposes current I to maintain a correct gain condition.

FIGURES 7 and 8 illustrate the operation of the system for correct gain (steady state) and incorrect gain conditions with respect to both normal sync and suppressed sync video signals. As seen from FIGURE 7, for a steady state correct gain condition manifested by a DRS sync tip voltage of substantially +1.0 volt, currents I and I' both exhibit a magnitude equal to that of detector saturation current $I_s(+)$, and AGC current I_T is zero whereby no gain change is produced. FIGURE 7 also indicates the magnitudes of current I , I' and I_T for an incorrect high gain condition with a decoder restored sync tip voltage of less than +1.0 volt (initially, before correction is achieved), and for an incorrect low gain condition with a decoder restored sync tip voltage of greater than +1.0 volt (initially). A high gain condition is typically experienced with a suppressed sync signal. A low gain condition is uncommon, but can arise momentarily due to an "overcorrection" which may exist briefly before the DRS gain control action has stabilized just before correct gain is achieved.

The values of interface current I' shown in the table of FIGURE 7 are produced in accordance with the voltage versus current response of interface network 110, which is illustrated by FIGURE 8.

As seen from FIGURE 8, interface network 110 produces an output current I' equal to 13 times saturation current $I_s(+)$ when the DRS sync tip voltage is substantially equal to +1.0 volt under correct signal gain conditions. The "13 times" multiplier factor is required because the interface network develops output current I' only during each horizontal synchronizing interval in response to the DRS signal from decoder 100. That is, current I' is a horizontal rate current pulse rather than a continuous DC current. The horizontal synchronizing interval encompasses only about 1/13 of the total horizontal line interval. Without the "13 times"

multiplier, interface output current I' , which must reach the I_s and $2I_s$ levels would average only $1/13$ of the level required to produce the desired I_s and $2I_s$ levels. The "times" multiplier assures that current I' can reach the I_s and $2I_s$ levels.

Interface network 110 is inactive (nonconductive) and produces a substantially zero output current for input voltages of approximately +1.3 volts and greater, where +1.3 volts corresponds to the blanking level of a restored sync signal with correct gain. Breakpoint voltages +0.93 volts and +1.06 volts are the voltages required to achieve results consistent with the AGC detector characteristic shown in FIGURE 6. Specifically, breakpoint voltages +0.93 volts and +1.06 volts for the interface transfer characteristic of FIGURE 8 respectively relate to the -0.5 db and +0.5 db gain change breakpoints for the AGC detector characteristic of FIGURE 6. Illustratively, a linear reduction in gain of from 0 to -0.5 db (FIGURE 6) is associated with a DRS sync tip voltage of from +1.0 to +0.93 volts (FIGURE 8). In FIGURE 6 a nonlinear gain reduction region from -0.5 db to -1.0 db and beyond is associated with a DRS sync tip voltage of less than +0.93 volts in FIGURE 8.

The transfer characteristic of FIGURE 8 is exhibited by a differential comparator with an associated current source, within interface network 110. For example, the comparator may be of the type including a pair of differentially connected transistors with interconnected emitters coupled to a common current source. Output currents are conducted via a collector output of one of the transistors, coupled to capacitor 69 via terminal 1. As determined by the gain and biasing of the differential comparator, the comparator exhibits a saturation region up to the 0.93v. breakpoint, a linear transition region between the +0.93v. and the +1.06v. breakpoints, and a cut-off region above the +1.06v. breakpoint.

The disclosed arrangement can also be used in conjunction with a video cassette recorder (VCR). In such

case a scrambled, suppressed sync television signal can be applied to a decoder for developing a restored sync video signal which would be provided as an input signal to an interface network in the VCR. The interface network would
5 provide a control signal to AGC circuits of the VCR, and the VCR would provide a gain controlled, restored sync video information signal to a television receiver which need not include a decoder interface network.

CLAIMS:

1. In a system for processing a broadcast type television signal and suitable for use with a video signal decoder responsive to a scrambled television signal, said system having a video signal channel including input means for receiving a broadcast type television signal and video detector means responsive to a received television signal for producing a detected baseband video signal, said detected video signal being subject to noise components during blanking intervals of said detected video signal, apparatus comprising:

noise suppressing means responsive to said detected video signal for providing an output video signal with suppressed noise components during the blanking intervals; and

means for inhibiting the operation of said noise suppressing means when descrambling of a scrambled television signal is in process.

2. Apparatus according to Claim 1, wherein: said scrambled television signal exhibits a suppressed synchronizing (sync) component subject to restoration by said decoder.

3. Apparatus according to Claim 1, wherein said noise suppressing means comprises means for selectively coupling a prescribed voltage in place of said detected video signal in response to a first control signal representative of the presence of noise components during said blanking intervals; and

said inhibiting means comprises means for developing a second control signal indicative of the operation of said decoder for descrambling a scrambled video signal, said second control signal being applied to said noise suppression means for inhibiting the operation thereof.



4. In combination with a system for processing an unscrambled broadcast type television signal and a scrambled broadcast type television signal, said system having a video signal channel including input means for
- 5 receiving a broadcast type television signal and video detector means responsive to received unscrambled and scrambled television signals for providing detected unscrambled and scrambled video signals, apparatus comprising:
- 10 noise suppressing means responsive to detected video signals for providing output video signals with suppressed noise components during video signal blanking intervals;
- decoder means responsive to scrambled detected
- 15 video signals for providing a descrambled video signal;
- means for providing a control signal indicative of said decoder being operative for descrambling a scrambled video signal; and
- means for coupling said control signal to a
- 20 control input of said noise suppressing means to inhibit the operation thereof.



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5. In a system for processing a broadcast type television signal and suitable for use with a video signal decoder responsive to a scrambled video signal, apparatus comprising:

- 5 input means for receiving a television signal, said input means including means for producing an intermediate frequency (IF) signal;
- detector means responsive to said IF signal for producing a detected baseband video signal, said detected
- 10 video signal, being subject to noise components during blanking intervals of said detected video signal;
- gain control means having an output coupled to said input means, and an input;
- noise suppressing means responsive to said
- 15 detected video signal for providing, to said input of said gain control means and to said decoder, an output video signal with suppressed noise components during the blanking intervals; and
- means for inhibiting the operation of said noise
- 20 suppressing means when descrambling of a scrambled television signal is in process.

6. Apparatus according to Claim 5, wherein said noise suppressing means comprises:

- 25 a comparator with an input for receiving a detected video signal, an input for receiving a reference voltage, and an output for providing a control signal; and
- switching means with an input for receiving a detected video signal, an input for receiving a reference
- 30 voltage, a switching control input responsive to said control signal from said comparator output, and an output coupled to said input of said noise suppressing means and to said decoder.



7. Apparatus according to Claim 6, wherein
said inhibiting means comprises a comparator with
an input for receiving a reference voltage, an input for
receiving a signal indicative of the presence of said
5 decoder for descrambling a scrambled video signal, and an
output for providing a control signal to said control input
of said switching means.

8. A system for processing a broadcast type
10 television signal substantially as herein described with
reference to the accompanying drawings.
