WHAT IS CLAIMED IS:

1. A nonvolatile memory comprising:

a first memory chip;

a second memory chip;

a clock pin, which is commonly connected to the first and second memory chips, configured to receive an external clock signal during a training period; and

an input/output pin commonly connected to the first and second memory chips,

wherein the first memory chip includes,

a first duty correction circuit (DCC) configured to perform a first duty correction operation on a first internal clock signal based on the external clock signal, and

a first output buffer connected between an output terminal of the first DCC and the input/output pin,

wherein the second memory chip includes,

a second DCC configured to perform a second duty correction operation on a second internal clock signal based on the external signal, and

a second output buffer connected between an output terminal of the second DCC and the input/output pin, and

wherein the first and second duty correction operations are performed in parallel during the training period.

2. The nonvolatile memory of claim 1, wherein, during the training period, the first and second output buffers are configured to be disabled, and the input/output pin is configured to be floated.

3. The nonvolatile memory of claim 1, wherein, during the training period, only the first output buffer is configured to be enabled, the second output buffer is configured to be disabled, and an output of the first output buffer is configured to be output to an outside through the input/output pin.

4. The nonvolatile memory of claim 1, wherein the first memory chip further comprises: a first internal circuit configured to receive the external clock signal

through the clock pin and generate the first internal clock signal from the received external clock signal, and

the second memory chip further comprises: a second internal circuit configured to receive the external clock signal through the clock pin and generate the second internal clock signal from the received external clock signal.

5. The nonvolatile memory of claim 1, wherein the external clock signal is a read enable signal configured to toggle at a frequency during the training period.

6. The nonvolatile memory of claim 5, wherein the read enable signal is configured to toggle at the frequency regardless of operations of the first and second output buffers during the training period.

7. The nonvolatile memory of claim 1, wherein the external clock signal is a data strobe signal configured to toggle at a frequency during the training period.

8. The nonvolatile memory of claim 1, wherein the training period comprises a number of clock cycles.

9. The nonvolatile memory of claim 1, wherein the first memory chip is configured to start the first duty correction operation upon receiving a duty correction start command and to end the first duty correction operation upon receiving a duty correction end command, and

the second memory chip is configured to start the second duty correction operation upon receiving the duty correction start command and to end the second duty correction operation upon receiving the duty correction end command.

10. The nonvolatile memory of claim 1, wherein the first memory chip is configured to start the first duty correction operation upon receiving a first set feature command and to end the first duty correction operation upon receiving a second set feature command, and

the second memory chip is configured to start the second duty correction operation upon receiving the first set feature command and to end the second duty correction operation upon receiving the second set feature command.

11. The nonvolatile memory of claim 1, further comprising:

a buffer chip located between the clock pin, the input/output pin, and the first and second memory chips, and configured to receive the external clock signal through the clock pin and to buffer the received external clock signal to provide a buffered external clock signal to the first and second memory chips.

12. The nonvolatile memory of claim 11, wherein the buffer chip comprises a third duty correction circuit (DCC) configured to perform a third duty correction operation on an output of the first output buffer or the second output buffer.

13. A nonvolatile memory comprising:

a clock pin configured to receive an external clock signal during a training period;

an input/output pin configured to transmit and receive a data signal or a data strobe signal;

a buffer chip connected to the clock pin and the input/output pin and configured to buffer the external clock signal to generate a buffered external clock signal;

a first memory chip configured to perform a first duty correction operation on a first internal clock signal based on the buffered external clock signal; and

a second memory chip configured to perform a second duty correction operation on a second internal signal based on the buffered external clock signal, the first and second duty correction operations being performed in parallel during the training period,

wherein the buffer chip includes,

a first duty correction circuit (DCC) configured to perform a third duty correction operation on an output signal received from the first memory chip or the second memory chip; and

a first output buffer connected between an output terminal of the first DCC and the input/output pin.

14. The nonvolatile memory of claim 13, wherein, during the training period, the first output buffer is configured to be disabled, and the input/output pin is configured to be floated.

15. The nonvolatile memory of claim 13, wherein, during the training period, the first output buffer is configured to be an enabled first output buffer, and an output of the enabled first output buffer is configured to be output to an outside through the input/output pin.

16. The nonvolatile memory of claim 13, wherein the first memory chip comprises:

a second DCC configured to perform the first duty correction operation on the first internal clock signal; and

a second output buffer connected between an output terminal of the second DCC and the buffer chip, and

the second memory chip comprises:

a third DCC configured to perform the second duty correction operation on the second internal clock signal; and

a third output buffer connected between an output terminal of the third DCC and the buffer chip.

17. The nonvolatile memory of claim 16, wherein, during the training period, only the second output buffer is configured to be an enabled second output buffer, the third output buffer is configured to be disabled, and an output of the enabled second output buffer is configured to be provided to the buffer chip.

18. The nonvolatile memory of claim 13, wherein the external clock signal is a read enable signal configured to toggle at a frequency during the training period.

19. A nonvolatile memory comprising:

a clock pin configured to receive an external clock signal during a training period;

an input/output pin configured to transmit and receive a data signal or a data strobe signal; and

a memory chip connected to the clock pin and the input/output pin,

wherein the memory chip includes,

an internal circuit configured to receive the external clock signal through the clock pin and generate an internal clock signal from the received external clock signal;

a duty correction circuit (DCC) configured to perform a duty correction operation on the internal clock signal; and

an output buffer connected between an output terminal of the DCC and the input/output pin, and

wherein, during the training period, the output buffer is configured to be disabled, and the input/output pin is configured to be floated.