CLAIMS

1. A method for performing low-density parity-check (LDPC) decoding, the method comprising: receiving log-likelihood ratios (LLRs) corresponding to bits encoded using LDPC encoding; updating the LLRs for each of the encoded bits corresponding to columns of a parity check matrix (PCM), the bit LLRs indicating a probability of a value of each of the encoded bits; determining, for each of the encoded bits, an a posteriori LLR for a row of the PCM by processing each LLR within the row, wherein for a first set of the encoded bits, determining the a posteriori LLR comprises using a first number of outdated LLRs, and wherein for a second set of the encoded bits, determining the a posteriori LLR comprises using a second number of updated LLRs, wherein the first set of the encoded bits and the second set of the encoded bits comprise all of the encoded bits; utilizing the LLRs to decode the encoded bits.

2. The method of claim 1, wherein updating the LLRs is based on a corresponding a posteriori LLR.

3. The method of claim 2, wherein updating the LLRs based on the corresponding a posteriori LLR comprises updating the LLRs based on a difference between a corresponding outdated a posteriori LLR and a corresponding updated a posteriori LLR.

4. The method of claim 1, further comprising storing a first set of updated LLRs corresponding to a third set of the encoded bits in a first memory bank, and storing a second set of updated LLRs corresponding to a fourth set of the encoded bits in a second memory bank, wherein the third set of the encoded bits and the fourth set of the encoded bits comprise all of the encoded bits.

5. The method of claim 4, further comprising reading from the second memory bank at the same time as reading from the first memory bank.

6. The method of claim 4, further comprising selecting bits for the third set of the encoded bits or the fourth set of the encoded bits based on dependencies between rows of the PCM.

7. The method of claim 6, further comprising determining an ordering for updating the bit LLRs based on dependencies between rows in the PCM.

8. The method of claim 1, wherein utilizing the LLRs to decode the encoded bits comprises performing layered decoding on the encoded bits utilizing the LLRs.

9. An apparatus for performing low-density parity-check (LDPC) decoding, comprising: at least one processor configured to: receive log-likelihood ratios (LLRs) corresponding to bits encoded using LDPC encoding; update the LLRs for each of the encoded bits corresponding to columns of a parity check matrix (PCM), the bit LLRs indicating a probability of a value of each of the encoded bits; determine, for each of the encoded bits, an a posteriori LLR for a row of the PCM by processing each LLR within the row, wherein for a first set of the encoded bits, determining the a posteriori LLR comprises using a first number of outdated LLRs, and wherein for a second set of the encoded bits, determining the a posteriori LLR comprises using a second number of updated LLRs, wherein the first set of the encoded bits and the second set of the encoded bits comprise all of the encoded bits; and utilize the LLRs to decode the encoded bits; and a memory coupled with the at least one processor.

10. The apparatus of claim 9, wherein updating the LLRs is based on a corresponding a posteriori LLR.

11. The apparatus of claim 10, wherein updating the LLRs based on the corresponding a posteriori LLR comprises updating the LLRs based on a difference between a corresponding outdated a posteriori LLR and a corresponding updated a posteriori LLR.

12. The apparatus of claim 9, wherein the at least one processor is further configured to store a first set of updated LLRs corresponding to a third set of the encoded bits in a first memory bank, and store a second set of updated LLRs corresponding to a fourth set of the encoded bits in a second memory bank, wherein the third set of the encoded bits and the fourth set of the encoded bits comprise all of the encoded bits, and wherein the memory comprises the first memory bank

and the second memory bank.

13. The apparatus of claim 12, wherein the at least one processor is further configured to read from the second memory bank at the same time as reading from the first memory bank.

14. The apparatus of claim 12, wherein the at least one processor is further configured to select bits for the third set of the encoded bits or the fourth set of the encoded bits based on dependencies between rows in the PCM.

15. The apparatus of claim 14, wherein the at least one processor is further configured to determine an ordering for updating the bit LLRs based on dependencies between rows in the PCM.

16. The apparatus of claim 9, wherein the at least one processor is configured to utilize the LLRs to decode the encoded bits by performing layered decoding on the encoded bits utilizing the LLRs.

17. An apparatus for performing low-density parity-check (LDPC) decoding, comprising: means for receiving log-likelihood ratios (LLRs) corresponding to bits encoded using LDPC encoding; means for updating the LLRs for each of the encoded bits corresponding to columns of a parity check matrix (PCM), the bit LLRs indicating a probability of a value of each of the encoded bits; means for determining, for each of the encoded bits, an a posteriori LLR for a row of the PCM by processing each LLR within the row, wherein for a first set of the encoded bits, determining the a posteriori LLR comprises using a first number of outdated LLRs, and wherein for a second set of the encoded bits, determining the a posteriori LLR comprises using a second number of updated LLRs, wherein the first set of the encoded bits and the second set of the encoded bits comprise all of the encoded bits; means for utilizing the LLRs to decode the encoded bits.

18. The apparatus of claim 17, wherein the means for updating further comprise means for updating the LLRs based on a corresponding a posteriori LLR.

19. The apparatus of claim 18, wherein the means for updating the LLRs based on the corresponding a posteriori LLR further comprise means for updating the LLRs based on a difference between a corresponding outdated a posteriori LLR and a corresponding updated a posteriori LLR.

20. The apparatus of claim 17, further comprising means for storing a first set of updated LLRs corresponding to a third set of the encoded bits in a first memory bank, and means for storing a second set of updated LLRs corresponding to a fourth set of the encoded bits in a second memory bank, wherein the third set of the encoded bits and the fourth set of the encoded bits comprise all of the encoded bits.

21. The apparatus of claim 20, further comprising means for reading from the second memory bank at the same time as reading from the first memory bank.

22. The apparatus of claim 20, further comprising means for selecting bits for the third set of the encoded bits or the fourth set of the encoded bits based on dependencies between rows in the PCM.

23. The apparatus of claim 22, further comprising means for determining an ordering for updating the bit LLRs based on dependencies between rows in the PCM.

24. The apparatus of claim 17, wherein the means for utilizing further comprise means for utilizing the LLRs to decode the encoded bits by performing layered decoding on the encoded bits utilizing the LLRs.

25. A non-transitory computer-readable medium for performing low-density parity-check (LDPC) decoding, comprising instructions that, when executed by at least one processor, configures the at least one processor to: receive log-likelihood ratios (LLRs) corresponding to bits encoded using LDPC encoding; update the LLRs for each of the encoded bits corresponding to columns of a parity check matrix (PCM), the bit LLRs indicating a probability of a value of each of the encoded bits; determine, for each of the encoded bits, an a posteriori LLR for a row

of the PCM by processing each LLR within the row, wherein for a first set of the encoded bits, determining the a posteriori LLR comprises using a first number of outdated LLRs, and wherein for a second set of the encoded bits, determining the a posteriori LLR comprises using a second number of updated LLRs, wherein the first set of the encoded bits and the second set of the encoded bits comprise all of the encoded bits; and utilize the LLRs to decode the encoded bits.

26. The non-transitory computer-readable medium of claim 25, wherein updating the LLRs is based on a corresponding a posteriori LLR, and wherein updating the LLRs based on the corresponding a posteriori LLR comprises updating the LLRs based on a difference between a corresponding outdated a posteriori LLR and a corresponding updated a posteriori LLR.

27. The non-transitory computer-readable medium of claim 25, further comprising instructions that configure the at least one processor to store a first set of updated LLRs corresponding to a third set of the encoded bits in a first memory bank, and store a second set of updated LLRs corresponding to a fourth set of the encoded bits in a second memory bank, wherein the third set of the encoded bits and the fourth set of the encoded bits comprise all of the encoded bits.

28. The non-transitory computer-readable medium of claim 27, further comprising reading from the second memory bank at the same time as reading from the first memory bank.

29. The non-transitory computer-readable medium of claim 27, further comprising at least one of: selecting bits for the third set of the encoded bits or the fourth set of the encoded bits based on dependencies between rows of the PCM; or determining an ordering for updating the bit LLRs based on dependencies between rows in the PCM.

30. The non-transitory computer-readable medium of claim 25, wherein the instructions for utilizing the LLRs to decode the encoded bits comprises instructions that cause the at least one processor to perform layered decoding on the encoded bits utilizing the LLRs.