



## INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

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| <p><b>(21) International Application Number:</b> PCT/US00/05420</p> <p><b>(22) International Filing Date:</b> 29 February 2000 (29.02.00)</p> <p><b>(30) Priority Data:</b><br/>         09/267,796                      12 March 1999 (12.03.99)                      US</p> <p><b>(71) Applicant (for all designated States except US):</b> INTEL CORPORATION [US/US]; 2200 Mission College Boulevard, Santa Clara, CA 95052 (US).</p> <p><b>(72) Inventors; and</b><br/> <b>(75) Inventors/Applicants (for US only):</b> SHAHIDZADEH, Shahrokh [US/US]; 16036 S.W. Waxwing Way, Beaverton, OR 97007 (US). BIGBEE, Bryant, E. [US/US]; 645 S.W. 195th Court, Aloha, OR 97006 (US). PAPWORTH, David, B. [US/US]; P.O. Box 6296, Beaverton, OR 97007 (US). BINNS, Frank [US/GB]; 1810 S.W. Manna Drive, Hillsboro, OR 97123 (US). COLWELL, Robert, P. [US/US]; 3594 N.W. Bronson Crest Loop, Portland, OR 97229 (US).</p> <p><b>(74) Agents:</b> MILLIKEN, Darren, J. et al.; Blakely, Sokoloff, Taylor &amp; Zafman LLP, 7th floor, 12400 Wilshire Boulevard, Los Angeles, CA 90025 (US).</p> | <p><b>(81) Designated States:</b> AE, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CR, CU, CZ, DE, DK, DM, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, US, UZ, VN, YU, ZA, ZW, ARIPO patent (GH, GM, KE, LS, MW, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).</p> <p><b>Published</b><br/> <i>With international search report.</i></p> |
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**(54) Title:** LINEAR ADDRESS EXTENSION AND MAPPING TO PHYSICAL MEMORY USING 4 AND 8 BYTE PAGE TABLE ENTRIES IN A 32-BIT MICROPROCESSOR

**(57) Abstract**

A microprocessor for providing an extended linear address of more than 32 bits. The extended linear address may be provided by concatenating a linear address with a segment selector extension, or by concatenating the values from two registers. Hierarchical translation of a linear address to a physical address is performed in which the number of levels in the hierarchy depends upon whether the linear address is an extended linear address.

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graph TD
    914[SEGMENT EXTENSION] --> 912[LINEAR ADDRESS]
    902[SEGMENT SELECTOR] --> 906[DESCRIPTOR TABLE]
    902 --> 908[SEGMENT DESCRIPTOR]
    908 --> Plus[+]
    910[OFFSET] --> Plus
    Plus --> 912
  
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