Abstract

STACKED FET STANDARD CELL ARCHITECTURE

A cell layout that implements stacked transistors is disclosed. The cell layout utilizes both topside metal routing and backside metal routing. Various connection routes between components of the transistors (e.g., gates, sources, and drains) and either the topside metal routing or the backside metal routing can be made. The specific connection routes can be determined based on a desired device construction. Thus, the cell layout disclosed enables various devices to be constructed based on a basic cell structure.

Figure 1