

This Sheet Has Been Replaced


REPLACED SHEETS		SG
☒ Description	: paged 1 to paged 13	
☒ Claim(s)	: paged 14 to paged 15	
☒ Drawing(s)	: paged 16 to paged 16	
☒ Abstract	: paged 17 to paged 17	
DATE OF RECEIPT		

RCA 86,980

AUTOMATIC SYNCHRONIZATION SWITCH FOR SIDE-BY-SIDE DISPLAYS

The invention relates to the field of televisions capable of displaying side-by-side pictures of substantially equal size from different sources, and in particular, to such televisions having a wide display format ratio screen. Most televisions today have a format display ratio, horizontal width to vertical height, of 4:3. A wide format display ratio corresponds more closely to the display format ratio of movies, for example 16:9. The invention is applicable to both direct view televisions and projection televisions.

Televisions with a wide display format ratio are suited to a wide variety of displays for both conventional and wide display format signals, as well as combinations thereof in multiple picture displays. However, the use of a wide display ratio screen entails numerous problems. Changing the display format ratios of multiple signal sources, developing consistent timing signals from asynchronous but simultaneously displayed sources, switching between multiple sources to generate multiple picture displays, and providing high resolution pictures from compressed data signals are general categories of such problems. A wide screen television disclosed in WO 91/19397, published December 12, 1991 and corresponding to PCT/US91/03746, is capable of providing high resolution, single and multiple picture displays, from single and multiple sources having similar or different format ratios, and with selectable display format ratios.

Such television apparatus as disclosed in WO 91/19397 can display multiple pictures simultaneously, for example from two video sources. The video sources may be the tuner in the television, a tuner in a video cassette recorder, a video camera, and others. A display mode particularly suited for a wide screen television is side-by-side pictures of substantially the same size, from different video sources, for example two different channels. In a wide screen television having a display format ratio (width to height) of 16:9, each of two side-by-side pictures of comparable size in a full screen display would have a format display ratio of 8:9. In order to fit a 4:3 picture into an 8:9 space, the 4:3 picture must be horizontally cropped or horizontally compressed, or some combination of both.

1-4783080



In order to display two pictures side-by-side, the display is locked to one of two incoming signals, referred to as the first signal or first picture for convenience. This can be the left picture or the right picture in the side-by-side mode. However the first picture may become nonfunctional. For example, the television receiver could be tuned to a blank channel, or the television station could go off the air, or the video source could be interrupted. If the first picture becomes nonfunctional, the synchronization for the second picture is also lost. Without proper synchronization, the second picture will jitter.

The first picture signal is monitored to prevent the loss of display synchronization when the first picture signal is lost. A display system for side-by-side pictures according to an inventive arrangement comprises a first circuit for separating a first composite synchronizing signal from a first video signal having a conventional format display ratio and a second circuit for separating a second composite synchronizing signal from a second video signal having the same conventional format display ratio. A detecting circuit senses the presence of the first video signal, by monitoring the horizontal synchronizing component thereof. A video display control circuit has a mode of operation in which pictures representative of the first and second video signals are displayed in side-by-side relationship and substantially without image aspect ratio distortion. A synchronization switch selects one of the first and second composite synchronizing signals for synchronizing the video display. The second composite synchronizing signal is automatically selected unless the horizontal synchronizing component of the first video signal is detected.

The detecting circuit comprises a synchronizing component separator, a bandpass filter, and a detector. When the first video signal is present, the horizontal synchronizing signal is separated and monitored. The detecting circuit generates an output signal indicating whether an adequate horizontal synchronizing component is present. The invention further comprises a microprocessor coupled to the detecting circuit and the automatic synchronization switch. The microprocessor controls the automatic synchronization switch output to be the second composite synchronizing signal when the first video signal is not detected by the detecting circuit.



The invention further comprises a first signal processing means for speeding up the first video signal, a video display means synchronized with the automatic synchronization switch output, means for vertically synchronizing the second video signal with the first video signal and the video display means, a second signal processing means for speeding up said second video signal, and means for combining the first and second processed video signals for side-by-side display. The first and second signal processing means can crop and reduce picture size so that the first and second pictures can be displayed on a wide screen display.

Thus, the second picture can be displayed in a side-by-side video display system despite the loss of the first picture.

FIGURE 1 is a block diagram of an automatic synchronization switch in a wide screen television.

FIGURE 2 is a timing diagram of the composite video signal processed by the detecting circuit shown in FIGURE 1.

FIGURE 3 is a circuit diagram of a sync separator and bandpass filter adapted to be used in the detecting circuit.

FIGURE 4 is a circuit diagram of a detector with hysteresis adapted to be used in the detecting circuit.

FIGURE 5 is a block diagram of the bandpass filter adapted to be used in the detecting circuit.

FIGURE 6 illustrates the response of the bandpass filter of FIGURES 3 and 5.

FIGURE 7 is a block diagram of a wide screen television adapted for operation at $2f_H$ horizontal scanning.

FIGURE 8 is a block diagram of the gate array of FIGURE 7, illustrating the main, auxiliary and output signal paths.

An overall block diagram for a wide screen television apparatus in accordance with WO 91/19397, and adapted to operate with $2f_H$ horizontal scanning, is shown in FIGURE 7 and generally designated 10. The television 10 generally comprises a video signals input section 20, a chassis or TV microprocessor (TV μ P) 216, a wide screen processor 30, a $1f_H$ to $2f_H$ converter 40, a deflection circuit 50, an RGB interface 60, a YUV to RGB converter 240, kine drivers 242, direct view or projection tubes 244 and a power supply 70. The YUV to RGB converter 240 may be an industry type TA7730. The grouping of various circuits into different



functional blocks is made for purposes of convenience in description, and is not intended as limiting the physical position of such circuits relative to one another.

The video signals input section 20 is adapted for receiving a plurality of composite video signals from different video sources. The video signals may be selectively switched for display as main and auxiliary video signals. An RF switch 204 has two antenna inputs ANT1 and ANT 2. These represent inputs for both off-air antenna reception and cable reception. The RF switch 204 controls which antenna input is supplied to a first tuner 206 and to a second tuner 208. The output of first tuner 206 is an input to a one-chip 202, which performs a number of functions related to tuning, horizontal and vertical deflection and video controls. The particular one-chip shown is industry designated type TA7777. The baseband video signal VIDEO OUT developed in the one-chip and resulting from the signal from first tuner 206 is an input to both video switch 200 and the TV1 input of wide screen processor 30. Other baseband video inputs to video switch 200 are designated AUX1 and AUX 2. These might be used for video cameras, laser disc players, video tape players, video games and the like. The output of the video switch 200, which is controlled by the chassis or TV microprocessor 216 is designated SWITCHED VIDEO. The SWITCHED VIDEO is another input to wide screen processor 30.

A switch SW1 wide screen processor selects between the TV1 and SWITCHED VIDEO signals as a SEL COMP OUT video signal which is an input to a Y/C decoder 210. The Y/C decoder 210 may be implemented as an adaptive line comb filter. Two further video sources S1 and S2 are also inputs to the Y/C decoder 210. Each of S1 and S2 represent different S-VHS sources, and each consists of separate luminance and chrominance signals. A switch, which may be incorporated as part of the Y/C decoder, as in some adaptive line comb filters, or which may be implemented as a separate switch, is responsive to the TV microprocessor 216 for selecting one pair of luminance and chrominance signals as outputs designated Y_M and C_IN respectively. The selected pair of luminance and chrominance signals is thereafter considered the main signal and is processed along a main signal path. Signal designations including _M or _MN refer to the main signal path. The chrominance signal C_IN is



redirected by the wide screen processor back to the one-chip, for developing color difference signals U_M and V_M . In this regard, U is an equivalent designation for $(R-Y)$ and V is an equivalent designation for $(B-Y)$. The Y_M , U_M , and V_M signals are converted
5 to digital form in the wide screen processor for further signal processing.

A second tuner 208, functionally defined as part of the wide screen processor 30, develops a baseband video signal $TV2$. A switch $SW2$ selects between the $TV2$ and SWITCHED VIDEO signals
10 as an input to a Y/C decoder 220. The Y/C decoder 220 may be implemented as an adaptive line comb filter. Switches $SW3$ and $SW4$ select between the luminance and chrominance outputs of Y/C decoder 220 and the luminance and chrominance signals of an external video source, designated Y_{EXT} and C_{EXT} respectively. The
15 Y_{EXT} and C_{EXT} signals correspond to the S-VHS input $S1$. The Y/C decoder 220 and switches $SW3$ and $SW4$ may be combined, as in some adaptive line comb filters. The output of switches $SW3$ and $SW4$ is thereafter considered the auxiliary signal and is processed along an auxiliary signal path. The selected luminance output is designated
20 Y_A . Signal designations including $_A$, $_AX$ and $_AUX$ refer to the auxiliary signal path. The selected chrominance is converted to color difference signals U_A and V_A . The Y_A , U_A and V_A signals are converted to digital form for further signal processing. The arrangement of video signal source switching in the main and
25 auxiliary signal paths maximizes flexibility in managing the source selection for the different parts of the different picture display formats.

A composite synchronizing signal COMP SYNC, corresponding to Y_M is provided by the wide screen processor to a sync separator
30 212. The horizontal and vertical synchronizing components H and V , respectively are inputs to a vertical countdown circuit 214. The vertical countdown circuit develops a VERTICAL RESET signal which is directed into the wide screen processor 30. The wide screen processor generates an internal vertical reset output signal INT
35 VERT RST OUT directed to the RGB interface 60. A switch in the RGB interface 60 selects between the internal vertical reset output signal and the vertical synchronizing component of the external RGB source. The output of this switch is a selected vertical



synchronizing component SEL_VERT_SYNC directed to the deflection circuit 50. Horizontal and vertical synchronizing signals of the auxiliary video signal are developed by sync separator 250 in the wide screen processor.

- 5 The $1f_H$ to $2f_H$ converter 40 is responsible for converting interlaced video signals to progressively scanned noninterlaced signals, for example one wherein each horizontal line is displayed twice, or an additional set of horizontal lines is generated by interpolating adjacent horizontal lines of the same field. In some
- 10 instances, the use of a previous line or the use of an interpolated line will depend upon the level of movement which is detected between adjacent fields or frames. The converter circuit 40 operates in conjunction with a video RAM 420. The video RAM may be used to store one or more fields of a frame, to enable the
- 15 progressive display. The converted video data as Y_{2f_H} , U_{2f_H} and V_{2f_H} signals is supplied to the RGB interface 60.

The RGB interface 60 enables selection of the converted video data or external RGB video data for display by the video signals input section. The external RGB signal is deemed to be a wide format

20 display ratio signal adapted for $2f_H$ scanning. The vertical synchronizing component of the main signal is supplied to the RGB interface by the wide screen processor as INT VERT RST OUT, enabling a selected vertical sync (f_{vm} or f_{vext}) to be available to the deflection circuit 50. Operation of the wide screen television

25 enables user selection of an external RGB signal, by generating an internal/external control signal INT/EXT. However, the selection of an external RGB signal input, in the absence of such a signal, can result in vertical collapse of the raster, and damage to the cathode ray tube or projection tubes. Accordingly, the RGB interface circuit

30 detects an external synchronizing signal, in order to override the selection of a non-existent external RGB input. The WSP microprocessor 340 also supplies color and tint controls for the external RGB signal.

The wide screen processor 30 comprises a picture in picture

35 processor 320 for special signal processing of the auxiliary video signal. A gate array 300 combines the main and auxiliary video signal data in a wide variety of display formats. The picture-in-picture processor (PIP) 320 and gate array 300 are under the control



of a wide screen microprocessor (WSP μ P) 340. Microprocessor 340 is responsive to the TV microprocessor 216 over a serial bus. The serial bus includes four signal lines, for data, clock signals, enable signals and reset signals. The wide screen processor 30 also
5 generates a composite vertical blanking/reset signal, as a three level sand castle signal. Alternatively, the vertical blanking and reset signals can be generated as separate signals. A composite blanking signal is supplied by the video signal input section to the RGB interface.

10 The deflection circuit 50 receives a vertical reset signal from the wide screen processor, a selected $2f_H$ horizontal synchronizing signal from the RGB interface 60 and additional control signals from the wide screen processor. These additional control signals relate to horizontal phasing, vertical size adjustment and east-west pin
15 adjustment. The deflection circuit 50 supplies $2f_H$ flyback pulses to the wide screen processor 30, the $1f_H$ to $2f_H$ converter 40 and the YUV to RGB converter 240.

Operating voltages for the entire wide screen television are generated by a power supply 70 which can be energized by an AC
20 mains supply.

The gate array 300 is responsible for combining video information from the main and auxiliary signal paths to implement a composite wide screen display. The main video signal is supplied to the wide screen processor in analog form, and Y U V format, as
25 signals designated Y_M, U_M and V_M. These main signals are converted from analog to digital form by analog to digital converters. The main signal path 304, auxiliary signal path 306 and output signal path 312 of the gate array 300 are shown in block diagram form in FIGURE 8. The gate array also comprises a
30 clocks/sync circuit 320 and a WSP μ P decoder 310. Data and address output lines of the WSP μ P decoder 310, identified as WSP DATA, are supplied to each of the main circuits and paths identified above, as well as to the picture-in-picture processor 320 and resolution processing circuit 370.

35 The gate array is responsible for expanding, compressing and cropping video data of the main video channel, as and if necessary, to implement different picture display formats. The luminance component Y_MN is stored in a first in first out (FIFO) line memory



356 for a length of time depending on the nature of the interpolation of the luminance component. The combined chrominance components U/V_MN are stored in FIFO 358. Auxiliary signal luminance and chrominance components Y_PIP, U_PIP and V_PIP are developed by demultiplexer 355. The luminance component undergoes resolution processing, as desired, in circuit 357, and is expanded as necessary by interpolator 359, generating signal Y_AUX as an output.

In some instances, the auxiliary display will be as large as the main signal display. The memory limitations associated with the picture-in-picture processor and video RAM 350 may provide an insufficient number of data points, or pixels for filling such a large display area. In those circumstances, resolution processing circuit 357 can be used to restore pixels to the auxiliary video signal to replace those lost during data compression, or reduction. As an example, circuit 357 may be a dedithering circuit if the video signal has previously been dithered.

The auxiliary video input data is sampled at a $640f_H$ rate and stored in video RAM 350. The auxiliary data is read out of video RAM 350 is designated VRAM_OUT. The PIP circuit 301 also has the capability of reducing the auxiliary picture by equal integer factors horizontally and vertically, as well as asymmetrically. The auxiliary channel data is buffered and synchronized to the main channel digital video by the 4-bit latches 352, the auxiliary FIFO 354 and clocks/sync circuit 320. The VRAM_OUT data is sorted into Y (luminance), U, V (color components), and FSW_DAT (fast switch data) by demultiplexer 355. The FSW_DAT indicates which field type was written into the video RAM. The PIP_FSW signal is received directly from the PIP circuit and applied to the output MUX control circuit 321 to determine which field read out of video RAM is to be displayed during the small picture modes.

The auxiliary channel is sampled at $640f_H$ rate while the main channel is sampled at a $1024f_H$ rate. The auxiliary channel FIFO 354 converts the data from the auxiliary channel sample rate to the main channel clock rate. In this process, the video signal undergoes an $8/5$ ($1024/640$) compression. This is more than the $4/3$ compression necessary to correctly display the auxiliary channel signal. Therefore, the auxiliary channel must be expanded by the interpolator 359 to correctly display a 4 X 3 small picture. The



M 24 11 93

interpolator 359 is controlled by interpolator control circuit 371, which is itself responsive to WSP μ P 340. The amount of interpolator expansion required is $5/6$. The expansion factor X is determined as follows:

5
$$X = (640/1024) * (4/3) = 5/6$$

The chrominance components U_PIP and V_PIP are delayed by circuit 367 for a length of time depending on the nature of the interpolation of the luminance component, generating signals U_AUX and V_AUX as outputs. The respective Y, U and V components of the
10 main and auxiliary signals are combined in respective multiplexers 315, 317 and 319 in the output signal path 312, by controlling the read enable signals of the FIFO's 354, 356 and 358. The multiplexers 315, 317 and 319 are responsive to output multiplexer control circuit 321. Output multiplexer control circuit 321 is responsive to
15 the clock signal CLK, the start of line signal SOL, the H_COUNT signal, the vertical blanking reset signal and the output of the fast switch from the picture-in-picture processor and WSP μ P 340. The multiplexed luminance and chrominance components Y_MX, U_MX and V_MX are supplied to respective digital/analog converters 360, 362
20 and 364 respectively. The digital to analog converters are followed by low pass filters. The various functions of the picture-in-picture processor, the gate array and the data reduction circuit are controlled by WSP μ P 340. The WSP μ P 340 is responsive to the TV
25 μ P 216, being connected thereto by a serial bus. The serial bus may be a four wire bus as shown, having lines for data, clock signals, enable signals and reset signals. The WSP μ P 340 communicates with the different circuits of the gate array through a WSP μ P decoder 310.

In one case, it is necessary to compress the 4 X 3 NTSC video
30 by a factor of $4/3$ to avoid aspect ratio distortion of the displayed picture. In the other case, the video can be expanded to perform horizontal zooming operations usually accompanied by vertical zooming. Horizontal zoom operations up to 33% can be accomplished by reducing compressions to less than $4/3$. A sample interpolator is
35 used to recalculate the incoming video to a new pixel positions because the luminance video bandwidth, up to 5.5 MHz for S-VHS format, occupies a large percentage of the Nyquist fold over frequency, which is 8 MHz for a $1024f_H$ clock.



24 11 00

The luminance data Y_MN is routed through an interpolator 337 in the main signal path 304 which recalculates sample values based on the compression or the expansion of the video. The function of the switches or route selectors 323 and 331 is to reverse the topology of the main signal path 304 with respect to the relative positions of the FIFO 356 and the interpolator 337. In particular, these switches select whether the interpolator 337 precedes the FIFO 356, as required for compression, or whether the FIFO 356 precedes the interpolator 337, as required for expansion. The switches 323 and 331 are responsive to a route control circuit 335, which is itself responsive to the WSP μ P 340. During small picture modes the auxiliary video signal is compressed for storage in the video RAM 350, and only expansion is necessary for practical purposes. Accordingly, no comparable switching is required in the auxiliary signal path.

FIGURE 1 illustrates a video display system with an automatic synchronization switch, which can be implemented in a wide screen television apparatus as disclosed in WO 91/19397. A first picture video signal or main video signal is separated into luminance Y and color C components by comb filter 734. A first composite synchronizing signal separator 732 derives a first composite synchronizing signal from the Y component of the first video signal. This first composite synchronizing signal is delivered to the first input 704 of automatic synchronization switch 700, which can be an industry type TA7348.

A second picture video signal or auxiliary video signal is separated into Y and C components by comb filter 724. A second composite synchronizing signal separator 726 derives a second composite synchronizing signal from the Y component of the second video signal. Synchronizing component separator 721 produces horizontal and vertical synchronizing signals from the second video signal. The horizontal and vertical synchronizing signals are delivered to a horizontal phase locked loop (PLL) and vertical countdown circuit 723 and then to the pix-in-pix processor 725. The pix-in-pix processor operates in conjunction with a digital to analog converter 720 and a field store video RAM 718. A composite synchronizing signal output from the pix-in-pix processor is fed to the second input 702 of synchronization switch 700.



RCA 86,980

The automatic synchronization switch output 706 is connected to the synchronizing component separator 712 and the horizontal PLL and vertical countdown circuit 714. Circuit 714 generates horizontal and vertical drive signals for synchronizing the deflection and display means. Also, digital Y and C components are generated for the first and second video signals. The main analog to digital converter 728, connected to demodulator 730, supplies a digitized first video signal to the wide screen processor 30. The second analog to digital converter 720 and the field store 718 supply a digitized second video signal to the wide screen processor 30. Demodulator 722 supplies second chroma signals (R-Y) and (B-Y) to converter 720. The wide screen processor 30 assembles the first and second pictures, for example as side-by-side pictures. The assembled picture is converted back to Y, U and V analog signals by digital to analog (D/A) converter 731

The automatic synchronization switch output 706 is controlled by a video signal/synchronizing signal detecting circuit 710 and microprocessor 708. The detecting circuit 710 senses the presence of the first video signal by separating and monitoring the horizontal synchronizing component of the first video signal. If the detecting circuit 710 detects the presence of the first video signal, the automatic synchronization output 706 will be the first composite synchronizing signal. If the video/sync sense circuit 710 fails to detect the presence of the first video signal or the first composite synchronizing signal, the automatic synchronization switch output 706 will be the second composite synchronizing signal. As a result, the second video picture can be displayed without jitter distortion even if the first video picture is missing. The source of synchronizing signals for controlling the wide screen display will be automatically shifted to the second video signal if the first video signal is missing or the synchronizing component of the first video signal is inadequate. Hysteresis in switching is provided to prevent unnecessary switching of the synchronization switch due to temporary conditions affecting the detection or adequacy of the horizontal synchronizing component in the first video signal.

Microprocessor 708 can comprise a Motorola MC 68HC05T2 type chip also known as Telekat and responds to the output from the video/sync sense circuit 710 which indicates the presence or



absence of the first video signal. If the display system is operating in the main picture only mode, microprocessor 708 can produce, for example, a blue display field and the characters "NO SIGNAL" when the main picture signal is not detected. If the display system is
5 operating in the PIP, or POP, or side-by-side mode, the microprocessor 708 directs the automatic synchronization switch 700 to produce the second synchronizing signal as an output 706. Thus, the auxiliary second signal controls the display synchronization when the main or first video signal is not detected
10 and jitter in the second picture is thereby avoided.

FIGURES 3 and 4 are detailed circuit diagrams of the detecting circuit. FIGURE 3 illustrates the synchronizing component separator 801 with clipping and the band pass filter 803 of the detecting circuit 710. The first video signal is received on the 0.1 microfarad
15 (μf) capacitor 802. The biasing for transistor Q1 is supplied by resistors 804 and 806. Transistor Q1 cuts off all the active video above V_{BE} as illustrated in FIGURE 2. Thus, the synchronizing signal is produced at output 805. The output 805 of synchronizing component separator 801 is connected to the input of band pass
20 filter 803 by resistor 808. The twin-T bandpass filter 803 shown in FIGURES 3 and 5 is an active filter. Transistor Q2 in FIGURE 3 and operational amplifier 819 in FIGURE 5 provide the inverting gain for the active filter 803. Bandpass filter 803 further comprises a 47 Kohm resistor 808, two 100 picofarad (pf) capacitors 810, 814, a
25 200 pf capacitor 812, and two 100 Kohm resistors 816, 818. As shown in FIGURE 6, only horizontal synchronizing components near the center frequency of 15.7 KHz are passed by the bandpass filter 803. The inverted horizontal synchronizing components from the band pass filter 803 are connected to the detector 807. Hysteresis
30 is provided by 1 μf capacitor 824. When an adequate synchronizing signal component is present, transistor Q3 turns on and charges the 2.2 μf capacitor 834. This causes transistor Q4 to turn on and indicate that sense line 840 has gone high. Hysteresis from 1 Mohm resistor 836 maintains transistor Q3 on and prevents transistor Q4
35 from switching off. Thus, sense line 840 is at a high level when the first video signal is detected and at a low level when the first video signal is not detected. The output signal from the detecting circuit 710 is coupled to microprocessor 708, which in turn controls the



24 11 55

operation of the automatic synchronization switch 700. By using the second video synchronizing signal to control display deflection when the first video signal is missing, the second picture will be displayed without distortion. Such an automatic synchronization switch can be used with picture-in-picture (PIP) and picture-outside-picture (POP) formats, as well as side-by-side picture formats.



1 2 3 4 5 6 7 8 9 10 11 12 13 14 15



What is claimed is:

1 1. A video display system, comprising means (244) for
2 simultaneously displaying pictures representative of first and
3 second video signals, characterized by;
4 means (700) for selectably synchronizing said display means
5 (244) with either one of said first and second video signals;
6 means (710) for separating a horizontal synchronizing
7 component from said first video signal;
8 means (710) for sensing said horizontal synchronizing
9 component separated from said first video signal; and,
10 means (708) for controlling said selectable synchronizing
11 means (700) responsive to said sensing means (710), for
12 synchronizing said display means (244) with said first video signal
13 when said horizontal synchronizing component separated from said
14 first video signal is sensed and for otherwise synchronizing said
15 display means (244) with said second video signal.

1 2. The video display system of claim 1, wherein said
2 separating means (710) is characterized by an active filter (803).

1 3. The video display system of claim 1, wherein said
2 separating means (710) is characterized by a bandpass filter (803).

1 4. The video display system of claim 1, wherein said
2 separating means (710) is characterized by an active bandpass filter
3 (803).

1 5. The video display system of claim 1, wherein said
2 separating means (710) is characterized by:
3 means (801) for generating from said first video signal an
4 intermediate signal including said horizontal synchronizing
5 component;
6 a filter (803) for extracting said horizontal synchronizing
7 component from said intermediate signal.

1 6. The system of claim 1, wherein said sensing means (710) is
2 characterized by a hysteresis characteristic.



1 7. The system of claim 1, wherein said means (708) for
2 controlling said selectable synchronizing means (700) is
3 characterized by a microprocessor.

1 8. The system of claim 1, wherein said video signals have
2 format display ratios and said video display means (244) is
3 characterized by a format display ratio wider than said format
4 display ratios of said video signals, and said pictures are displayed
5 side-by-side.

1 9. The system of claim 8, characterized by said pictures being
2 of substantially similar size.

This Sheet Has Been Replaced

